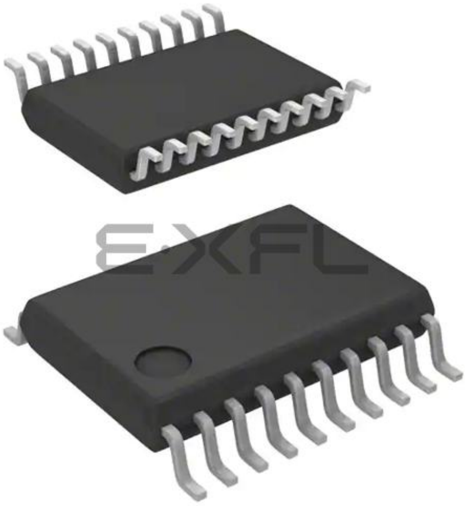

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21322ddsp-u0

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, U2RB, U2SMR5, U2SMR4, U2SMR3, U2SMR2, and U2SMR
A/D converter: Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Even address Byte Access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

Figure 9.7 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed.
To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.7.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
FMSTP Bit	VCA20 Bit					
0 (flash memory operates)	0 (internal power low consumption disabled)	0 µs	Period of system clock × 1 cycle + 60 µs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode to interrupt routine execution.
	1 (internal power low consumption enabled)	100 µs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 µs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 µs (max.)				

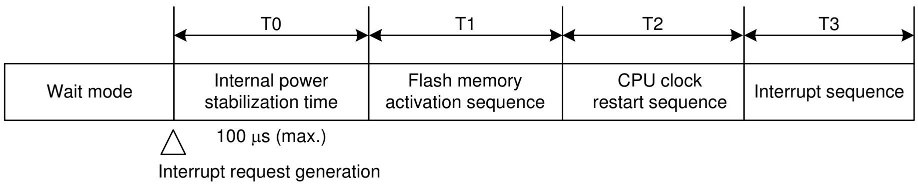


Figure 9.7 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

11.2.2 Interrupt Control Register (FMRDYIC, TRCIC)

Address 0041h (FMRDYIC), 0047h (TRCIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

13.3 Notes on Option Function Select Area

13.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)      ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows a Watchdog Timer Block Diagram.

Table 14.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selected by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

Table 15.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RC	Timer RE
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)	4-bit counter 8-bit counter
Count		Decrement	Decrement	Increment	Increment
Count sources		• f1 • f2 • f8 • fOCO • fC32 • fC	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRCCLK	• f4 • f8 • f32 • fC4
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode (output compare function)	—
	Count of the external count source	Event counter mode	—	Timer mode (output compare function)	—
	External pulse width/ period measurement	Pulse width measurement mode, pulse period measurement mode	—	Timer mode (input capture function; 4 pins)	—
	PWM output	Pulse output mode (1), Event counter mode (1)	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1), PWM mode (3 pins), PWM2 mode (1 pin)	—
	One-shot waveform output	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	PWM mode (3 pins)	—
	Three-phase waveforms output	—	—	—	—
	Timer	Timer mode (only fC32 count)	—	—	Real-time clock mode
Input pin		TRAIO	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD	—
Output pin		TRAO TRAIO	TRBO	TRCIOA, TRCIOB, TRCIOC, TRCIOD	—
Related interrupt		Timer RA interrupt	Timer RB interrupt, $\overline{\text{INT0}}$ interrupt	Compare match/input capture A to D interrupt, Overflow interrupt, $\overline{\text{INT0}}$ interrupt	Timer RE interrupt
Timer stop		Provided	Provided	Provided	Provided

Note:

1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

16.2.3 Timer RA Mode Register (TRAMR)

Address 0102h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	—	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: fC32 1 0 1: Do not set. 1 1 0: fC 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source 1: Cuts off count source	R/W

When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

16.2.4 Timer RA Prescaler Register (TRAPRE)

Address 0103h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W
	Pulse output mode		00h to FFh	R/W
	Event counter mode	Counts an external count source	00h to FFh	R/W
	Pulse width measurement mode	Measure pulse width of input pulses from external (counts internal count source)	00h to FFh	R/W
	Pulse period measurement mode	Measure pulse period of input pulses from external (counts internal count source)	00h to FFh	R/W

Note:

1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

16.2.5 Timer RA Register (TRA)

Address 0104h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts on underflow of TRAPRE register	00h to FFh	R/W

Note:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

16.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bits	Set to 0.	R/W
b3	—			
b4	—			
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.

Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

18.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Disable pin output by compare match (TRCIOA pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRA register 1 0: “H” output by compare match in the TRCGRA register 1 1: Toggle output by compare match in the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Disable pin output by compare match (TRCIOB pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRB register 1 0: “H” output by compare match in the TRCGRB register 1 1: Toggle output by compare match in the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.2.8 Operating Example

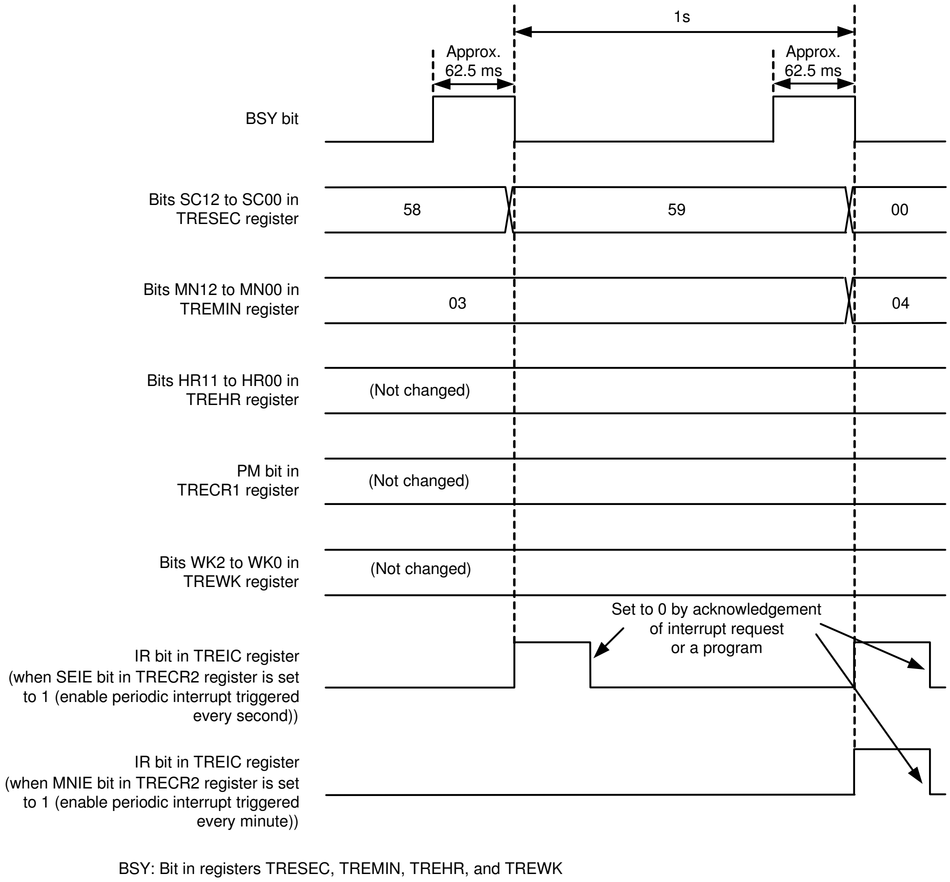


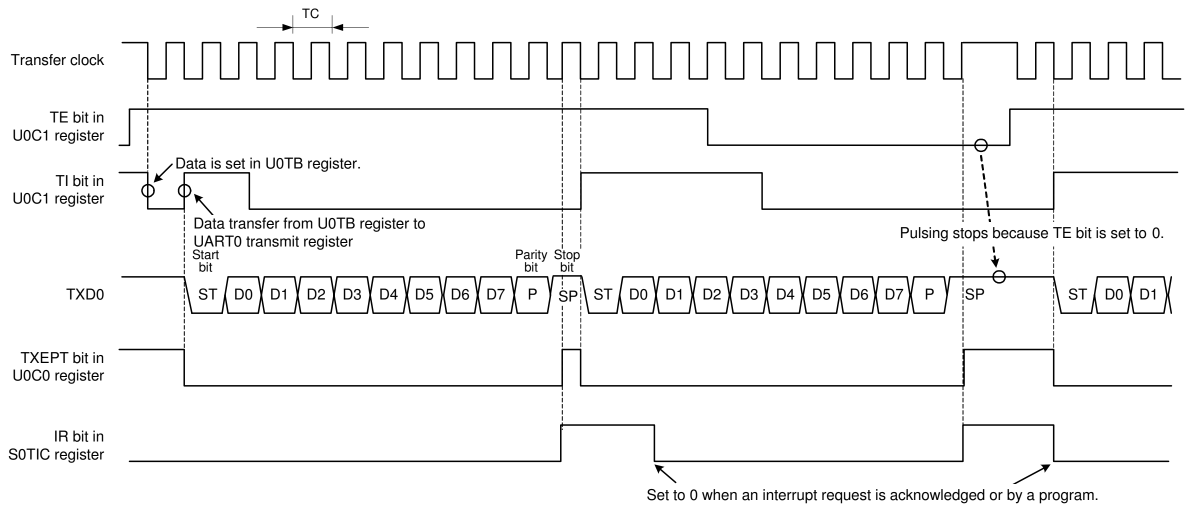
Figure 19.3 Operating Example in Real-Time Clock Mode

Table 20.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U0TB	b0 to b8	Set transmit data. (1)
U0RB	b0 to b8	Receive data can be read. (2)
	OER,FER,PER,SUM	Error flag
U0BRG	b0 to b7	Set a bit rate.
U0MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
U0C0	CLK0, CLK1	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXD0 pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 0.

Notes:
1. The bits used for transmission/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits 7 and 8 when the transfer data is 7 bits long
   - Bit 8 when the transfer data is 8 bits long

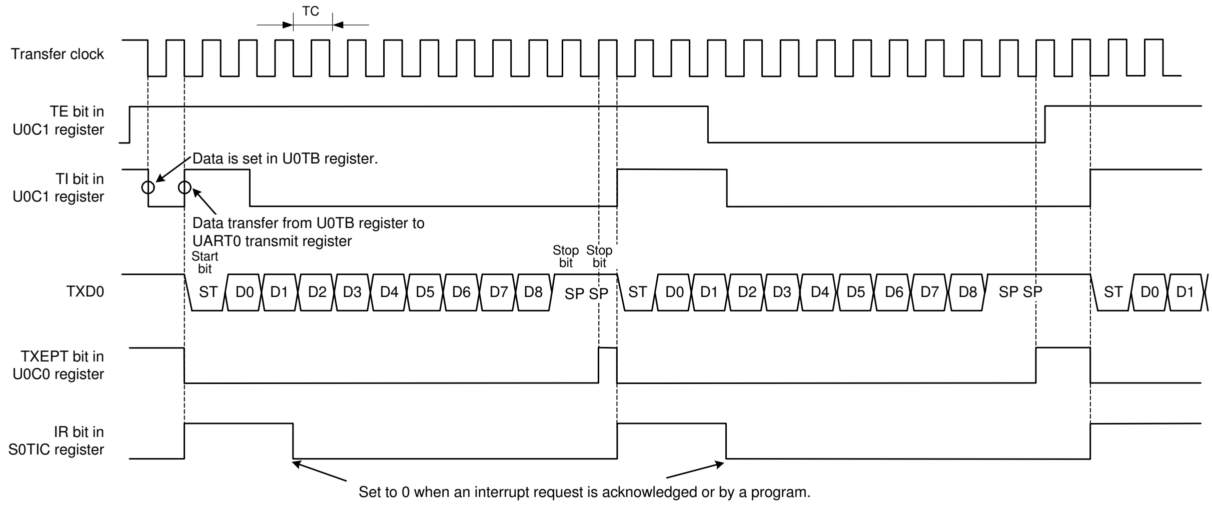
• Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in U0MR register = 1 (parity enabled)
- STPS bit in U0MR register = 0 (one stop bit)
- U0IRS bit in U0C1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)



The above applies when:
- PRYE bit in U0MR register = 0 (parity disabled)
- STPS bit in U0MR register = 1 (two stop bits)
- U0IRS bit in U0C1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

Figure 20.6 Transmit Timing in UART Mode

21. Serial Interface (UART2)

The serial interface consists of three channels, UART0 to UART2. This chapter describes the UART2.

21.1 Overview

UART2 has a dedicated timer to generate a transfer clock.
Figure 21.1 shows a UART2 Block Diagram. Figure 21.2 shows a Block Diagram of UART2 Transmit/Receive Unit. Table 21.1 lists the Pin Configuration of UART2.

UART2 has the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I^2C mode)
- Multiprocessor communication function

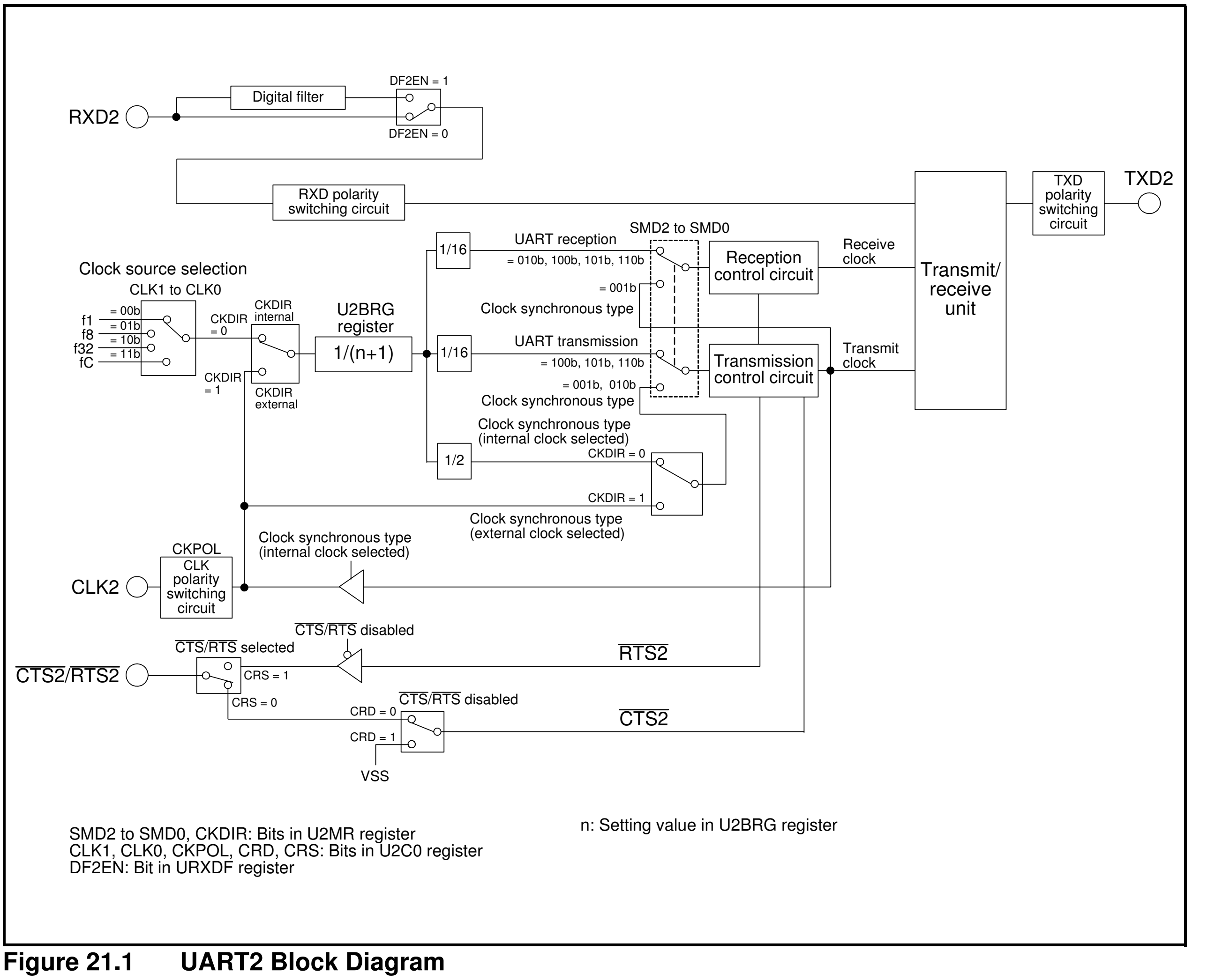


Figure 21.1 UART2 Block Diagram

21.3.3 LSB First/MSB First Select Function

Use the UFORM bit in the U2C0 register to select the transfer format. Figure 21.5 shows the Transfer Format.

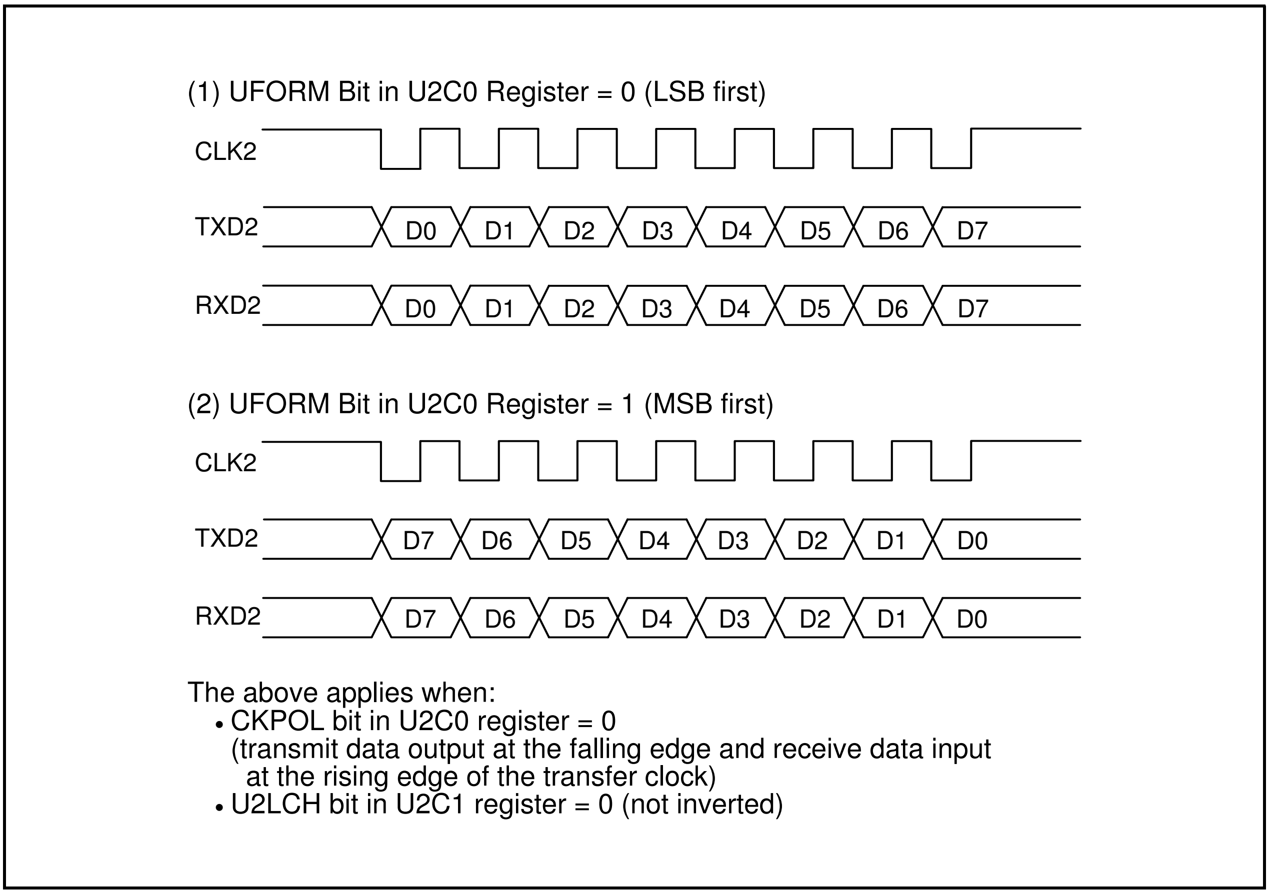


Figure 21.5 Transfer Format

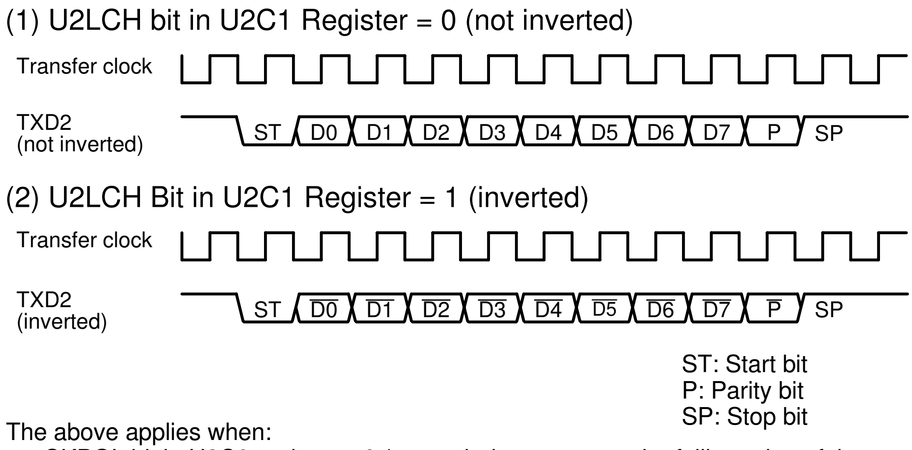
21.3.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data present in the U2TB register) by reading the U2RB register. If the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

21.4.4 Serial Data Logic Switching Function

The data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 21.10 shows the Serial Data Logic Switching.

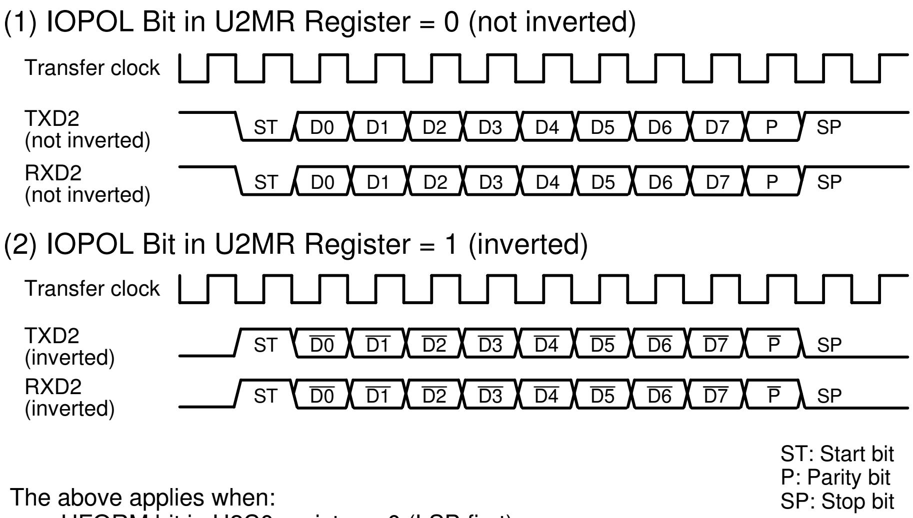


The above applies when:
- CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge of the transfer clock)
- UFORM bit in U2C0 register = 0 (LSB first)
- STPS bit in U2MR register = 0 (one stop bit)
- PRYE bit in U2MR register = 1 (parity enabled)

Figure 21.10 Serial Data Logic Switching

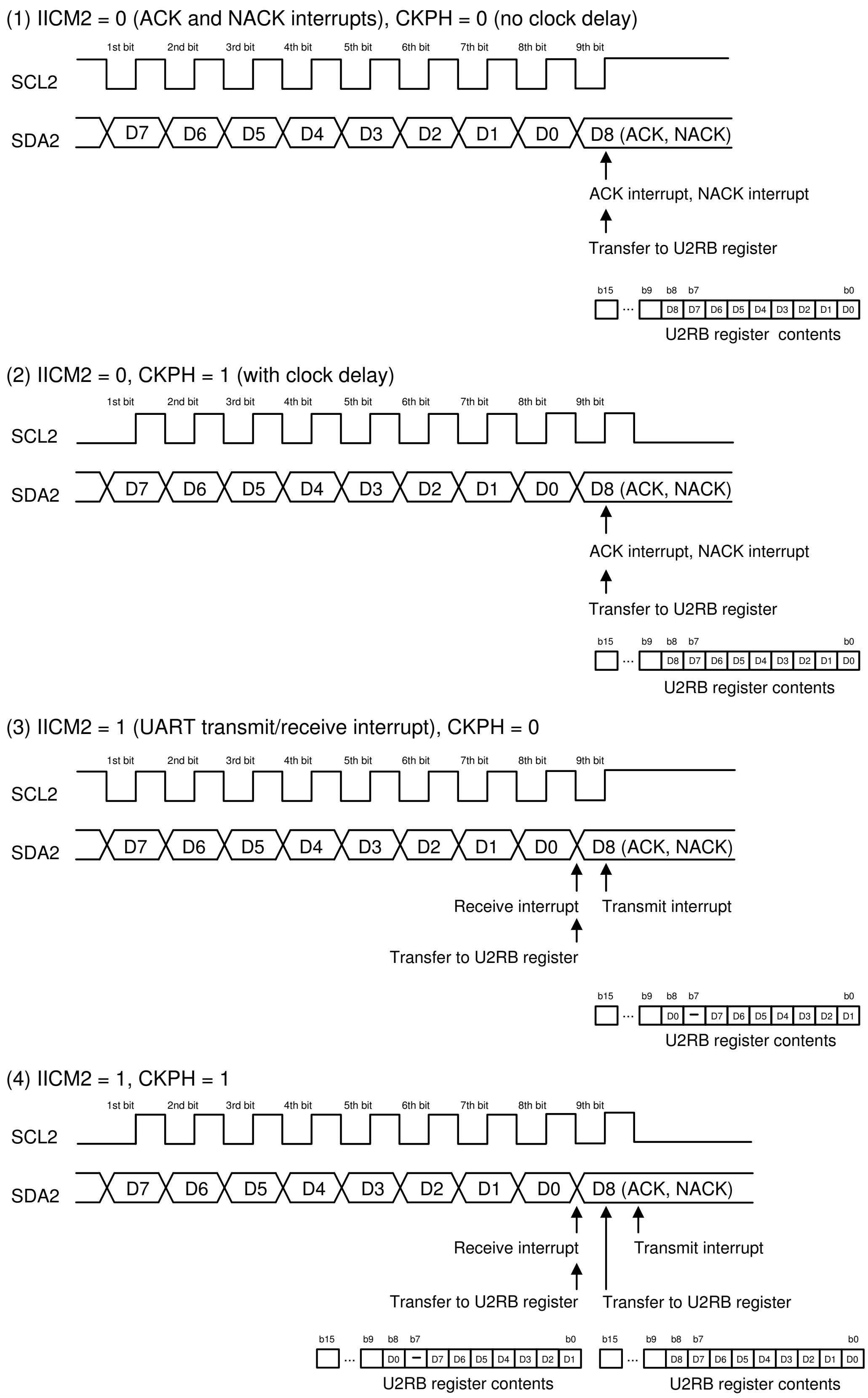
21.4.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 21.11 shows the TXD and RXD I/O Inversion.



The above applies when:
- UFORM bit in U2C0 register = 0 (LSB first)
- STPS bit in U2MR register = 0 (one stop bit)
- PRYE bit in U2MR register = 1 (parity enabled)

Figure 21.11 TXD and RXD I/O Inversion



The above applies when:
- CKDIR bit in U2MR register = 0 (master selected)

Figure 21.14 Transfer to U2RB Register and Interrupt Timing

21.5.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.
Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.
Figure 21.15 shows the Detection of Start and Stop Conditions.

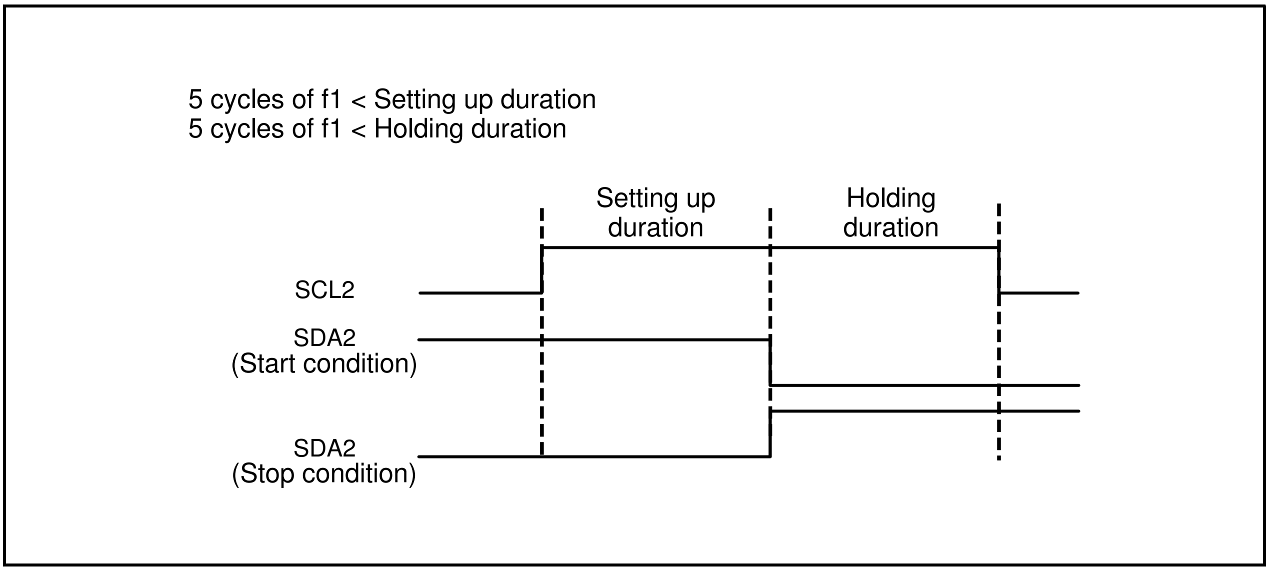


Figure 21.15 Detection of Start and Stop Conditions

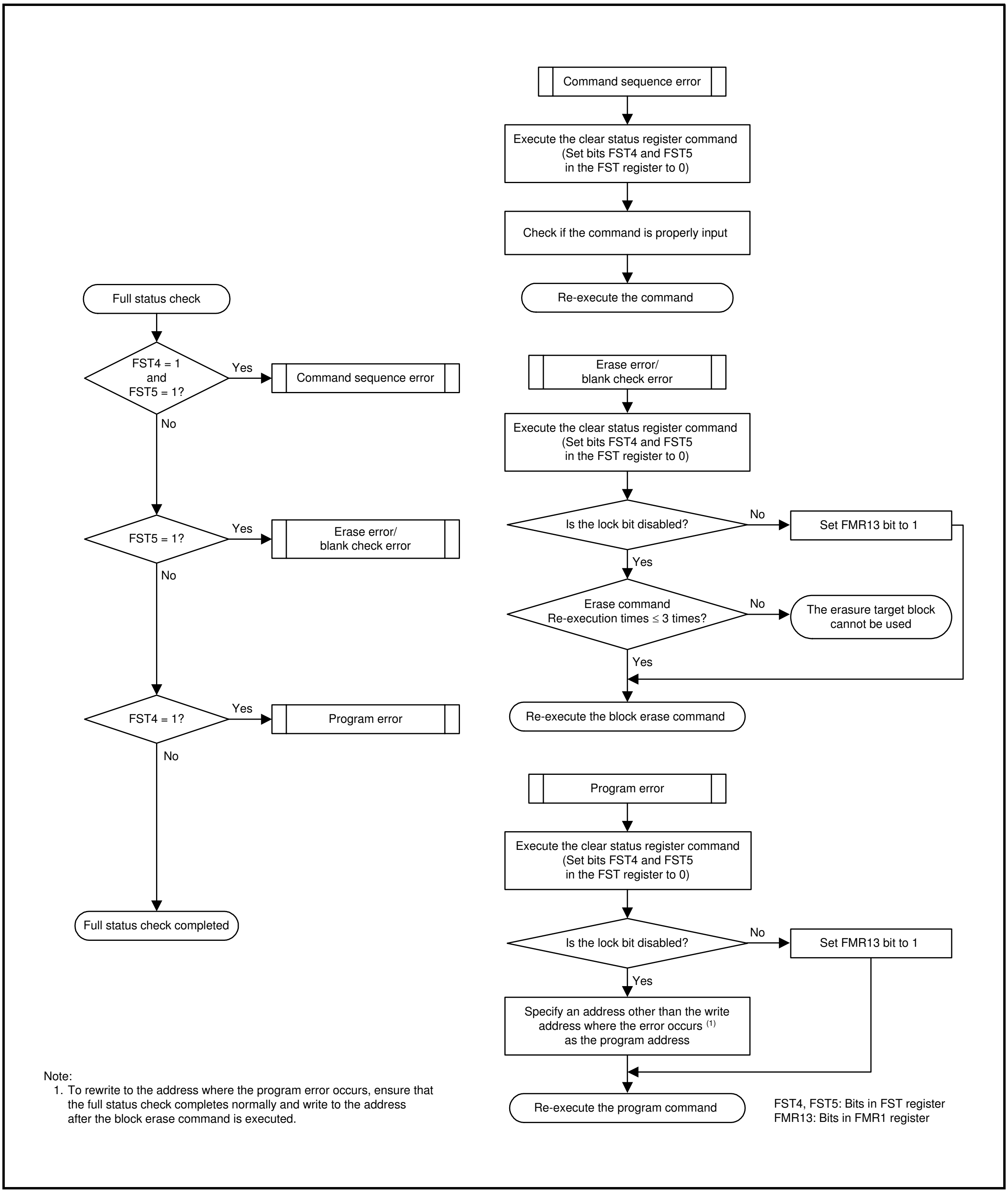


Figure 24.15 Full Status Check and Handling Procedure for Individual Errors

Table 26.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.15	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.15	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.75	–	–	µs
IV_{ref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
V_{ref}	Reference voltage				2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 26.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	–	V_{CC} – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	–	V_{CC} + 0.3	V
–	Offset		–	5	100	mV
td	Comparator output delay time (2)	V_I = Vref ± 100 mV	–	0.1	–	µs
I_{CMP}	Comparator operating current	V_{CC} = 5.0 V	–	17.5	–	µA

Notes:
1. V_{CC} = 2.7 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. When the digital filter is disabled.

27.8.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

• Using an interrupt
Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

• Monitoring with a program 1
Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

• Monitoring with a program 2
(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

• Using read results if they are the same value twice
(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.
Also, when reading several registers, read them as continuously as possible.