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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atuc256l4u-aut

1. Description

The Atmel® AVR® ATUC64/128/256L3/4U is a complete system-on-chip microcontroller based on the AVR32 UC RISC processor running at frequencies up to 50MHz. AVR32 UC is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density, and high performance.

The processor implements a Memory Protection Unit (MPU) and a fast and flexible interrupt controller for supporting modern and real-time operating systems. The Secure Access Unit (SAU) is used together with the MPU to provide the required security and integrity.

Higher computation capability is achieved using a rich set of DSP instructions.

The ATUC64/128/256L3/4U embeds state-of-the-art picoPower technology for ultra-low power consumption. Combined power control techniques are used to bring active current consumption down to 174µA/MHz, and leakage down to 220nA while still retaining a bank of backup registers. The device allows a wide range of trade-offs between functionality and power consumption, giving the user the ability to reach the lowest possible power consumption with the feature set required for the application.

The Peripheral Direct Memory Access (DMA) controller enables data transfers between peripherals and memories without processor involvement. The Peripheral DMA controller drastically reduces processing overhead when transferring continuous and large data streams.

The ATUC64/128/256L3/4U incorporates on-chip Flash and SRAM memories for secure and fast access. The FlashVault technology allows secure libraries to be programmed into the device. The secure libraries can be executed while the CPU is in Secure State, but not read by non-secure software in the device. The device can thus be shipped to end customers, who will be able to program their own code into the device to access the secure libraries, but without risk of compromising the proprietary secure code.

The External Interrupt Controller (EIC) allows pins to be configured as external interrupts. Each external interrupt has its own interrupt request and can be individually masked.

The Peripheral Event System allows peripherals to receive, react to, and send peripheral events without CPU intervention. Asynchronous interrupts allow advanced peripheral operation in low power sleep modes.

The Power Manager (PM) improves design flexibility and security. The Power Manager supports SleepWalking functionality, by which a module can be selectively activated based on peripheral events, even in sleep modes where the module clock is stopped. Power monitoring is supported by on-chip Power-on Reset (POR), Brown-out Detector (BOD), and Supply Monitor (SM). The device features several oscillators, such as Phase Locked Loop (PLL), Digital Frequency Locked Loop (DFLL), Oscillator 0 (OSC0), and system RC oscillator (RCSYS). Either of these oscillators can be used as source for the system clock. The DFLL is a programmable internal oscillator from 20 to 150MHz. It can be tuned to a high accuracy if an accurate reference clock is running, e.g. the 32KHz crystal oscillator.

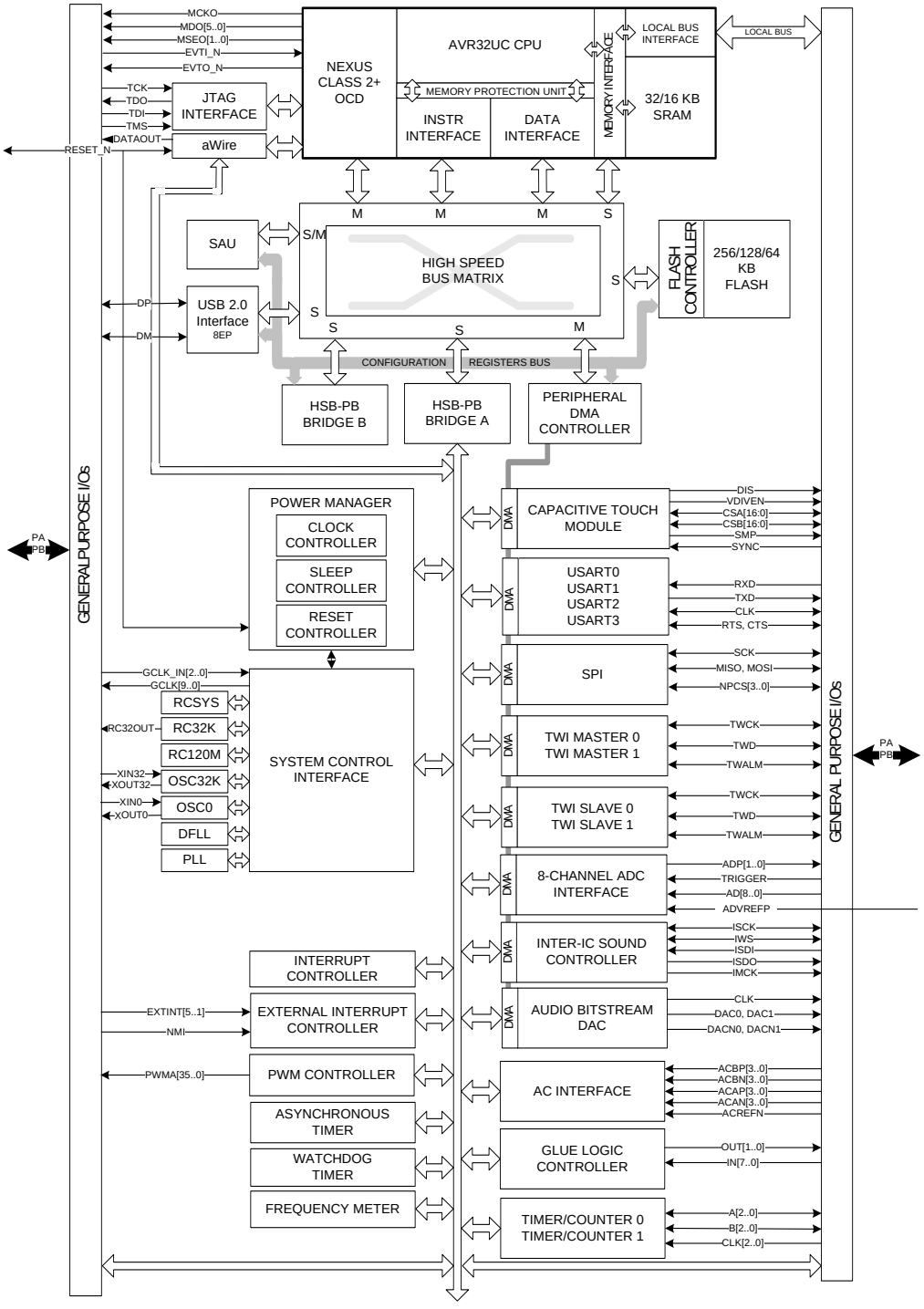
The Watchdog Timer (WDT) will reset the device unless it is periodically serviced by the software. This allows the device to recover from a condition that has caused the system to be unstable.

The Asynchronous Timer (AST) combined with the 32KHz crystal oscillator supports powerful real-time clock capabilities, with a maximum timeout of up to 136 years. The AST can operate in counter or calendar mode.

2. Overview

2.1 Block Diagram

Figure 2-1. Block Diagram

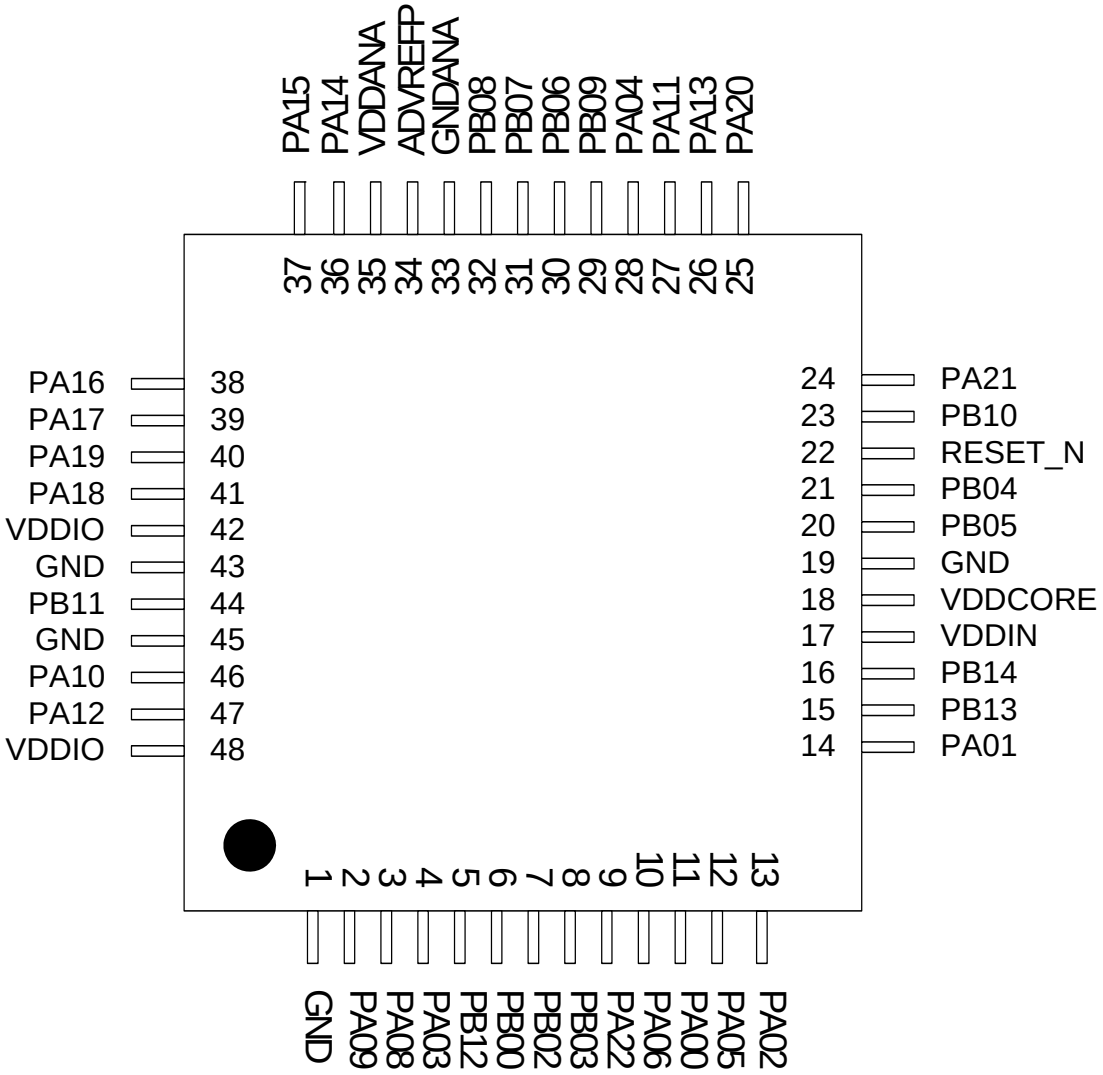


2.2 Configuration Summary

Table 2-1. Configuration Summary

Feature	ATUC256L3U	ATUC128L3U	ATUC64L3U	ATUC256L4U	ATUC128L4U	ATUC64L4U
Flash	256KB	128KB	64KB	256KB	128KB	64KB
SRAM	32KB		16KB	32KB		16KB
GPIO	51			36		
High-drive pins	6			4		
External Interrupts	6					
TWI	2					
USART	4					
Peripheral DMA Channels	12					
Peripheral Event System	1					
SPI	1					
Asynchronous Timers	1					
Timer/Counter Channels	6					
PWM channels	36					
Frequency Meter	1					
Watchdog Timer	1					
Power Manager	1					
Secure Access Unit	1					
Glue Logic Controller	1					
Oscillators	Digital Frequency Locked Loop 20-150MHz (DFLL) Phase Locked Loop 40-240MHz (PLL) Crystal Oscillator 0.45-16MHz (OSC0) Crystal Oscillator 32KHz (OSC32K) RC Oscillator 120MHz (RC120M) RC Oscillator 115kHz (RCSYS) RC Oscillator 32kHz (RC32K)					
ADC	8-channel 12-bit					
Temperature Sensor	1					
Analog Comparators	8					
Capacitive Touch Module	1					
JTAG	1					
aWire	1					
USB	1					
Audio Bitstream DAC	1			0		
IIS Controller	1			0		
Max Frequency	50MHz					
Packages	TQFP64/QFN64			TQFP48/QFN48/TLLGA48		

Figure 3-2. ATUC64/128/256L4U TLLGA48 Pinout



Peripheral Multiplexing on I/O lines

3.1.1 Multiplexed Signals

Each GPIO line can be assigned to one of the peripheral functions. The following table describes the peripheral signals multiplexed to the GPIO lines.

Table 3-1. GPIO Controller Function Multiplexing

48-pin	64-pin	Pin Name	GPIO	Supply	Pad Type	GPIO Function							
						A	B	C	D	E	F	G	H
11	15	PA00	0	VDDIO	Normal I/O	USART0-TXD	USART1-RTS	SPI-NPCS[2]		PWMA-PWMA[0]		SCIF-GCLK[0]	CAT-CSA[2]
14	18	PA01	1	VDDIO	Normal I/O	USART0-RXD	USART1-CTS	SPI-NPCS[3]	USART1-CLK	PWMA-PWMA[1]	ACIFB-ACAP[0]	TWIMS0-TWALM	CAT-CSA[1]
13	17	PA02	2	VDDIO	High-drive I/O	USART0-RTS	ADCIFB-TRIGGER	USART2-TXD	TC0-A0	PWMA-PWMA[2]	ACIFB-ACBP[0]	USART0-CLK	CAT-CSA[3]
4	6	PA03	3	VDDIO	Normal I/O	USART0-CTS	SPI-NPCS[1]	USART2-TXD	TC0-B0	PWMA-PWMA[3]	ACIFB-ACBN[3]	USART0-CLK	CAT-CSB[3]
28	38	PA04	4	VDDIO	Normal I/O	SPI-MISO	TWIMS0-TWCK	USART1-RXD	TC0-B1	PWMA-PWMA[4]	ACIFB-ACBP[1]		CAT-CSA[7]
12	16	PA05	5	VDDIO	Normal I/O (TWI)	SPI-MOSI	TWIMS1-TWCK	USART1-TXD	TC0-A1	PWMA-PWMA[5]	ACIFB-ACBN[0]	TWIMS0-TWD	CAT-CSB[7]
10	14	PA06	6	VDDIO	High-drive I/O, 5V tolerant	SPI-SCK	USART2-TXD	USART1-CLK	TC0-B0	PWMA-PWMA[6]	EIC-EXTINT[2]	SCIF-GCLK[1]	CAT-CSB[1]
	19	PA07	7	VDDIO	Normal I/O (TWI)	SPI-NPCS[0]	USART2-RXD	TWIMS1-TWALM	TWIMS0-TWCK	PWMA-PWMA[7]	ACIFB-ACAN[0]	EIC-NMI (EXTINT[0])	CAT-CSB[2]
3	3	PA08	8	VDDIO	High-drive I/O	USART1-TXD	SPI-NPCS[2]	TC0-A2	ADCIFB-ADP[0]	PWMA-PWMA[8]			CAT-CSA[4]
2	2	PA09	9	VDDIO	High-drive I/O	USART1-RXD	SPI-NPCS[3]	TC0-B2	ADCIFB-ADP[1]	PWMA-PWMA[9]	SCIF-GCLK[2]	EIC-EXTINT[1]	CAT-CSB[4]
46	62	PA10	10	VDDIO	Normal I/O	TWIMS0-TWD		TC0-A0		PWMA-PWMA[10]	ACIFB-ACAP[1]	SCIF-GCLK[2]	CAT-CSA[5]
27	35	PA11	11	VDDIN	Normal I/O					PWMA-PWMA[11]			
47	63	PA12	12	VDDIO	Normal I/O		USART2-CLK	TC0-CLK1	CAT-SMP	PWMA-PWMA[12]	ACIFB-ACAN[1]	SCIF-GCLK[3]	CAT-CSB[5]
26	34	PA13	13	VDDIN	Normal I/O	GLOC-OUT[0]	GLOC-IN[7]	TC0-A0	SCIF-GCLK[2]	PWMA-PWMA[13]	CAT-SMP	EIC-EXTINT[2]	CAT-CSA[0]
36	48	PA14	14	VDDIO	Normal I/O	ADCIFB-AD[0]	TC0-CLK2	USART2-RTS	CAT-SMP	PWMA-PWMA[14]		SCIF-GCLK[4]	CAT-CSA[6]
37	49	PA15	15	VDDIO	Normal I/O	ADCIFB-AD[1]	TC0-CLK1		GLOC-IN[6]	PWMA-PWMA[15]	CAT-SYNC	EIC-EXTINT[3]	CAT-CSB[6]
38	50	PA16	16	VDDIO	Normal I/O	ADCIFB-AD[2]	TC0-CLK0		GLOC-IN[5]	PWMA-PWMA[16]	ACIFB-ACREFN	EIC-EXTINT[4]	CAT-CSA[8]

Table 3-1. GPIO Controller Function Multiplexing

39	51	PA17	17	VDDIO	Normal I/O (TWI)		TC0-A1	USART2-CTS	TWIMS1-TWD	PWMA-PWMA[17]	CAT-SMP	CAT-DIS	CAT-CSB[8]
41	53	PA18	18	VDDIO	Normal I/O	ADCIFB-AD[4]	TC0-B1		GLOC-IN[4]	PWMA-PWMA[18]	CAT-SYNC	EIC-EXTINT[5]	CAT-CSB[0]
40	52	PA19	19	VDDIO	Normal I/O	ADCIFB-AD[5]		TC0-A2	TWIMS1-TWALM	PWMA-PWMA[19]	SCIF-GCLK_IN[0]	CAT-SYNC	CAT-CSA[10]
25	33	PA20	20	VDDIN	Normal I/O	USART2-TXD		TC0-A1	GLOC-IN[3]	PWMA-PWMA[20]	SCIF-RC32OUT		CAT-CSA[12]
24	32	PA21	21	VDDIN	Normal I/O (TWI, 5V tolerant, SMBus)	USART2-RXD	TWIMS0-TWD	TC0-B1	ADCIFB-TRIGGER	PWMA-PWMA[21]	PWMA-PWMAOD[21]	SCIF-GCLK[0]	CAT-SMP
9	13	PA22	22	VDDIO	Normal I/O	USART0-CTS	USART2-CLK	TC0-B2	CAT-SMP	PWMA-PWMA[22]	ACIFB-ACBN[2]		CAT-CSB[10]
6	8	PB00	32	VDDIO	Normal I/O	USART3-TXD	ADCIFB-ADP[0]	SPI-NPCS[0]	TC0-A1	PWMA-PWMA[23]	ACIFB-ACAP[2]	TC1-A0	CAT-CSA[9]
	20	PB01	33	VDDIO	High-drive I/O	USART3-RXD	ADCIFB-ADP[1]	SPI-SCK	TC0-B1	PWMA-PWMA[24]		TC1-A1	CAT-CSB[9]
7	9	PB02	34	VDDIO	Normal I/O	USART3-RTS	USART3-CLK	SPI-MISO	TC0-A2	PWMA-PWMA[25]	ACIFB-ACAN[2]	SCIF-GCLK[1]	CAT-CSB[11]
8	10	PB03	35	VDDIO	Normal I/O	USART3-CTS	USART3-CLK	SPI-MOSI	TC0-B2	PWMA-PWMA[26]	ACIFB-ACBP[2]	TC1-A2	CAT-CSA[11]
21	29	PB04	36	VDDIN	Normal I/O (TWI, 5V tolerant, SMBus)	TC1-A0	USART1-RTS	USART1-CLK	TWIMS0-TWALM	PWMA-PWMA[27]	PWMA-PWMAOD[27]	TWIMS1-TWCK	CAT-CSA[14]
20	28	PB05	37	VDDIN	Normal I/O (TWI, 5V tolerant, SMBus)	TC1-B0	USART1-CTS	USART1-CLK	TWIMS0-TWCK	PWMA-PWMA[28]	PWMA-PWMAOD[28]	SCIF-GCLK[3]	CAT-CSB[14]
30	42	PB06	38	VDDIO	Normal I/O	TC1-A1	USART3-TXD	ADCIFB-AD[6]	GLOC-IN[2]	PWMA-PWMA[29]	ACIFB-ACAN[3]	EIC-NMI (EXTINT[0])	CAT-CSB[13]
31	43	PB07	39	VDDIO	Normal I/O	TC1-B1	USART3-RXD	ADCIFB-AD[7]	GLOC-IN[1]	PWMA-PWMA[30]	ACIFB-ACAP[3]	EIC-EXTINT[1]	CAT-CSA[13]
32	44	PB08	40	VDDIO	Normal I/O	TC1-A2	USART3-RTS	ADCIFB-AD[8]	GLOC-IN[0]	PWMA-PWMA[31]	CAT-SYNC	EIC-EXTINT[2]	CAT-CSB[12]
29	39	PB09	41	VDDIO	Normal I/O	TC1-B2	USART3-CTS	USART3-CLK		PWMA-PWMA[32]	ACIFB-ACBN[1]	EIC-EXTINT[3]	CAT-CSB[15]
23	31	PB10	42	VDDIN	Normal I/O	TC1-CLK0	USART1-TXD	USART3-CLK	GLOC-OUT[1]	PWMA-PWMA[33]	SCIF-GCLK_IN[1]	EIC-EXTINT[4]	CAT-CSB[16]
44	56	PB11	43	VDDIO	Normal I/O	TC1-CLK1	USART1-RXD		ADCIFB-TRIGGER	PWMA-PWMA[34]	CAT-VDIVEN	EIC-EXTINT[5]	CAT-CSA[16]
5	7	PB12	44	VDDIO	Normal I/O	TC1-CLK2		TWIMS1-TWALM	CAT-SYNC	PWMA-PWMA[35]	ACIFB-ACBP[3]	SCIF-GCLK[4]	CAT-CSA[15]
15	22	PB13	45	VDDIN	USB I/O	USBC-DM	USART3-TXD		TC1-A1	PWMA-PWMA[7]	ADCIFB-ADP[1]	SCIF-GCLK[5]	CAT-CSB[2]
16	23	PB14	46	VDDIN	USB I/O	USBC-DP	USART3-RXD		TC1-B1	PWMA-PWMA[24]		SCIF-GCLK[5]	CAT-CSB[9]

Table 3-4. Nexus OCD AUX Port Connections

Pin	AXS=1	AXS=0
EVTO_N	PA04	PA04
MCKO	PA06	PB01
MSEO[1]	PA07	PB11
MSEO[0]	PA11	PB12

3.2.5 Oscillator Pinout

The oscillators are not mapped to the normal GPIO functions and their muxings are controlled by registers in the System Control Interface (SCIF). Please refer to the SCIF chapter for more information about this.

Table 3-5. Oscillator Pinout

48-pin	64-pin	Pin Name	Oscillator Pin
3	3	PA08	XIN0
46	62	PA10	XIN32
26	34	PA13	XIN32_2
2	2	PA09	XOUT0
47	63	PA12	XOUT32
25	33	PA20	XOUT32_2

3.2.6 Other Functions

The functions listed in Table 3-6 are not mapped to the normal GPIO functions. The aWire DATA pin will only be active after the aWire is enabled. The aWire DATAOUT pin will only be active after the aWire is enabled and the 2_PIN_MODE command has been sent. The WAKE_N pin is always enabled. Please refer to Section 6.1.4.2 on page 45 for constraints on the WAKE_N pin.

Table 3-6. Other Functions

48-pin	64-pin	Pin Name	Function
27	35	PA11	WAKE_N
22	30	RESET_N	aWire DATA
11	15	PA00	aWire DATAOUT

Table 3-7. Signal Descriptions List

B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWIMS0, TWIMS1				
TWALM	SMBus SMBALERT	I/O	Low	
TWCK	Two-wire Serial Clock	I/O		
TWD	Two-wire Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input	Low	
RTS	Request To Send	Output	Low	
RXD	Receive Data	Input		
TXD	Transmit Data	Output		

Note: 1. ADCIFB: AD3 does not exist.

Table 3-8. Signal Description List, Continued

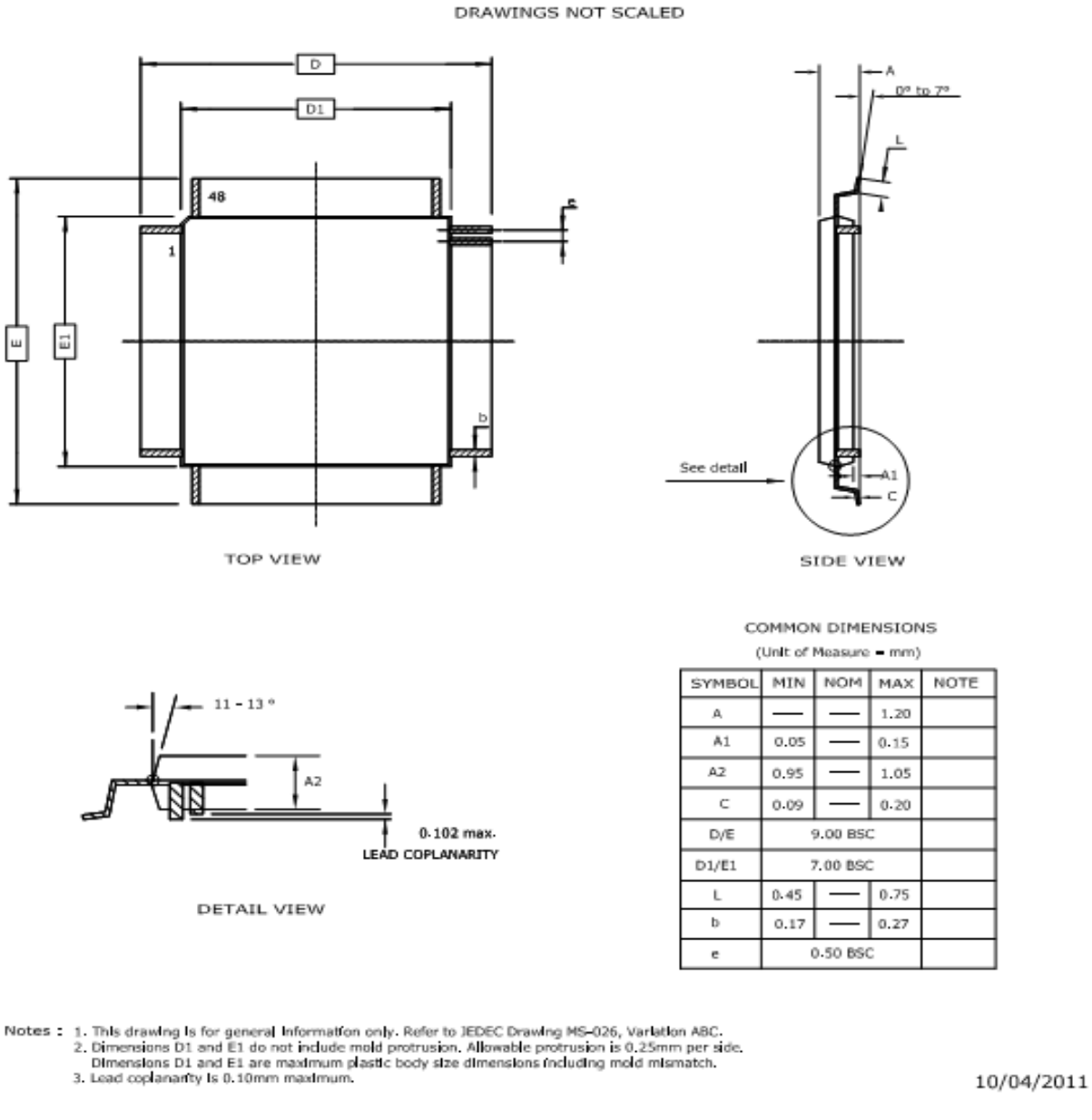
Signal Name	Function	Type	Active Level	Comments
Power				
VDDCORE	Core Power Supply / Voltage Regulator Output	Power Input/Output		1.62V to 1.98V
VDDIO	I/O Power Supply	Power Input		1.62V to 3.6V. VDDIO should always be equal to or lower than VDDIN.
VDDANA	Analog Power Supply	Power Input		1.62V to 1.98V
ADVREFP	Analog Reference Voltage	Power Input		1.62V to 1.98V
VDDIN	Voltage Regulator Input	Power Input		1.62V to 3.6V[1]
GNDANA	Analog Ground	Ground		
GND	Ground	Ground		
Auxiliary Port - AUX				
MCKO	Trace Data Output Clock	Output		
MDO5 - MDO0	Trace Data Output	Output		

3.4.10 ADC Input Pins

These pins are regular I/O pins powered from the VDDIO. However, when these pins are used for ADC inputs, the voltage applied to the pin must not exceed 1.98V. Internal circuitry ensures that the pin cannot be used as an analog input pin when the I/O drives to VDD. When the pins are not used for ADC inputs, the pins may be driven to the full I/O voltage range.

4.2 Package Drawings

Figure 4-1. TQFP-48 Package Drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	—	1.05	
C	0.09	—	0.20	
D/E		9.00 BSC		
D1/E1		7.00 BSC		
L	0.45	—	0.75	
b	0.17	—	0.27	
e		0.50 BSC		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

Table 4-2. Device and Package Maximum Weight

140	mg

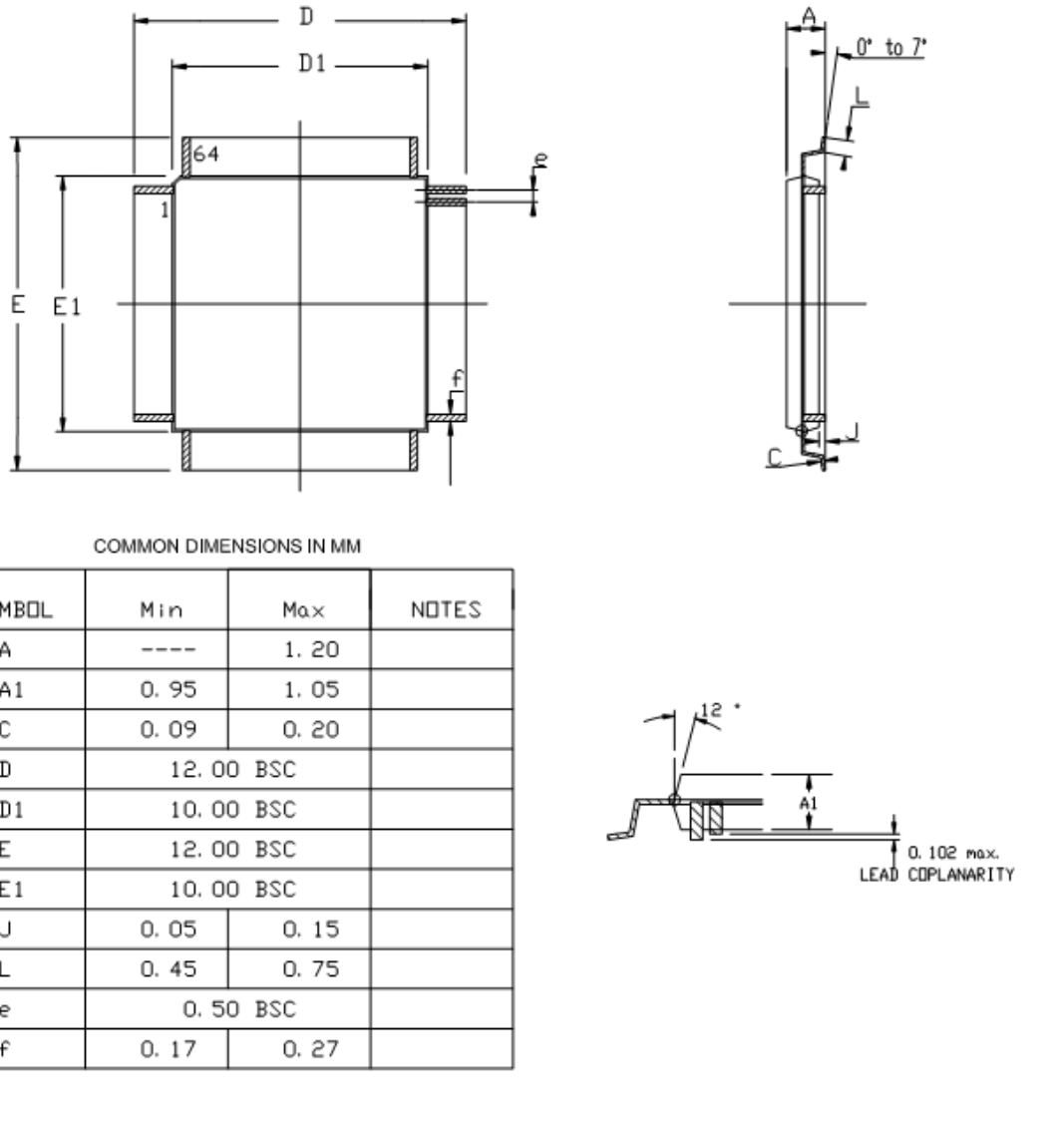
Table 4-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 4-4. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 4-4. TQFP-64 Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

Table 4-11. Device and Package Maximum Weight

300	mg

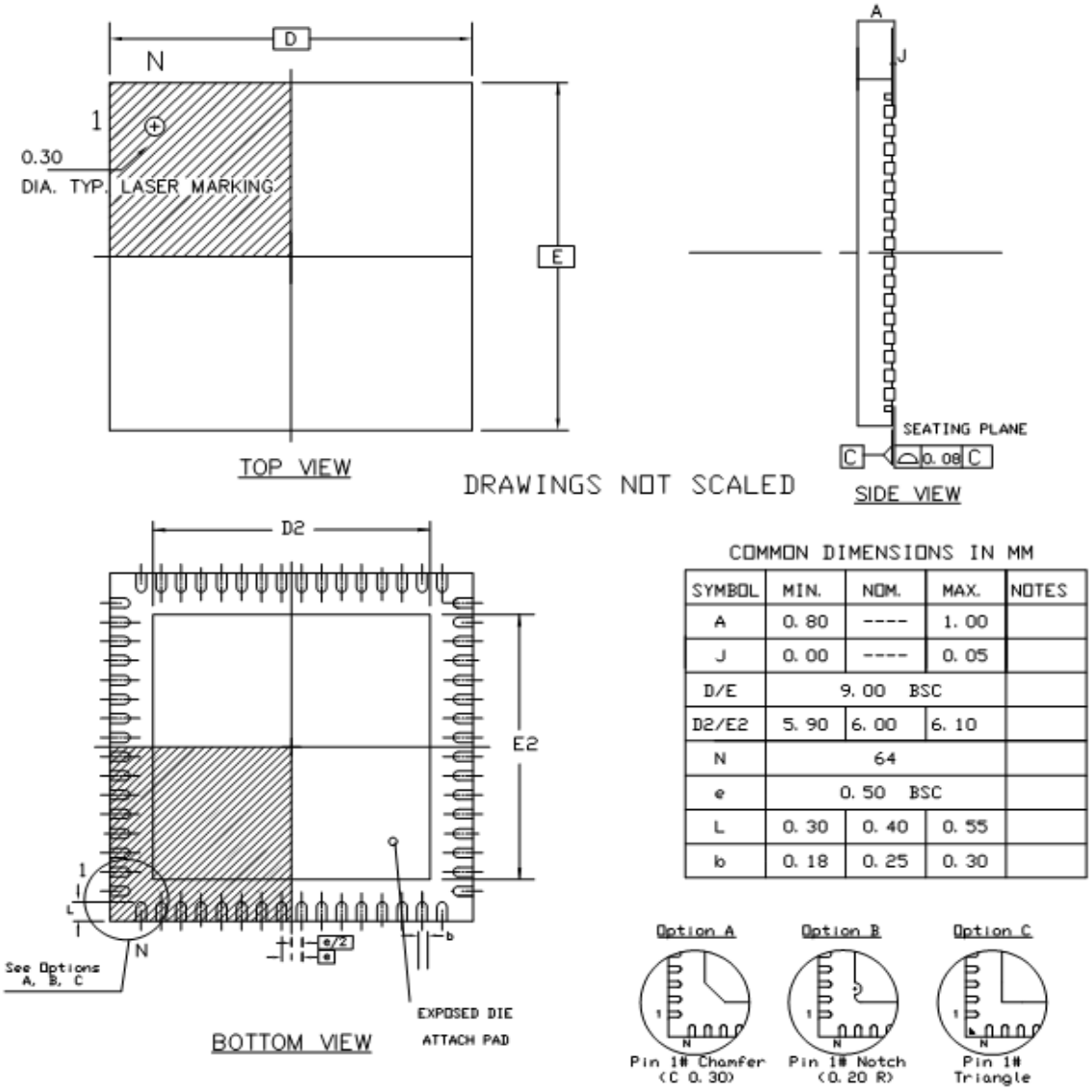
Table 4-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 4-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 4-5. QFN-64 Package Drawing



SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E		9.00 BSC		
D2/E2	5.90	6.00	6.10	
N		64		
e		0.50 BSC		
L	0.30	0.40	0.55	
b	0.18	0.25	0.30	

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 4-14. Device and Package Maximum Weight

200	mg

Table 4-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 4-16. Package Reference

JEDEC Drawing Reference	M0-220
JESD97 Classification	E3

4. **SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0**
   When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
   Fix/Workaround
   When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

5. **SPI mode fault detection enable causes incorrect behavior**
   When mode fault detection is enabled (MR.MODFDIS==0), the SPI module may not operate properly.
   Fix/Workaround
   Always disable mode fault detection before using the SPI by writing a one to MR.MODFDIS.

6. **SPI RDR.PCS is not correct**
   The PCS (Peripheral Chip Select) field in the SPI RDR (Receive Data Register) does not correctly indicate the value on the NPCS pins at the end of a transfer.
   Fix/Workaround
   Do not use the PCS field of the SPI RDR.

6.1.3 TWI

1. **SMBALERT bit may be set after reset**
   The SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.
   Fix/Workaround
   After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

2. **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**
   When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
   Fix/Workaround
   Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

6.1.4 TC

1. **Channel chaining skips first pulse for upper channel**
   When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.
   Fix/Workaround
   Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

6.1.5 CAT

1. **CAT QMatrix sense capacitors discharged prematurely**
   At the end of a QMatrix burst charging sequence that uses different burst count values for different Y lines, the Y lines may be incorrectly grounded for up to n-1 periods of the periph-

eral bus clock, where n is the ratio of the PB clock frequency to the GCLK_CAT frequency. This results in premature loss of charge from the sense capacitors and thus increased variability of the acquired count values.

Fix/Workaround

Enable the 1 kOhm drive resistors on all implemented QMatrix Y lines (CSA 1, 3, 5, 7, 9, 11, 13, and/or 15) by writing ones to the corresponding odd bits of the CSARES register.

2. **Autonomous CAT acquisition must be longer than AST source clock period**

When using the AST to trigger CAT autonomous touch acquisition in sleep modes where the CAT bus clock is turned off, the CAT will start several acquisitions if the period of the AST source clock is larger than one CAT acquisition. One AST clock period after the AST trigger, the CAT clock will automatically stop and the CAT acquisition can be stopped prematurely, ruining the result.

Fix/Workaround

Always ensure that the ATCFG1.max field is set so that the duration of the autonomous touch acquisition is greater than one clock period of the AST source clock.

6.1.6 aWire

1. **aWire MEMORY_SPEED_REQUEST command does not return correct CV**

The aWire MEMORY_SPEED_REQUEST command does not return a CV corresponding to the formula in the aWire Debug Interface chapter.

Fix/Workaround

Issue a dummy read to address 0x100000000 before issuing the MEMORY_SPEED_REQUEST command and use this formula instead:

$$f_{sab} = \frac{7 f_{aw}}{CV - 3}$$

6.1.7 Flash

1. **Corrupted data in flash may happen after flash page write operations**

After a flash page write operation from an external in situ programmer, reading (data read or code fetch) in flash may fail. This may lead to an exception or to others errors derived from this corrupted read access.

Fix/Workaround

Before any flash page write operation, each write in the page buffer must preceded by a write in the page buffer with 0xFFFF_FFFF content at any address in the page.

6.2 Rev. B

6.2.1 SCIF

1. **The RC32K output on PA20 is not always permanently disabled**

The RC32K output on PA20 may sometimes re-appear.

Fix/Workaround

Before using RC32K for other purposes, the following procedure has to be followed in order to properly disable it:

- Run the CPU on RCSYS
- Disable the output to PA20 by writing a zero to PM.PPCR.RC32OUT
- Enable RC32K by writing a one to SCIF.RC32KCR.EN, and wait for this bit to be read as one

Under certain circumstances, the lock signal from the Phase Locked Loop (PLL) oscillator may not go back to zero after the PLL oscillator has been disabled. This can cause the propagation of clock signals with the wrong frequency to parts of the system that use the PLL clock.

Fix/Workaround

PLL must be turned off before entering STOP, DEEPSTOP or STATIC sleep modes. If PLL has been turned off, a delay of 30us must be observed after the PLL has been enabled again before the SCIF.PLL0LOCK bit can be used as a valid indication that the PLL is locked.

3. **PLLCOUNT value larger than zero can cause PLLEN glitch**

   Initializing the PLLCOUNT with a value greater than zero creates a glitch on the PLLEN signal during asynchronous wake up.

   Fix/Workaround

   The lock-masking mechanism for the PLL should not be used.
   The PLLCOUNT field of the PLL Control Register should always be written to zero.

4. **RCSYS is not calibrated**

   The RCSYS is not calibrated and will run faster than 115.2kHz. Frequencies around 150kHz can be expected.

   Fix/Workaround

   If a known clock source is available the RCSYS can be runtime calibrated by using the frequency meter (FREQM) and tuning the RCSYS by writing to the RCCR register in SCIF.

5. **Writing 0x5A5A5A5A to the SCIF memory range will enable the SCIF UNLOCK feature**

   The SCIF UNLOCK feature will be enabled if the value 0x5A5A5A5A is written to any location in the SCIF memory range.

   Fix/Workaround

   None.

6.3.4 WDT

1. **Clearing the Watchdog Timer (WDT) counter in second half of timeout period will issue a Watchdog reset**

   If the WDT counter is cleared in the second half of the timeout period, the WDT will immediately issue a Watchdog reset.

   Fix/Workaround

   Use twice as long timeout period as needed and clear the WDT counter within the first half of the timeout period. If the WDT counter is cleared after the first half of the timeout period, you will get a Watchdog reset immediately. If the WDT counter is not cleared at all, the time before the reset will be twice as long as needed.

2. **WDT Control Register does not have synchronization feedback**

   When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fieldss of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clcok domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.

   Fix/Workaround

   -When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.
   -When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

6.3.7 TWI

1. **TWIS may not wake the device from sleep mode**
   If the CPU is put to a sleep mode (except Idle and Frozen) directly after a TWI Start condition, the CPU may not wake upon a TWIS address match. The request is NACKed.
   Fix/Workaround
   When using the TWI address match to wake the device from sleep, do not switch to sleep modes deeper than Frozen. Another solution is to enable asynchronous EIC wake on the TWIS clock (TWCK) or TWIS data (TWD) pins, in order to wake the system up on bus events.

2. **SMBALERT bit may be set after reset**
   The SMBus Alert (SMBALERT) bit in the Status Register (SR) might be erroneously set after system reset.
   Fix/Workaround
   After system reset, clear the SR.SMBALERT bit before commencing any TWI transfer.

3. **Clearing the NAK bit before the BTF bit is set locks up the TWI bus**
   When the TWIS is in transmit mode, clearing the NAK Received (NAK) bit of the Status Register (SR) before the end of the Acknowledge/Not Acknowledge cycle will cause the TWIS to attempt to continue transmitting data, thus locking up the bus.
   Fix/Workaround
   Clear SR.NAK only after the Byte Transfer Finished (BTF) bit of the same register has been set.

4. **TWIS stretch on Address match error**
   When the TWIS stretches TWCK due to a slave address match, it also holds TWD low for the same duration if it is to be receiving data. When TWIS releases TWCK, it releases TWD at the same time. This can cause a TWI timing violation.
   Fix/Workaround
   None.

5. **TWIM TWALM polarity is wrong**
   The TWALM signal in the TWIM is active high instead of active low.
   Fix/Workaround
   Use an external inverter to invert the signal going into the TWIM. When using both TWIM and TWIS on the same pins, the TWALM cannot be used.

6.3.8 PWMA

1. **The SR.READY bit cannot be cleared by writing to SCR.READY**
   The Ready bit in the Status Register will not be cleared when writing a one to the corresponding bit in the Status Clear register. The Ready bit will be cleared when the Busy bit is set.
   Fix/Workaround
   Disable the Ready interrupt in the interrupt handler when receiving the interrupt. When an operation that triggers the Busy/Ready bit is started, wait until the ready bit is low in the Status Register before enabling the interrupt.

6.3.9 TC

1. **Channel chaining skips first pulse for upper channel**
   When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.

Fix/Workaround
Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

6.3.10 ADCIFB

1. **ADCIFB DMA transfer does not work with divided PBA clock**
DMA requests from the ADCIFB will not be performed when the PBA clock is slower than the HSB clock.
Fix/Workaround
Do not use divided PBA clock when the PDCA transfers from the ADCIFB.

6.3.11 CAT

1. **CAT QMatrix sense capacitors discharged prematurely**
At the end of a QMatrix burst charging sequence that uses different burst count values for different Y lines, the Y lines may be incorrectly grounded for up to n-1 periods of the peripheral bus clock, where n is the ratio of the PB clock frequency to the GCLK_CAT frequency. This results in premature loss of charge from the sense capacitors and thus increased variability of the acquired count values.
Fix/Workaround
Enable the 1 kOhm drive resistors on all implemented QMatrix Y lines (CSA 1, 3, 5, 7, 9, 11, 13, and/or 15) by writing ones to the corresponding odd bits of the CSARES register.

2. **Autonomous CAT acquisition must be longer than AST source clock period**
When using the AST to trigger CAT autonomous touch acquisition in sleep modes where the CAT bus clock is turned off, the CAT will start several acquisitions if the period of the AST source clock is larger than one CAT acquisition. One AST clock period after the AST trigger, the CAT clock will automatically stop and the CAT acquisition can be stopped prematurely, ruining the result.
Fix/Workaround
Always ensure that the ATCFG1.max field is set so that the duration of the autonomous touch acquisition is greater than one clock period of the AST source clock.

3. **CAT consumes unnecessary power when disabled or when autonomous touch not used**
A CAT prescaler controlled by the ATCFG0.DIV field will be active even when the CAT module is disabled or when the autonomous touch feature is not used, thereby causing unnecessary power consumption.
Fix/Workaround
If the CAT module is not used, disable the CLK_CAT clock in the PM module. If the CAT module is used but the autonomous touch feature is not used, the power consumption of the CAT module may be reduced by writing 0xFFFF to the ATCFG0.DIV field.

4. **CAT module does not terminate QTouch burst on detect**
The CAT module does not terminate a QTouch burst when the detection voltage is reached on the sense capacitor. This can cause the sense capacitor to be charged more than necessary. Depending on the dielectric absorption characteristics of the capacitor, this can lead to unstable measurements.
Fix/Workaround
Use the minimum possible value for the MAX field in the ATCFG1, TG0CFG1, and TG1CFG1 registers.

6.3.12 aWire

1. **aWire MEMORY_SPEED_REQUEST command does not return correct CV**
   The aWire MEMORY_SPEED_REQUEST command does not return a CV corresponding to the formula in the aWire Debug Interface chapter.
   Fix/Workaround
   Issue a dummy read to address 0x100000000 before issuing the MEMORY_SPEED_REQUEST command and use this formula instead:

$$f_{sab} = \frac{7 f_{aw}}{CV - 3}$$

6.3.13 Flash

1. **Corrupted data in flash may happen after flash page write operations**
   After a flash page write operation from an external in situ programmer, reading (data read or code fetch) in flash may fail. This may lead to an exception or to others errors derived from this corrupted read access.
   Fix/Workaround
   Before any flash page write operation, each write in the page buffer must preceded by a write in the page buffer with 0xFFFF_FFFF content at any address in the page.

6.3.14 I/O Pins

1. **PA05 is not 3.3V tolerant.**
   PA05 should be grounded on the PCB and left unused if VDDIO is above 1.8V.
   Fix/Workaround
   None.

2. **No pull-up on pins that are not bonded**
   PB13 to PB27 are not bonded on UC3L0256/128, but has no pull-up and can cause current consumption on VDDIO/VDDIN if left undriven.
   Fix/Workaround
   Enable pull-ups on PB13 to PB27 by writing 0x0FFFE000 to the PUERS1 register in the GPIO.

3. **PA17 has low ESD tolerance**
   PA17 only tolerates 500V ESD pulses (Human Body Model).
   Fix/Workaround
   Care must be taken during manufacturing and PCB design.

Table of Contents

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