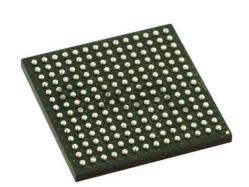
NXP USA Inc. - XC56L307VL150 Datasheet



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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

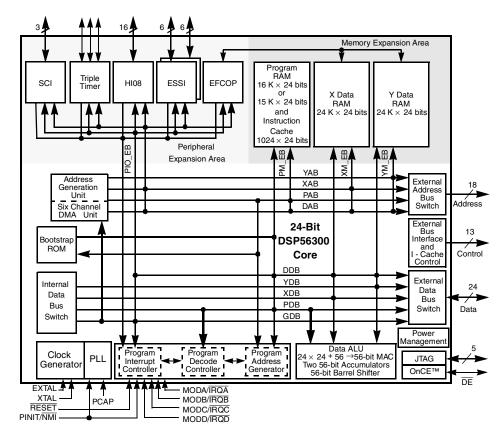
Details	
Product Status	Obsolete
Туре	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	150MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 100°C
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/xc56l307vl150

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

DSP56L307

24-Bit Digital Signal Processor



The DSP56L307 is intended for applications requiring a large amount of internal memory, such as networking and wireless infrastructure applications. The EFCOP can accelerate general filtering applications, such as echo-cancellation applications, correlation, and general-purpose convolutionbased algorithms.

Figure 1. DSP56L307 Block Diagram

The Freescale DSP56L307, a member of the DSP56300 DSP family, supports network applications with general filtering operations. The Enhanced Filter Coprocessor (EFCOP) executes filter algorithms in parallel with core operations, enhancing signal quality with no impact on channel throughput or total channels supported. The result is increased overall performance. Like the other DSP56300 family members, the DSP56L307 uses a high-performance, single-clock-cycle-per- instruction engine (DSP56000 code-compatible), a barrel shifter, 24-bit addressing, an instruction cache, and a direct memory access (DMA) controller (see **Figure 1**). The DSP56L307 performs at 160 million multiply-accumulates per second (MMACS), attaining 320 MMACS when the EFCOP is in use. It operates with an internal 160 MHz clock with a 1.8 volt core and independent 3.3 volt input/output (I/O) power.

Note: This document contains information on a new product. Specifications and information herein are subject to change without notice.



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Features

 Table 1 lists the features of the DSP56L307 device.

S6-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control High-Performance DSP56300 Core Program control unit (PCU) with position-independent code (P(C) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware D0 loops, and fast auto-return interrupts; and trigging from interrupt lines and all peripherals Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination • Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG test access port (TAP) • Internal 24 × 24-bit filtering and echo-cancellation coprocessor that runs in parallel to the DSP core • Operation at the same frequency as the core (up to 160 MHz) • Support for a variety of filter modes, some of which are optimized for cellular base station applications: • Real finite impulse response (FIR) with real taps • Complex FIR generating pure real or pure imaginary outputs alternately • Adaptive FIR filter with complex taps • Direct form 2 (DFII) IIR filter, HIP support, adaptive fIR filter with delayed LMS coefficient updates • Adaptive FIR filter with delayed LMS coefficient updates • Adaptive FIR filter with delayed LMS coefficient updates • Adaptive FIR filter with true least mean square (LMS) coefficient upda	-	 applications) w Object code cc Data arithmetic 56-bit parallel t ALU instruction Program contro DSP applicatio expandable ha Direct memory 	with a 160 MHz clopmpatible with the clogic unit (Data barrel shifter (fasi ns, and 24-bit or ol unit (PCU) with ons (including imm ardware stack, ne	ock at 1.8 V core e DSP56000 core ALU) with fully p t shift and norma 16-bit arithmetic n position-indepen nediate offsets),	and 3.3 V I/O with highly para ipelined 24×24 - lization; bit strear support under so	llel instruction bit parallel mu n generation a	EFCOP ii	Description			
• Operation at the same frequency as the core (up to 160 MHz) • Support for a variety of filter modes, some of which are optimized for cellular base station applications: • Real finite impulse response (FIR) with real taps • Complex FIR generating pure real or pure imaginary outputs alternately • A 4-bit decimation factor in FIR filters, thus providing a decimation ratio up to 16 • Direct form 1 (DFI) Infinite Impulse Response (IIR) filter • Direct form 2 (DFII) IIR filter • Direct form 2 (DFII) IIR filter • Direct form 2 (DFII) IIR filter • Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs • Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allow six-channel home theater) • Serial communications interface (SCI) with baud rate generator • Triple timer module • Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled • 192 × 24-bit Bootstrap ROM • 192 K × 24-bit RAM total		 160 million multiply-accumulates per second (MMACS) (321 MMACS using the EFCOP in filtering applications) with a 160 MHz clock at 1.8 V core and 3.3 V I/O Object code compatible with the DSP56000 core with highly parallel instruction set Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) 									
Internal Peripherals glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs • Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allow six-channel home theater) • Serial communications interface (SCI) with baud rate generator • Triple timer module • Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled • 192 × 24-bit bootstrap ROM • 192 K × 24-bit RAM total		 Operation at the same frequency as the core (up to 160 MHz) Support for a variety of filter modes, some of which are optimized for cellular base station applications: Real finite impulse response (FIR) with real taps Complex FIR with complex taps Complex FIR generating pure real or pure imaginary outputs alternately A 4-bit decimation factor in FIR filters, thus providing a decimation ratio up to 16 Direct form 1 (DFI) Infinite Impulse Response (IIR) filter Direct form 2 (DFII) IIR filter Four scaling factors (1, 4, 8, 16) for IIR output Adaptive FIR filter with true least mean square (LMS) coefficient updates 									
• 192 K × 24-bit RAM total	Internal Peripherals	 glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater) Serial communications interface (SCI) with baud rate generator Triple timer module Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are 									
Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:		 192 × 24-bit bootstrap ROM 192 K × 24-bit RAM total Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable: 									
Program RAM Instruction X Data RAM Y Data RAM Instruction Switch Size Cache Size Size* Size* Cache MSW1 MSW1		Program RAM						MSW1	MSW0		
16 K × 24-bit 0 24 K × 24-bit 24 K × 24-bit disabled 0/1 0/1		•	Cache Size	Size*	3120		disabled	0/1	0/1		
$15 \text{ K} \times 24 \text{-bit} 1024 \times 24 \text{-bit} 24 \text{ K} \times 24 \text{-bit} 24 \text{ K} \times 24 \text{-bit} \text{enabled} \text{disabled} 0/1 0/1$		Size				disabled	diaphlad	0/1	0/1		
$\begin{array}{ c c c c c c c c c } \hline 48 \text{K} \times 24 \text{-bit} & 0 & 8 \text{K} \times 24 \text{-bit} & \text{disabled} & \text{enabled} & 0 & 0 \\ \hline & & & & & & & & & & & & & & & & & &$		Size 16 K × 24-bit 15 K × 24-bit	0 1024 × 24-bit	24 K × 24-bit 24 K × 24-bit	24 K × 24-bit 24 K × 24-bit	enabled		0			
		Size 16 K × 24-bit 15 K × 24-bit 48 K × 24-bit	0 1024 × 24-bit 0	24 K × 24-bit 24 K × 24-bit 8 K × 24-bit	24 K × 24-bit 24 K × 24-bit 8 K × 24-bit	enabled disabled	enabled				
	Internal Memories	Size 16 K × 24-bit 15 K × 24-bit 48 K × 24-bit 47 K × 24-bit	0 $1024 \times 24-bit$ 0 $1024 \times 24-bit$	$\begin{array}{c} 24 \text{ K} \times 24\text{-bit} \\ 24 \text{ K} \times 24\text{-bit} \\ 8 \text{ K} \times 24\text{-bit} \\ 8 \text{ K} \times 24\text{-bit} \end{array}$	$\begin{array}{c} 24 \text{ K} \times 24\text{-bit} \\ 24 \text{ K} \times 24\text{-bit} \\ 8 \text{ K} \times 24\text{-bit} \\ 8 \text{ K} \times 24\text{-bit} \end{array}$	enabled disabled enabled	enabled enabled		0		
	Internal Memories	Size 16 K × 24-bit 15 K × 24-bit 48 K × 24-bit 47 K × 24-bit 40 K × 24-bit	0 $1024 \times 24-bit$ 0 $1024 \times 24-bit$ 0	$\begin{array}{c} 24 \ {\rm K} \times \ 24\ {\rm bit} \\ 24 \ {\rm K} \times \ 24\ {\rm bit} \\ 8 \ {\rm K} \times \ 24\ {\rm bit} \\ 8 \ {\rm K} \times \ 24\ {\rm bit} \\ 12 \ {\rm K} \times \ 24\ {\rm bit} \end{array}$	$\begin{array}{c} 24 \ {\rm K} \times \ 24\ {\rm bit} \\ 24 \ {\rm K} \times \ 24\ {\rm bit} \\ 8 \ {\rm K} \times \ 24\ {\rm bit} \\ 8 \ {\rm K} \times \ 24\ {\rm bit} \\ 12 \ {\rm K} \times \ 24\ {\rm bit} \end{array}$	enabled disabled enabled disabled	enabled enabled enabled	0	0		
	Internal Memories	$\begin{tabular}{ c c c c c c c } \hline Size \\ \hline 16 \ K \times 24 \ bit \\ \hline 15 \ K \times 24 \ bit \\ \hline 48 \ K \times 24 \ bit \\ \hline 47 \ K \times 24 \ bit \\ \hline 40 \ K \times 24 \ bit \\ \hline 39 \ K \times 24 \ bit \\ \hline \end{tabular}$	$0 \\ 1024 \times 24-bit \\ 0 \\ 1024 \times 24-bit \\ 0 \\ 1024 \times 24-bit \\ 1024 \times 24-bit \\ 0 \\ 1024$	24 K × 24-bit 24 K × 24-bit 8 K × 24-bit 8 K × 24-bit 12 K × 24-bit 12 K × 24-bit	$\begin{array}{c} 24 \ {\rm K} \times 24\ {\rm bit} \\ 24 \ {\rm K} \times 24\ {\rm bit} \\ 8 \ {\rm K} \times 24\ {\rm bit} \\ 8 \ {\rm K} \times 24\ {\rm bit} \\ 12 \ {\rm K} \times 24\ {\rm bit} \\ 12 \ {\rm K} \times 24\ {\rm bit} \end{array}$	enabled disabled enabled disabled enabled	enabled enabled enabled enabled	0 0	0 1 1		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Internal Memories	$\begin{tabular}{ c c c c c } \hline Size \\ \hline 16 \ K \times 24 \ bit \\ \hline 15 \ K \times 24 \ bit \\ \hline 48 \ K \times 24 \ bit \\ \hline 47 \ K \times 24 \ bit \\ \hline 40 \ K \times 24 \ bit \\ \hline 39 \ K \times 24 \ bit \\ \hline 32 \ K \times 24 \ bit \\ \hline \end{array}$	$ \begin{array}{c} 0 \\ 1024 \times 24 \text{-bit} \\ 0 \\ 1024 \times 24 \text{-bit} \\ 0 \\ 1024 \times 24 \text{-bit} \\ 0 \\ \end{array} $	$\begin{array}{c} 24 \ {\rm K} \times \ 24\ {\rm bit} \\ 24 \ {\rm K} \times \ 24\ {\rm bit} \\ 8 \ {\rm K} \times \ 24\ {\rm bit} \\ 8 \ {\rm K} \times \ 24\ {\rm bit} \\ 12 \ {\rm K} \times \ 24\ {\rm bit} \\ 12 \ {\rm K} \times \ 24\ {\rm bit} \\ 12 \ {\rm K} \times \ 24\ {\rm bit} \\ 16 \ {\rm K} \times \ 24\ {\rm bit} \end{array}$	$\begin{array}{c} 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \end{array}$	enabled disabled enabled disabled enabled disabled	enabled enabled enabled enabled enabled	0 0 1	0 1 1 0		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Internal Memories	$\begin{array}{c} \textbf{Size} \\ \hline 16 \ \text{K} \times 24 \text{-bit} \\ 15 \ \text{K} \times 24 \text{-bit} \\ \hline 48 \ \text{K} \times 24 \text{-bit} \\ \hline 47 \ \text{K} \times 24 \text{-bit} \\ \hline 40 \ \text{K} \times 24 \text{-bit} \\ \hline 39 \ \text{K} \times 24 \text{-bit} \\ \hline 32 \ \text{K} \times 24 \text{-bit} \\ \hline 31 \ \text{K} \times 24 \text{-bit} \\ \hline \end{array}$	$\begin{array}{c} 0 \\ 1024 \times 24\text{-bit} \\ 0 \\ 1024 \times 24\text{-bit} \\ 0 \\ 1024 \times 24\text{-bit} \\ 0 \\ 1024 \times 24\text{-bit} \end{array}$	$\begin{array}{c} 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \end{array}$	$\begin{array}{c} 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \end{array}$	enabled disabled enabled disabled enabled enabled	enabled enabled enabled enabled enabled	0 0 1 1	0 1 1 0 0		
*Includes 4 K \times 24-bit shared memory (that is, memory shared by the core and the EFCOP)	Internal Memories	$\begin{array}{c} \textbf{Size} \\ \hline 16 \ \text{K} \times 24\text{-bit} \\ 15 \ \text{K} \times 24\text{-bit} \\ \hline 48 \ \text{K} \times 24\text{-bit} \\ \hline 47 \ \text{K} \times 24\text{-bit} \\ \hline 40 \ \text{K} \times 24\text{-bit} \\ \hline 39 \ \text{K} \times 24\text{-bit} \\ \hline 32 \ \text{K} \times 24\text{-bit} \\ \hline 31 \ \text{K} \times 24\text{-bit} \\ \hline 24 \ \text{K} \times 24\text{-bit} \\ \hline \end{array}$	$\begin{array}{c} 0 \\ 1024 \times 24\text{-bit} \\ 0 \\ \end{array}$	$\begin{array}{c} 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 24 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 8 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 12 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \\ 16 \ {\rm K} \times 24{\text -}{\rm bit} \\ 20 \ {\rm K} \times 24{\text -}{\rm bit} \end{array}$	$\begin{array}{c} 24 \ {\rm K} \times 24\mbox{-bit} \\ 24 \ {\rm K} \times 24\mbox{-bit} \\ 8 \ {\rm K} \times 24\mbox{-bit} \\ 12 \ {\rm K} \times 24\mbox{-bit} \\ 12 \ {\rm K} \times 24\mbox{-bit} \\ 16 \ {\rm K} \times 24\mbox{-bit} \\ 16 \ {\rm K} \times 24\mbox{-bit} \\ 20 \ {\rm K} \times 24\mbox{-bit} \end{array}$	enabled disabled enabled disabled disabled enabled disabled	enabled enabled enabled enabled enabled enabled	0 0 1 1 1	0 1 1 0 0 1		

Table 1.	DSP56L307	Features
	DOI 301007	i catalos



Table 1.	DSP56L307	Features	(Continued))
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Feature	Description			
External Memory Expansion	 Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines External memory expansion port Chip select logic for glueless interface to static random access memory (SRAMs) Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs) up to 100 MHz operating frequency 			
Power Dissipation	 Very low-power CMOS design Wait and Stop low-power standby modes Fully static design specified to operate down to 0 Hz (dc) Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent) 			
Packaging	Molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions.			

Target Applications

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- DSP resource boards
- High-speed modem banks
- Packet telephony

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56L307 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Name	Description	Order Number
DSP56L307 Technical Data	Description, features list, and specifications of the DSP56L307	DSP56L307
DSP56L307 User's Manual	Detailed functional description of the DSP56L307 memory configuration, operation, and register programming	DSP56L307UM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56L307 product website

Table 2.	DSP56L307	Documentation



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DSP56L307PB Rev. 2 1/2005

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