Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	Infrared Motion Detection
Core Processor	eZ8®
Program Memory Type	FLASH (4kB)
Controller Series	Z8 Encore! XP®
RAM Size	256 x 8
Interface	UART/USART
Number of I/O	5
Voltage - Supply	2.7V ~ 3.6V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8fs040bsb20eg

List of Figures

Signal Descriptions

At reset, all port pins are set to the GPIO input state on the 8-pin SOIC package except for $\overline{\text{RESET}}$/DE0/T1$_{OUT}$, which is configured to $\overline{\text{RESET}}$, and PA0/T0$_{IN}$/T0$_{OUT}$/X$_{IN}$/DBG, which is configured to DBG. On the 20- and 28-pin SSOP packages, RESET/PD0 is configured to $\overline{\text{RESET}}$.

Table 3 describes the Z8FS040 Series signals.

Table 3. Z8FS040 MCU Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A–D		
PA[7:0]	I/O	Port A. These pins are used for general-purpose I/O.
PB[5:0]	I/O	Port B. These pins are used for general-purpose I/O.
PC[7:0]	I/O	Port C. These pins are used for general-purpose I/O.
PD[0]	O	Port D. This pin is used for general-purpose output only.
UART Controllers		
TXD0	O	Transmit Data. This signal is the transmit output from the UART and IrDA.
RXD0	I	Receive Data. This signal is the receive input for the UART and IrDA.
CTS0	I	Clear To Send. This signal is the flow control input for the UART.
DE	O	Driver Enable. This signal allows automatic control of external RS-485 drivers. It is approximately the inverse of the Transmit Empty (TXE) bit in the UART Status 0 Register. The DE signal can be used to ensure that the external RS-485 driver is enabled when data is transmitted by the UART.
Timers		
T0$_{OUT}$/T1$_{OUT}$	O	Timer Output 0–1. These signals are outputs from the timers.
T0$_{OUT}$/T1$_{OUT}$	O	Timer Complement Output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0$_{IN}$/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs.
Comparator		
C$_{IN}$P/C$_{IN}$N	I	Comparator Inputs. These signals are the positive and negative inputs to the comparator.
C$_{OUT}$	O	Comparator Output.

Memory Map

The Z8FS040 MCU is based on Zilog's Z8F082A device, which contains a total of 8 KB of Flash memory. Zilog's PIR technology is located in the 4 KB address range `1000h` to `1FFFh`, a code space that is locked and cannot be erased by the user, by the Zilog Debug Interface (ZDI) mass or page erase commands. The remaining 4 KB of this Flash memory space, in the address range `0000h` to `0FFFh`, is available for user application code.

A memory map of the Z8SF040 MCU is illustrated in Figure 5.
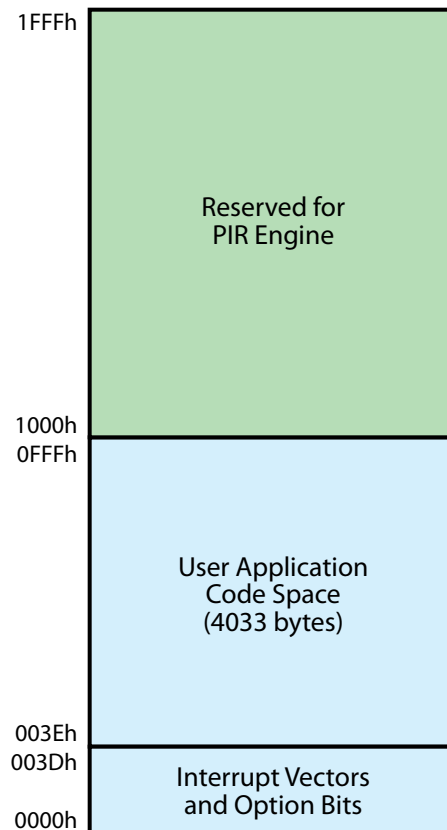
Figure 5. Z8FS040 MCU Program Memory Map

located in the address range 0F0h to 0FFh. See the Zilog's PIR Technology and API chapter on page 19 for details about the API registers and setting up the project memory environment.

Peripherals

The following sections describe the differences, changes, or limitations placed on any of the Z8FS040 peripherals or other functions from the base Z8F082A device. To learn more about the operation of each peripheral please refer to the appropriate section of the Z8 Encore! XP F082A Series Product Specification (PS0228).

Peripheral Availability

Table 4 shows how the Z8FS040 MCU peripherals are used by Zilog's PIR technology and how these peripherals differ from their counterparts on the base Z8F082A device. The peripherals used by the PIR technology should not be used by the application unless the engine is disabled through the PIR Engine Enable Register.

Table 4. Peripheral Availability

	Device		
	Z8FS040xSB20EG	**Z8FS040xHH20EG**	**Z8FS040xHJ20EG**
Base MCU Device	Z8F082ASB020EG	Z8F082AHH020EG	Z8F082AHJ020EG
Pins/Package	8 pin SOIC	20-Pin SSOP	28-Pin SSOP
ADC	ANA2 is used for PIR sensor input. ANA3 is used for a second sensor input in DUAL PYRO Mode.	ANA2 is used for PIR sensor input. ANA3 is connected to ANA6/V_{REF}. ANA3 is used for a second sensor input and ANA6 becomes available in DUAL PYRO Mode.	ANA2 is used for PIR sensor input. ANA3 is connected to V_{REF}. ANA3 is used for a second sensor in DUAL PYRO Mode
VREF	Internal V_{REF} used by the PIR engine and set to 1V.	Internal V_{REF} used by the PIR engine and set to 1V.	Internal V_{REF} used by the PIR engine and set to 1V.
Timer 0	Available to application.	Available to application.	Available to application.
Timer 1	Available to application.	Available to application.	Available to application.

8-Pin Device	Pin 5 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. Any other functions multiplexed with Pin 5 (PA3/$\overline{\text{CTS0}}$, C_{OUT} and T1IN) are not available for user applications.
	In DUAL PYRO Mode (the application uses 2 pyroelectric sensors), Pin 3 (ANA3) is used as an analog ADC input for second sensor and is therefore not available for other functions (T0$_{OUT}$/V_{REF}/CLKIN).
20-Pin Device	Pin 2 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. In SINGLE PYRO Mode, Pin 3 (ANA3) must be externally tied to V_{REF} on Pin 18 (PC2/ANA6/LED/V_{REF}). PC2 will be configured as the V_{REF} output by the PIR engine when it is enabled.
	In DUAL PYRO Mode (which supports 2 pyroelectric sensors), Pin 3 (ANA3) is used for the second sensor. In this mode, the Pin 18 V_{REF} signal is not connected externally to any other ADC inputs and is therefore available to the application (PC2/ANA6/LED/V_{REF}).
28-Pin Device	Pin 1 (ANA2) is reserved as the analog ADC input from the pyroelectric sensor. In SINGLE PYRO Mode, Pin 4 (ANA3) must be externally tied to V_{REF} on Pin 3 (PB5/V_{REF}). PB5 will be configured as V_{REF} output by the PIR engine when it is enabled.
	In DUAL PYRO Mode (which supports 2 pyroelectric sensors), Pin 4 (ANA3) is used for second sensor. In this mode, the Pin 3 V_{REF} signal is not connected externally to any other ADC inputs and is therefore available to the application (PB5/V_{REF}).

Hardware Connection Requirements

This section describes the required external hardware connection for the ZMOTION MCU Series.

Pins are automatically configured to their required function when the PIR engine is initialized via the EPIR_INIT macro.

See Appendix A. Application Schematics on page 43 for example schematic diagrams showing the required connections.

The device can be operated in SINGLE PYRO Mode to support one pyroelectric sensor, or DUAL PYRO Mode to support two pyroelectric sensors. Both of these modes can be operated in NORMAL or LOW SCAN RATE modes.

Depending on the application, there can be up to 3 connection requirements supporting these modes:

Pyroelectric Sensor (PIR Sensor). The signal from the PIR sensor is connected directly to the ANA2 input of the ADC. The ADC is configured for differential, buffered mode by Zilog's PIR technology. The sensor signal should be connected directly to the ADC input with no additional signal conditioning circuitry unless specified by the pyroelectric sensor manufacturer.

ADC V_{REF}. The on-chip V_{REF} is configured for 1 V nominal. The PIR Sensor signal is connected to the "+" differential input of the ADC (ANA2), and the V_{REF} signal is connected to the "–" differential input (ANA3). The 8 pin device has an internal connection from V_{REF} to ANA3 to support this configuration therefore no external hardware connection is required. The 20 and 28 pin devices require an external connection from the V_{REF} out signal to the ADC– (ANA3) input.

Pyroelectric Passive Infrared Sensor #2. In DUAL PYRO Mode, the ADC is still used in differential, buffered mode (the same as SINGLE PYRO Mode). The signal from the second PIR sensor is connected to ANA3. The V_{REF} signal is no longer connected to ANA3 ("–" ADC input). The fist PIR sensor is connected to the "+" ADC input (ANA2) as it is in SINGLE PYRO Mode. The V_{REF} signal is still used internally for the ADC, but the external pin is unused in DUAL PYRO Mode.

Table 9. PIR Status/Control Register 0 (ePIR_SC0)

Bit	7	6	5	4	3	2	1	0
Field	Extended Detection		Engine Disabled	MD Suspend	Motion Direction Control	Motion Direction	Motion Detected	PIR Stable
Control	R/W		R	R/W	R/W	R	R/W	R
Address	102H							

Extended Detection Level (Bits 7–6)

Sets the sensitivity level of the extended detector; controlled by the application.

- These 2 bits enhance the motion detection algorithms to detect slower, faster and/or more subtle motion. The Extended Detection level is selected to provide a balance between additional sensitivity while maintaining stability (no false detections). In certain applications such as lighting control the Extended Detection level can be increased after normal motion has been detected. Extended detection is dependent on the lens pattern used. Smaller lens beams tend to provide more subtle motion detection.
- The Extended Detection level effects user control over the range provided in ePIR_SC2. As the Extended Detection level is increased, the Range setting becomes less effective.

  00 = Extended Detection Level 0 – Minimum (least sensitive).

  01 = Extended Detection Level 1.

  10 = Extended Detection Level 2.

  11 = Extended Detection Level 3 – High (most sensitive).

Engine Disabled (Bit 5)

PIR Engine Disable/Suspend Acknowledged; controlled by the PIR engine.

- This bit indicates the operational status of and is controlled by the PIR engine. When the engine is initialized and enabled by loading the PIR Enable Register with the ePIR_ENABLE_PATTERN value, this bit is cleared to indicate that the Engine is ready. When the Engine is disabled by loading the PIR Enable Register with the ePIR_DISABLE_PATTERN, it will respond by setting this bit to 1 and perform no further operations until reenabled. In order for the Engine to detect that it has been disabled, the user must allow the Engine ADC interrupt to run at least once after loading the PIR Enable Register with the ePIR_DISABLE_PATTERN.

  0 = Engine is enabled and operational.

  1 = Engine is disabled and not operational.

Frequency Response (Bits 6–3)

Frequency Response of PIR engine; controlled by Application

Range: 0h–Ch

- This value determines the frequency response of the motion detection system. Higher values allow lower frequencies to be accepted by the PIR engine. Lower values cause the Engine to ignore targets that generate lower frequencies. These targets typically include horizontally oriented objects such as pets.
- The frequency of the signal that is presented to the PIR engine is largely dependent on the structure of the PIR lens being used (number and dispersion of beams). A lens with several evenly distributed beams provides better frequency response performance than a lens with an uneven beam distribution.

Note: Lower programmed values also have the effect of reducing the relative range of detection.

PIR Scan Rate (Bit 2)

PIR ADC conversion rate for the Pyroelectric Sensor; controlled by the application.

- The PIR engine performs the necessary ADC conversions on the PIR sensor input. Each conversion generates an interrupt that is processed by the PIR engine from the EPIR_ADC_ISR macro. The PIR Scan Rate bit determines the rate at which the ADC conversions are generated.
- In NORMAL SCAN RATE Mode (PIR Scan Rate set to 0), the Z8FS040 ADC peripheral is set to CONTINUOUS CONVERSION Mode, which causes a conversion to be carried out automatically every 256 system clocks. In this mode, the application is only required to execute the EPIR_ADC_ISR macro for each ADC interrupt. The ADC continually runs and continuously generates interrupts.
- When LOW SCAN RATE Mode is selected by setting this bit to a 1, CONTINUOUS CONVERSION Mode is disabled and the ADC is operated in SINGLE-SHOT Mode such that each conversion takes 5129 system clocks to complete. In this mode, the application software must initiate the ADC conversion request (set bit 7 of ADCCTL0) and execute the EPIR_ADC_ISR macro once every 5mS.
- In LOW SCAN RATE Mode, the ADC is disabled between conversions to reduce power consumption. Power consumption can be reduced further if the application software uses this mode in conjunction with the CPU's Halt or Stop modes. Alternately, this mode can be used to provide the application software with additional CPU processing time.
- Although the LOW SCAN RATE Mode provides the application with more processing power and the opportunity for the system to reduce power consumption, the normal scan rate will provide better sensitivity and range. While operating in LOW SCAN RATE Mode, sensitivity is reduced by approximately 20%. The performance of Direction Detection may also be reduced in this mode. EMC immunity is disabled while in LOW SCAN RATE Mode.
- If the PIR Scan Rate bit is changed during engine operation, the engine will stop detecting motion for up to 200mS to avoid potential false motion detection. When changing the PIR SCAN RATE Mode, the Advanced API registers must first be updated with the appropriate values.

  0 = NORMAL SCAN RATE Mode
  1 = LOW SCAN RATE Mode

Table 15. PIR ADC Result Value (ePIR_ADC_Result)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	ADC Result Value															
Control	Read															
Address	10AH								10BH							

PIR ADC Result Value (Bits 15–0)

ADC Scan Request Result Value

Controlled by PIR engine

The PIR ADC Result Value contains the result of the last application requested ADC conversion.

The data format is identical to that discussed in the Z8 Encore XP Product Specification (PS0228) for registers ADCD_H and ADCD_L.

Example for requesting an ANA0 Conversion:

- Set bit 0 (ANA0 Scan Request) in PIR Status/Control Register 3 (ePIR_SC3).
- Wait until the ANA0 Scan Request bit is cleared by the Engine.
- Read the ADC conversion result from the PIR ADC Result Value register

Note: Even though the ADC Result Value is a 16 bit register, atomic operations are not required since the value is only updated at the request of the application.

Table 16. PIR Version (ePIR_Version)

Bit	7	6	5	4	3	2	1	0
Field	Version							
Control	Read							
Address	10CH							

Version (Bits 7–0)

PIR engine software version; controlled by the PIR engine.

- The value stored in this register indicates the software version of the PIR engine.

Value	PIR Engine Software Version
03h	2.00

Advanced API Register Set

The registers listed in Table 17 are available for advanced configuration of the PIR engine. They include customizations for lens and pyroelectric sensor configurations. These registers, each described in this section, are not initialized by the PIR engine.

Table 17. PIR Engine Advanced Registers

API Advanced Register Name	Address	Mnemonic	Description
PIR Advanced Status/Control Register 0 (ePIR_ASC0)	F0h	ePIR_ASC0	EM noise and MD origin status
PIR Advanced Status/Control Register 2 (ePIR_ASC2)	F2h	ePIR_ASC2	Window Size, Lock Level, and Window Update Rate
PIR Process Rate (ePIR_Process_Rate)	F3h/F4h	ePIR_Process_Rate	Relative Processing available to PIR engine
PIR Sample Size Register (ePIR_Sample_Size)	F5h	ePIR_Sample_Size	Controls amount of sensor signal averaging
PIR Debounce Time Register (ePIR_Debounce)	F6h	ePIR_Debounce_Time	Controls time to Debounce motion signal
PIR Debounce Batch Size Register (ePIR_Debounce_Batch)	F7h	ePIR_Debounce_Batch	Controls out of window samples required for Debounce
PIR Transient Sensitivity Level	F8h	ePIR_Transient_Sense	Sets PIR engine sensitivity to transient detection
PIR Noise Sensitivity Level	F9h	ePIR_Noise_Sense	Sets PIR engine sensitivity to noise detection
PIR Signal	FAh/FBh	ePIR_Signal	Current Pyro Sensor signal sample
PIR Pyro DC Signal Level	FCh/FDh	ePIR_Signal_DC	Current calculated Pyro Sensor DC offset

Table 18. PIR Advanced Status/Control Register 0 (ePIR_ASC0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Buffer Refresh	New Sample	MD Origin	EM Noise Detected	EM Transient Detected
Control	0	0	0	R/W	R/W	R	R/W	R/W
Address	F0H							

Reserved (Bits 7–5)

Buffer Refresh (Bit 4)

Uses a fast-fill algorithm to quickly refill the motion detection buffers; controlled by the application.

This bit is used to restart motion detection by quickly reinitializing and refilling the motion detection constructed sample buffers. This method can be used to restore motion detection after waking up from SLEEP Mode, or it can be used to help ignore external events that may cause false detections.

Waking up from SLEEP Mode:

If this bit is set when the EPIR_INIT macro is executed the Engine refills the constructed sample buffers with a fast fill algorithm that allows it to quickly restore motion detection. Typically, a simple external wake-up circuit would be implemented that provides an unqualified motion detection signal to wake up the MCU from SLEEP Mode (SMR). Upon SMR, the application would set the Buffer Refresh bit, execute EPIR_INIT, and then continue with normal motion detection functions for some period of time before returning to SLEEP Mode. By setting this bit prior to EPIR_INIT, the Engine buffers are filled much faster enabling it to analyze the original signal seen by the external wake-up circuit and determine if it is actual motion.

Ignoring False Detection Events:

If the MCU is used to control external components (LED's, relays, lights, triacs, etc.), a fluctuation on the power supply can be created as the external device is turned on or off. The Buffer Refresh bit can be used to ignore any false detection that could be created by these fluctuations. When the external device is turned on or off, the application can set the Buffer Refresh bit to effectively reset the motion detection history and therefore ignore any effect from the external device.

New Sample (Bit 3)

New sample available from PIR Signal High/Low Register.

Set by the PIR engine, cleared by the application.

- This bit indicates that the PIR engine has a new sensor signal input sample available that may be read by the application. This status is available as an advanced feature as the application is not normally required to read the sampled PIR sensor signal. The application must clear this bit when the sample has been read.

Window Size (Bits 4–3)

Controlled by the application.

This register determines the size of the control limit window. A larger window size produces more stable control limits at the cost of additional CPU usage. If a smaller window size is used, the more frequently the window can be calculated which allows it to track the signal better.

> 00 = Reserved
>
> 01 = Small window
>
> 02 = Medium window
>
> 03 = Large window

Window Update Rate (Bits 2–0)

Controlled by the application.

This register determines how frequently the control limits are calculated. It is measured in PIR samples. A smaller number produces more frequent calculations which allow the control limits to track the signal better, at the cost of increased CPU usage. The valid range is 0 to 7.

- The window is updated every 4 + (Window Update Rate * 2) PIR samples.

Table 20. PIR Process Rate (ePIR_Process_Rate)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	PIR Process Rate															
Control	Read															
Address	F3H								F4H							

PIR Process Rate (Bits 7–0)

Controlled by PIR engine

The PIR Process Rate Indicator is provided by the Engine to determine if the user application process and interrupts overhead is impacting the performance of the Engine. If the Engine process rate drops significantly, its ability to detect motion can be significantly reduced. This value is typically used at the application development stage. This number gives an indication of how much CPU time the Engine is receiving. Higher numbers are better. Generally, if the process rate drops below 0080h, the ability to detect motion could be compromised.

Note: The 16-bit value provided by these two 8-bit registers must be read as an atomic operation by the application. This can be ensured by either using the CPU's ATM instruction or by disabling interrupts while reading the two 8 bit registers.

Table 23. PIR Debounce Batch Size Register (ePIR_Debounce_Batch)

Bit	7	6	5	4	3	2	1	0
Field	PIR Debounce Batch Size							
Control	Read/Write							
Address	F7H							

Debounce Batch Size (Bits 7–0)

Controlled by the application.

This register determines the number of consecutive out-of-window samples required to consider the sequence a valid debounce count. The field works as a mask. Increasing the mask size (i.e. more bits set to 1) will increase the noise immunity of the engine but result in lower sensitivity to subtle motion signals.

Valid values are 01h, 03h, 07h, 0Fh, 1Fh, 3Fh, 7Fh, and FFh.

Table 24. PIR Transient Sensitivity Level (ePIR_Transient_Sense)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PIR Transient Sensitivity						
Control	0	Read/Write						
Address	F8H							

Reserved (Bit 7)

Transient Sensitivity (Bits 6–0)

Controlled by the application.

This register determines how sensitive the transient detection part of the engine is to sudden changes in the PIR signal. A lower number makes the engine more sensitive, at the cost of potential rejection of large signal motion (ex. warm target very close to detector).

The valid range is 0 (disabled) to 64h.

Related Documents

Additional information can be found in the following documents, available from the Zilog website at www.zilog.com.

Document Number	Description
AN0301	Power Management and Customer Sensing with Zilog's ZMOTION Detection Module Application Note
AN0307	ZMOTION Detection Module Application Walkthrough Application Note
AN0309	High Brightness LED Reference Design Application Note
PB0223	ZMOTION Detection Module Product Brief
PB0225	ZMOTION Detection and Control Product Brief
PS0228	Z8 Encore! XPF082A Series Product Specification
PS0284	ZMOTION Detection Module Product Specification
PS0286	ZMOTION Lens and Pyroelectric Sensor Product Specification
QS0073	ZMOTION Detection Module Evaluation Kit Quick Start Guide
QS0076	ZMOTION Detection and Control Development Kit Quick Start Guide
UM0223	ZMOTION Detection Module Evaluation Kit User Manual
UM0230	ZMOTION Detection and Control Development Kit User Manual
WP0017	A New PIR Motion Detection Architecture White Paper
WP0018	ZMOTION Detection Lens and Pyro Sensor Configuration Guide

Appendix A. Application Schematics

The ZMOTION Detection and Control MCU is available in 8-pin, 20-pin and 28-pin parts and configurable with dual and quad pyro sensor and lens combinations.

8-Pin Z8FS040xSB20EG MCU

Figure 10 shows an example circuit for part number *Z8FS040xSB20EG*, an 8-pin ZMO-TION Detection and Control MCU. The interface to the pyroelectric sensor is via the dedicated input ANA2 (pin 5). The status LED is driven by pin 6 which is normally configured as a GPIO by the application to control the state of the LED. Pin 2 is used as the debug input to the chip, but can be used for other functions as required. Pin 4 is set up for the Reset function, but may also be used for other functions as the application requires. Pull-up resistors (10K) are provided on the Debug and Reset signals as required for the Debug interface. The signals on pins 3 and 7 can be used as required. The power supply design is left to the application requirements.

In DUAL PYRO Mode, the second Pyroelectric sensor is connected to Pin 3 (ANA3). All other connections remain the same.

5. Initialize any application-specific I/O and peripherals.

6. Enable interrupts.

7. Ensure that the PIR Sensor Stable bit (ePIR_SC0:0) is set.

8. Continue with the application.

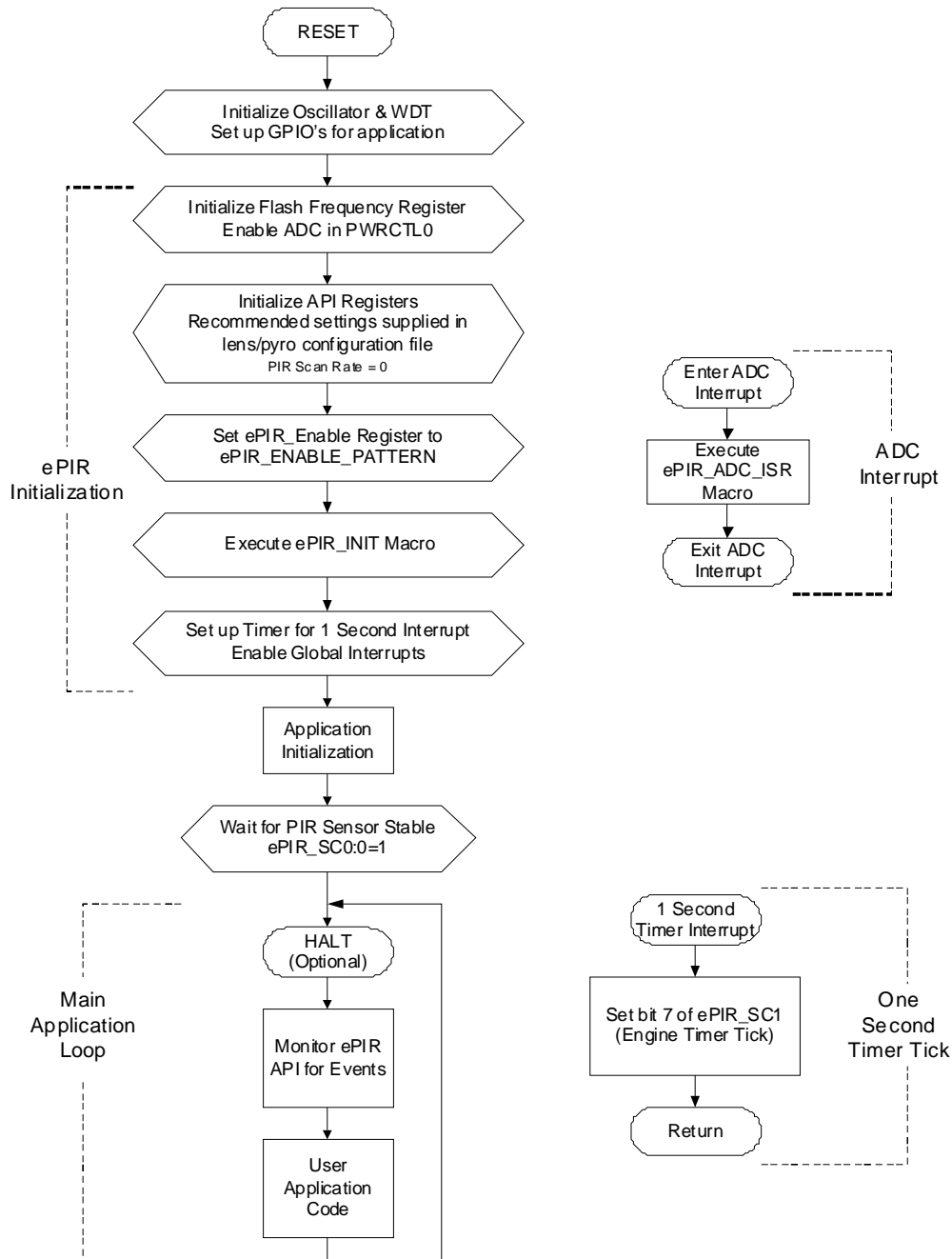The flow diagram in Figure 15 shows the general software operation for NORMAL SCAN RATE Mode.

Figure 12. Application Flow Diagram: Normal Scan Rate

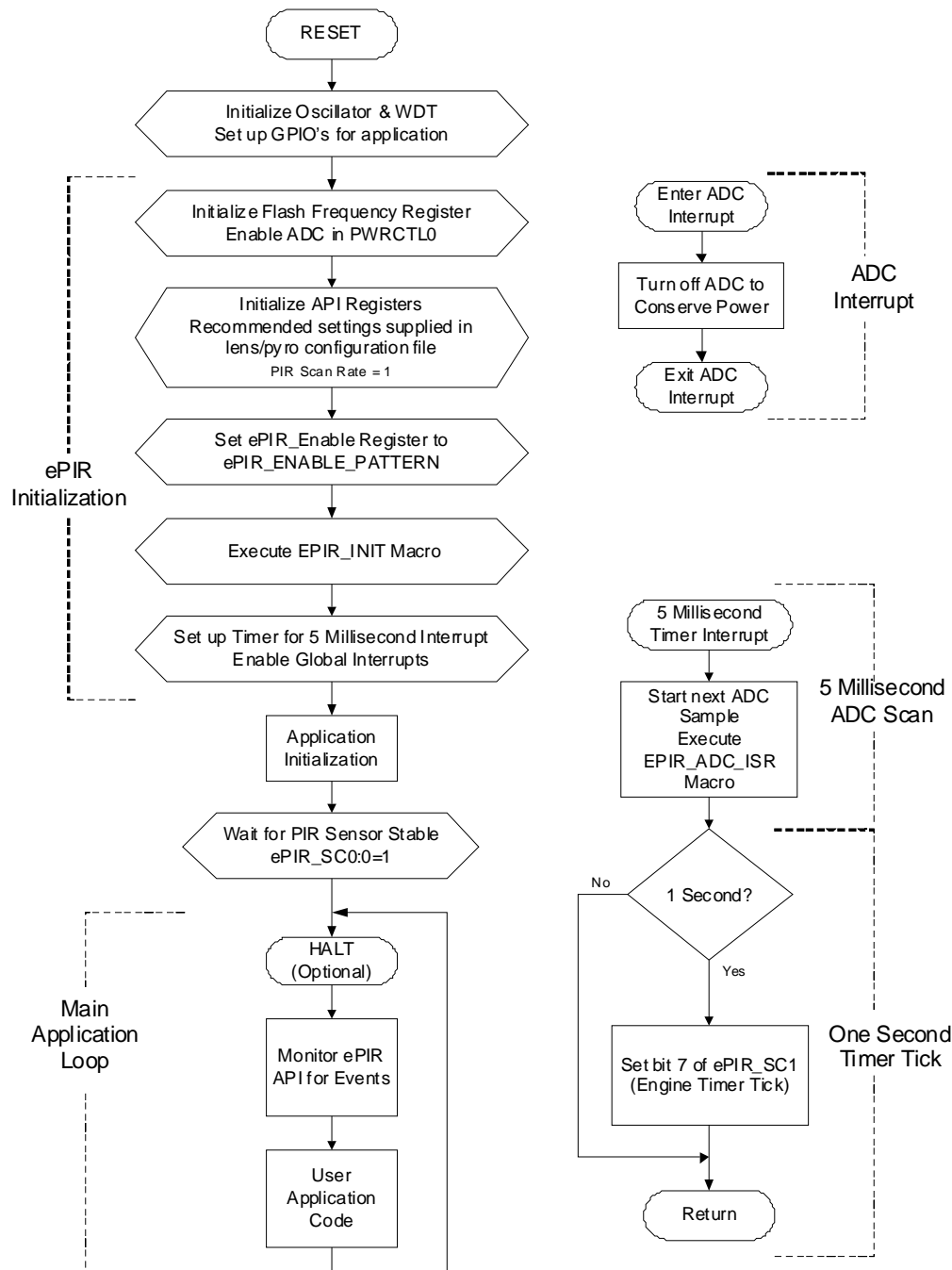The flow diagram in Figure 16 shows the general software operation for LOW SCAN RATE Mode.

Figure 13. Application Flow Diagram: Low Scan Rate

- – Address range `10h` to `1Fh` is the working register group reserved for first level interrupt
  - – If more than 1 level of interrupt nesting is required by the application, the `20h` must be increased by `10h` for every additional nesting level.
  - – Address range `F0h` to `FFh` contains the Advanced API Registers

- EData: `100h–10Fh`, `110h–18Fh`
  - – Defined in ZDS II Project Settings under Linker Address Spaces
  - – Address range `100h` to `10Fh` contains the Standard API Registers

- SP = `80h`
  - – Defined in `startupePIR.asm`
  - – First stack location is `7Fh` and it grows down

- RP = `00h`
  - – Defined in `startupePIR.asm`
  - – The application code uses working register group 0

- __intrp = `10h`
  - – Defined in `startupePIR.asm`
  - – First level interrupt uses working register group 1

- Engine RP = `E0h`
  - – This is the working register group used by the PIR engine
  - – Defined by the Engine Entry macro's EPIR_INIT and EPIR_ADC_ISR

Table 35. ZMOTION Lens and Pyroelectric Sensor Selection Guide (Continued)

Part Number	Description	Typical Applications	Configuration Header File	Pyroelectric Sensor
NCL-3R Lens Specification	10mm ceiling/wall mount array (360°) • Clips on to pyroelectric sensor • 2:1 diameter-to-height coverage • 14 zones • 5 meter range	Room occupancy and proximity sensing • Lighting control • HVAC control • Appliances • Kiosk/display control • Vending power management	ePIR_INIT_08.h	RE200B-P SBDI46-504AA
NCL-10S Lens Specification	10mm wall mount array (18°) • Clips on to pyroelectric sensor • 2 beams X (27°) • 1 beam Y (18°) • 10 meter range	Entrance detection with directional detection • Kiosk/display counters • Vending • HVAC • Entrance/access control	ePIR_INIT_09.h	RE200B-P