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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	68
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l387anfp-u1

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Table 1.15 Product List for R8C/L3AB Group **Current of Oct. 2009**

Part No.	Internal ROM Capacity	Internal RAM Capacity	Package Type	Remarks
R5F2L3A7BNFP	48 Kbytes	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7BNFA	48 Kbytes	6 Kbytes	PRQP0100JD-B	
R5F2L3A8BNFP	64 Kbytes	8 Kbytes	PLQP0100KB-A	
R5F2L3A8BNFA	64 Kbytes	8 Kbytes	PRQP0100JD-B	
R5F2L3AABNFP	96 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3AABNFA	96 Kbytes	10 Kbytes	PRQP0100JD-B	
R5F2L3ACBNFP	128 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3ACBNFA	128 Kbytes	10 Kbytes	PRQP0100JD-B	
R5F2L3A7BDFP	48 Kbytes	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7BDFA	48 Kbytes	6 Kbytes	PRQP0100JD-B	
R5F2L3A8BDFP	64 Kbytes	8 Kbytes	PLQP0100KB-A	
R5F2L3A8BDFA	64 Kbytes	8 Kbytes	PRQP0100JD-B	
R5F2L3AABDFP	96 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3AABDFA	96 Kbytes	10 Kbytes	PRQP0100JD-B	
R5F2L3ACBDFP	128 Kbytes	10 Kbytes	PLQP0100KB-A	
R5F2L3ACBDFA	128 Kbytes	10 Kbytes	PRQP0100JD-B	

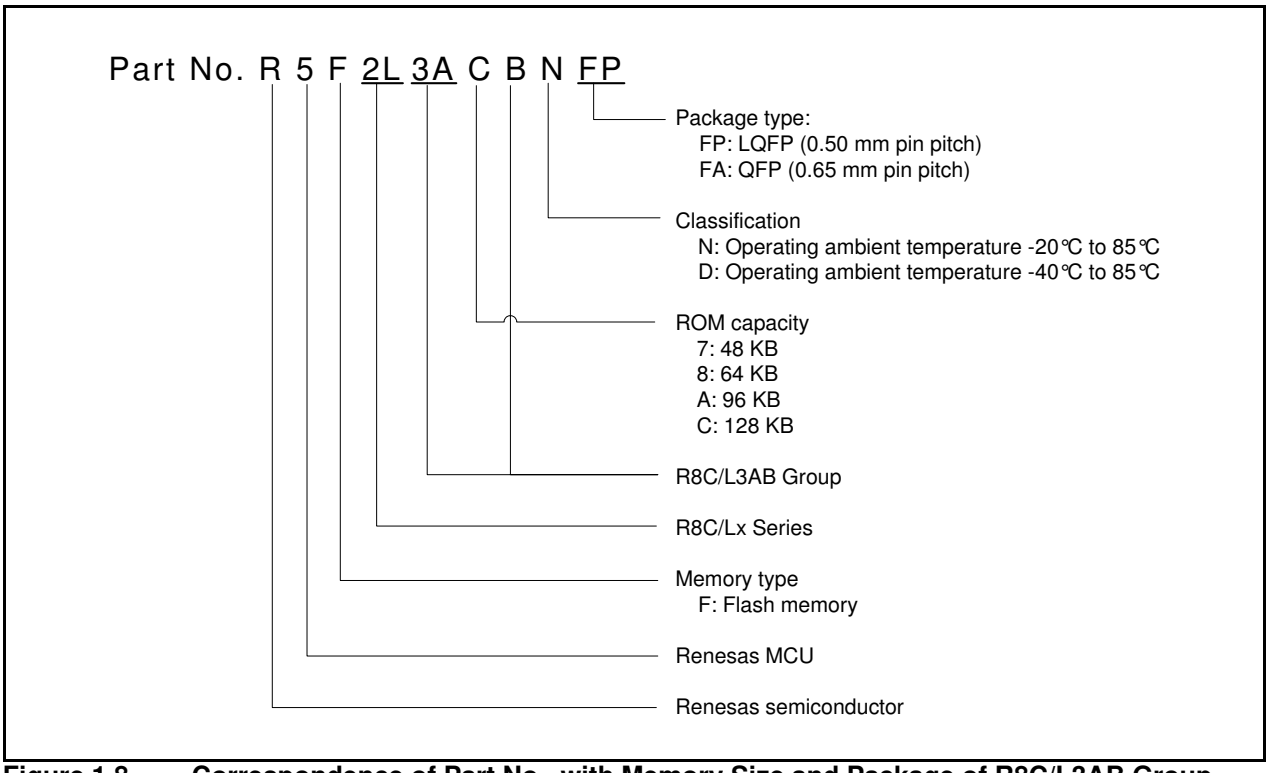


Figure 1.8 Correspondence of Part No., with Memory Size and Package of R8C/L3AB Group

Table 6.9 Port P3

Pin	Register	PD3	LSE3	INTSR	INTEN	INTEN1	ADMOD		TRBRCSR		TRCMR	TRCCR2		Function
	Bit	PD3_i	LSEi+24	INTiSEL0	INTiEN	INTiEN	ADCAP1	ADCAP0	TRCTRGSEL1	TRCTRGSEL0	PWM2	TCEG1	TCEG0	
Port P3_0 SEG24 $\overline{\text{INT0}}$	i = 0	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—		—		—	—		—	LCD drive control output (SEG24)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT0}}$ input (1)
Port P3_1 SEG25 $\overline{\text{INT1}}$	i = 1	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG25)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT1}}$ input (1)
Port P3_2 SEG26 $\overline{\text{INT2}}$	i = 2	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—		—		—	—		—	LCD drive control output (SEG26)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT2}}$ input (1)
Port P3_3 SEG27 $\overline{\text{INT3}}$	i = 3	0	0	X	X	—	—	—	—	—	—	—	—	Input port (1)
		1	0	X	X	—	—	—	—	—	—	—	—	Output port
		X	1	X	X	—	—	—	—	—	—	—	—	LCD drive control output (SEG27)
		0	0	0	1	—	—	—	—	—	—	—	—	$\overline{\text{INT3}}$ input (1)
Port P3_4 SEG28 $\overline{\text{INT4}}$	i = 4	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X		—		—	—		—	LCD drive control output (SEG28)
		0	0	0	—	1	—	—	—	—	—	—	—	$\overline{\text{INT4}}$ input (1)
Port P3_5 SEG29 $\overline{\text{INT5}}$	i = 5	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X	—	—	—	—	—	—	—	LCD drive control output (SEG29)
		0	0	0	—	1	—	—	—	—	—	—	—	$\overline{\text{INT5}}$ input (1)
Port P3_6 SEG30 $\overline{\text{INT6}}$	i = 6	0	0	X	—	X	—	—	—	—	—	—	—	Input port (1)
		1	0	X	—	X	—	—	—	—	—	—	—	Output port
		X	1	X	—	X		—		—	—		—	LCD drive control output (SEG30)
		0	0	0	—	1	—	—	—	—	—	—	—	$\overline{\text{INT6}}$ input (1)
Port P3_7 SEG31 $\overline{\text{INT7}}$ $\overline{\text{ADTRG}}$ TRCTRG	i = 7	0	0	X	—	X	X	X	X	X	X	X	X	Input port (1)
		1	0	X	—	X	X	X	X	X	X	X	X	Output port
		X	1	X	—	1	X	X	X	X	X	X	X	LCD drive control output (SEG31)
		0	0	0	—	1	X	X	X	X	X	X	X	$\overline{\text{INT7}}$ input (1)
		0	0	0	—	1	1	1	X	X	X	X	X	$\overline{\text{ADTRG}}$ input (1)
		0	0	X	— —	X	X	X	0	1	0	0 1	1 X	PWM2 mode TRCTRG input (1)

X: 0 or 1; —: No change in outcome

Note:

1. Pulled up by setting the corresponding bit in the P3PUR register to 1.

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
Timer RD: Registers TRDi (i = 0 or 1), TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi
Timer RG: Registers TRG, TRGGRA, and TRGGRB
SSU: Registers SSTDR, SSTDRH, SSRDR, and SSRDRH
UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, U2RB, U2SMR5, U2SMR4, U2SMR3, U2SMR2, and U2SMR
A/D converter: Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1
D/A converter: Registers DA0 and DA1
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in Table 7.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt. Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

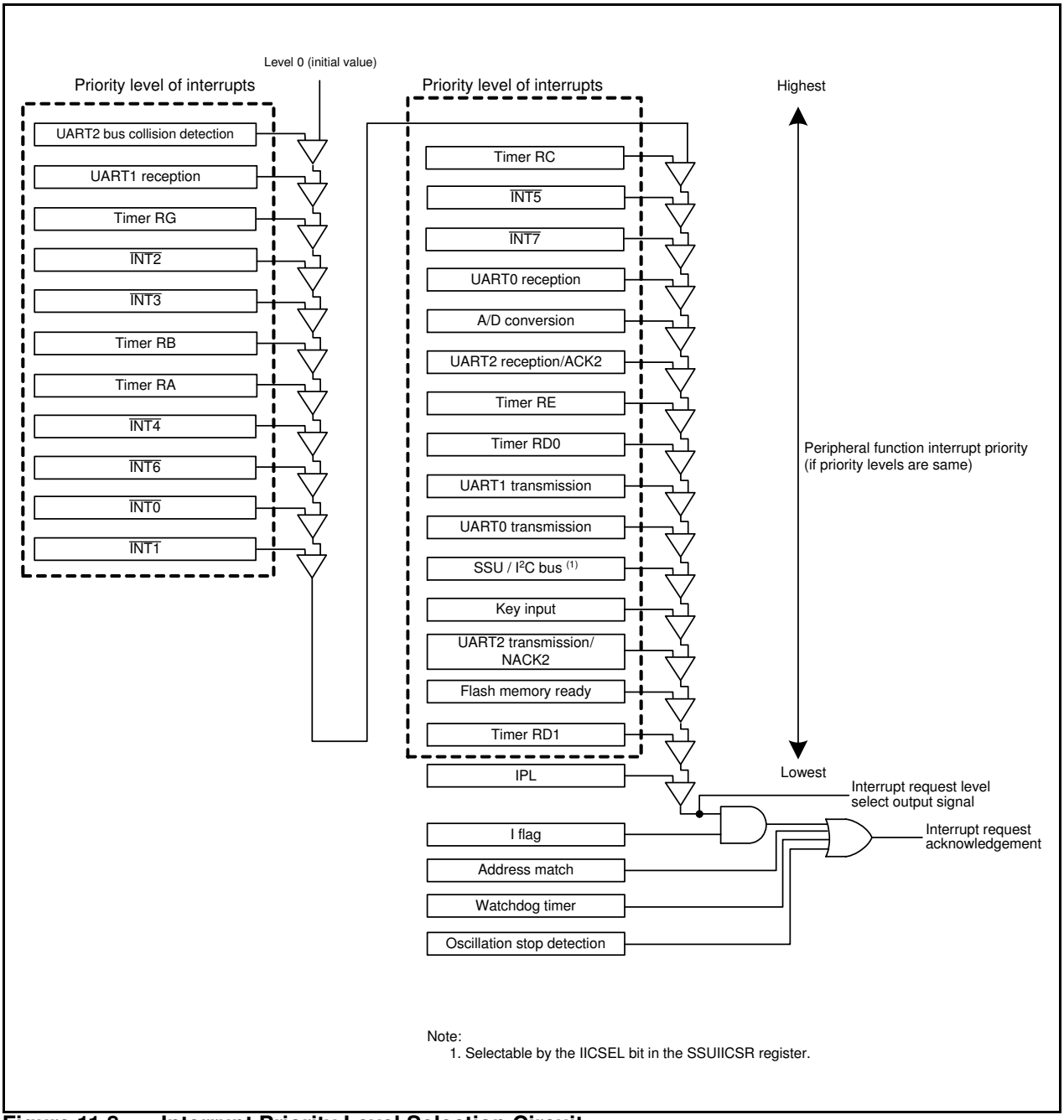


Figure 11.8 Interrupt Priority Level Selection Circuit

11.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi (i = 0 or 1) register. This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi (i = 0 or 1) register. The AIERi bit in the AIERi register can be used to select the interrupt enabled or disabled. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **11.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.8 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged.

Table 11.8 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than listed above	Address indicated by RMADi register + 1

Notes:
1. Refer to the **11.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001). **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 11.9 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

14.1 Introduction

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.3 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows the Watchdog Timer Block Diagram.

Table 14.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting). (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selectable by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selectable by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)

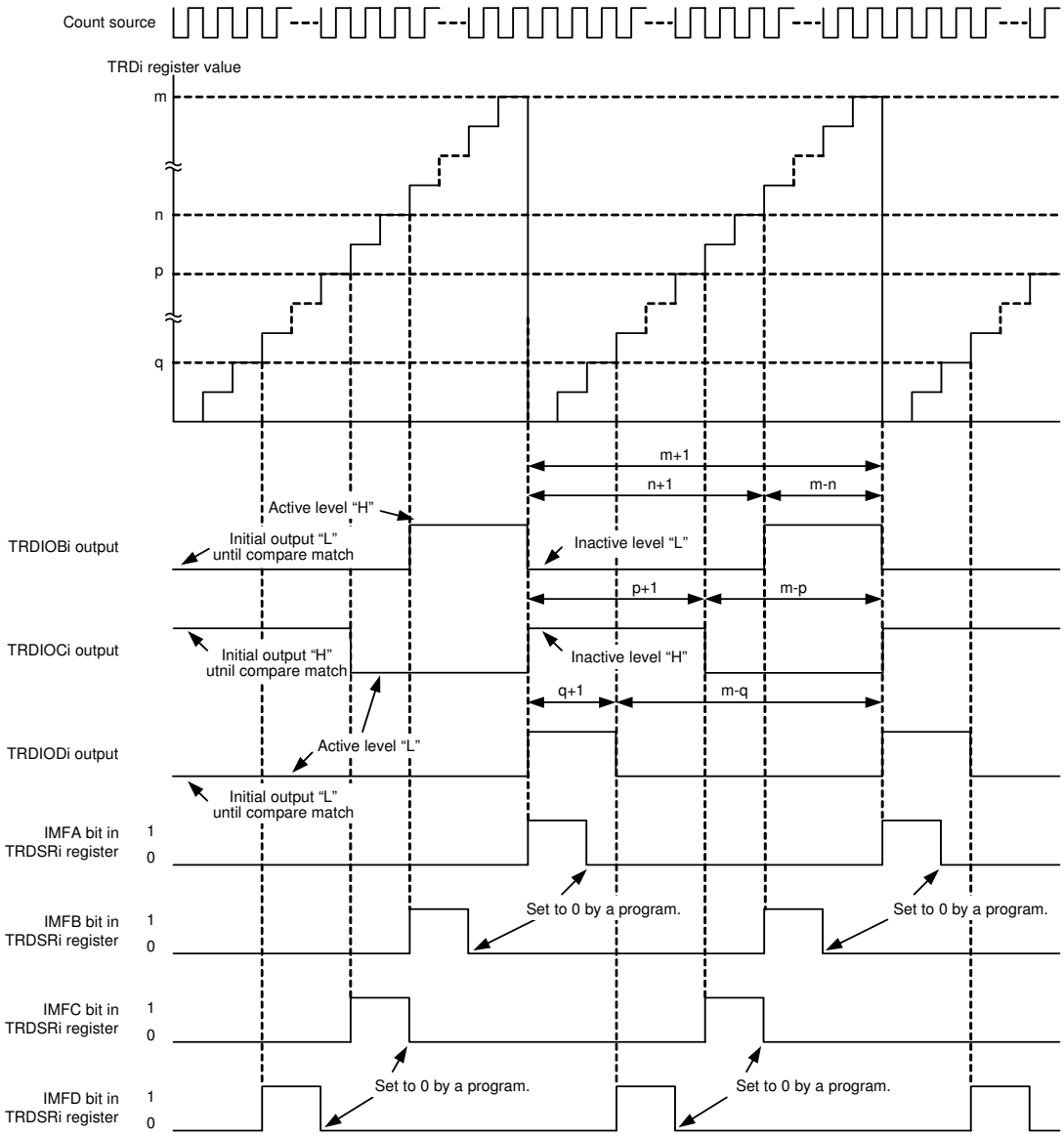
Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCIOBSEL1	TRCIOBSEL0	—	—	—	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA pin select bit	0: TRCIOA pin not used 1: TRCIOA pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	TRCIOBSEL0	TRCIOB pin select bit	b5 b4 0 0: TRCIOB pin not used 0 1: P4_5 assigned 1 0: P4_6 assigned 1 1: P4_7 assigned	R/W
b5	TRCIOBSEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The TRCPSR0 register selects whether to use the timer RC input. To use the input pins for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value of this register during timer RC operation.

20.5.19 Operating Example



i = 0 or 1

m: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register
q: Value set in TRDGRDi register

The above applies under the following conditions:
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EBi, ECi and EDi in the TRDOER1 register are set to 0 (TRDIOBi, TRDIOCi and TRDIODi pin output enabled).
Bits TOBi and TOCi in the TRDOCR register are set to 0 (inactive level), the TODi bit is set to 1 (active level).
The POLB bit in the TRDPOCRi register is set to 1 (active level is high), bits POLC and POLD are set to 0 (active level is low).

Figure 20.15 Operating Example in PWM Mode

20.6.11 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt (IMIA) by IMFA bit disabled 1: Interrupt (IMIA) by IMFA bit enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt (IMIB) by IMFB bit disabled 1: Interrupt (IMIB) by IMFB bit enabled	R/W
b2	IMIEC	Input-capture/compare-match interrupt enable bit C	0: Interrupt (IMIC) by IMFC bit disabled 1: Interrupt (IMIC) by IMFC bit enabled	R/W
b3	IMIED	Input-capture/compare-match interrupt enable bit D	0: Interrupt (IMID) by IMFD bit disabled 1: Interrupt (IMID) by the IMFD bit enabled	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Interrupt (OVI) by OVF bit disabled 1: Interrupt (OVI) by OVF bit enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.6.12 Timer RD Counter 0 (TRD0) in Reset Synchronous PWM Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	A count source is counted. Count operation is increment. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
The TRD1 register is not used in reset synchronous PWM mode.

22.3.2 Buffer Operation

The BUFA or BUFB bit in the TRGIOR register can be used to select the TRGGRC or TRGGRD register as the buffer register of the TRGGRA or TRGGRB register.

- Buffer register of TRGGRA register: TRGGRC register
- Buffer register of TRGGRB register: TRGGRD register

Buffer operation differs depending on the mode.

Table 22.5 lists the Buffer Operation in Each Mode, Figure 22.3 shows the Buffer Operation of Input Capture Function, and Figure 22.4 shows the Buffer Operation of Output Compare Function.

Table 22.5 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	The content of the TRGGRA (TRGGRB) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRG register and the TRGGRA (TRGGRB) register	The content of the buffer register is transferred to the TRGGRA (TRGGRB) register.

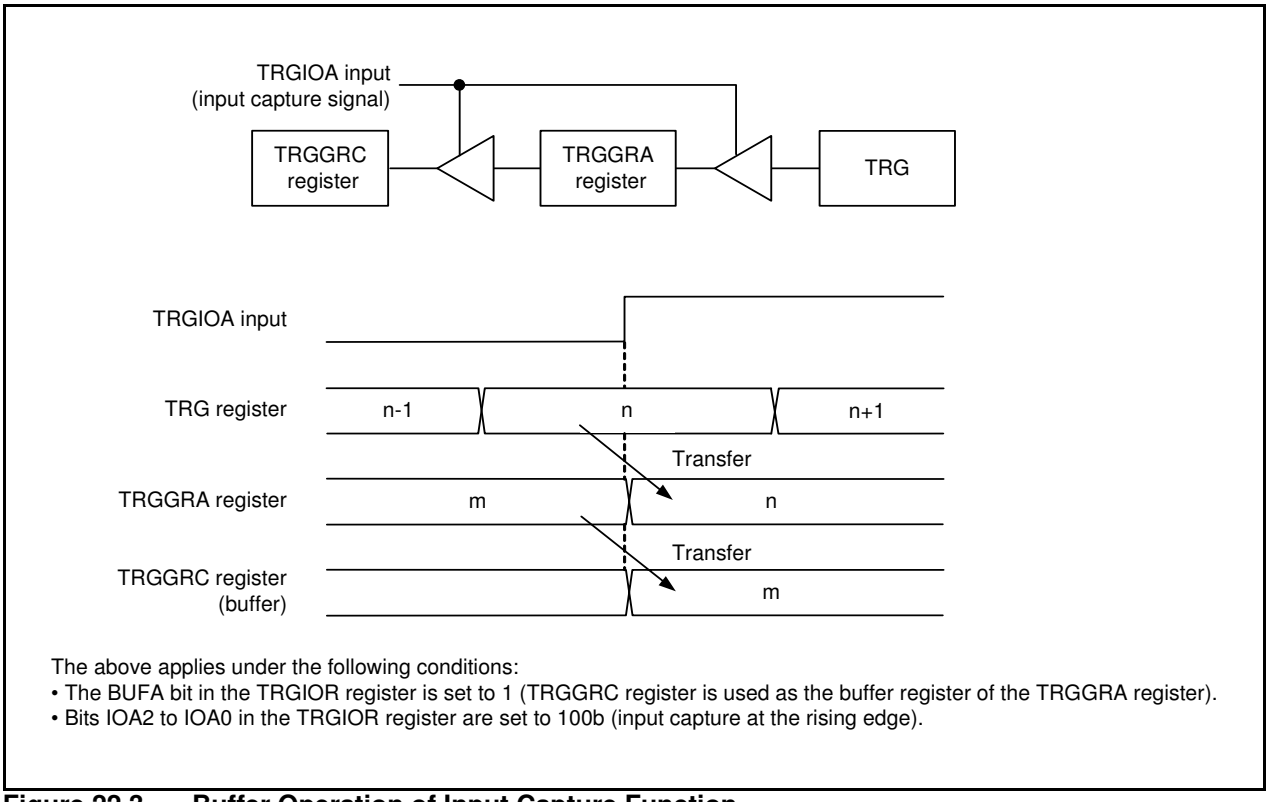


Figure 22.3 Buffer Operation of Input Capture Function

22.4.2 Procedure Example for Setting Input Capture Operation

Figure 22.6 shows a Procedure Example for Setting Input Capture Operation.

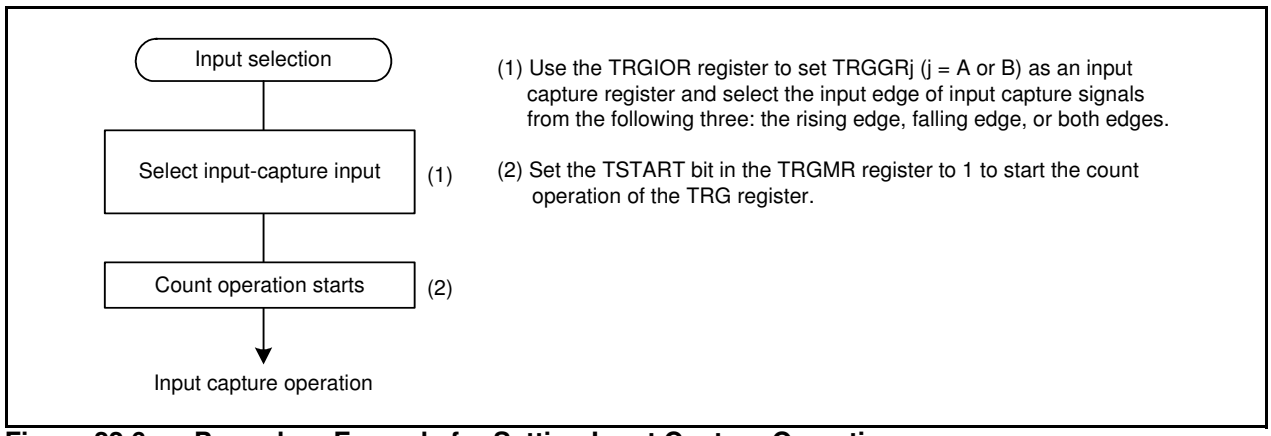


Figure 22.6 Procedure Example for Setting Input Capture Operation

22.4.3 Input Capture Signal Timing

The rising edge, falling edge, or both edges can be selected for input-capture input by setting the TRGIOR register.

Figure 22.7 shows the Input-Capture Input Signal Timing.

The pulse width of input-capture input signals should be 1.5 f1 or more for a single edge and 2.5 f1 or more for both edges.

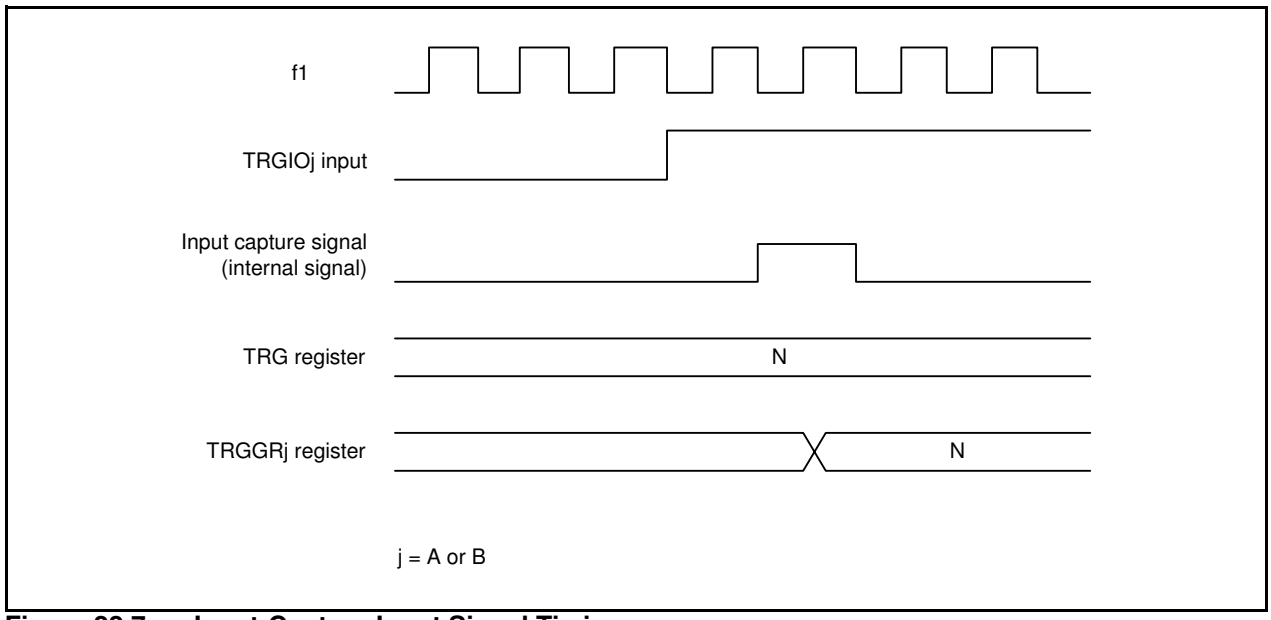


Figure 22.7 Input-Capture Input Signal Timing

23.2.8 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK1SEL0	—	RXD1SEL0	—	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	0: TXD1 pin not used 1: TXD1 pin used	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD1SEL0	RXD1 pin select bit	0: RXD1 pin not used 1: RXD1 pin used	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK1SEL0	CLK1 pin select bit	0: CLK1 pin not used 1: CLK1 pin used	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U1SR register selects which pin is assigned as the UART1 input/output. To use the I/O pins for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value of this register during UART1 operation.

26.5.2 Data Transmission

Figure 26.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During the data transmit operation, the synchronous serial communication unit operates as described below (the data transfer length can be set from 8 to 16 bits using the SSBR register).

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is low-input state.

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmission enabled), the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1 at this time, the TXI interrupt request is generated.

After one frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. When the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled) at this time, the TEI interrupt request is generated. The SSCK pin remains high after transmit-end and the $\overline{SCS}$ pin is held high. When transmitting continuously while the $\overline{SCS}$ pin is held low, write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as the master device. The SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is high-input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 26.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

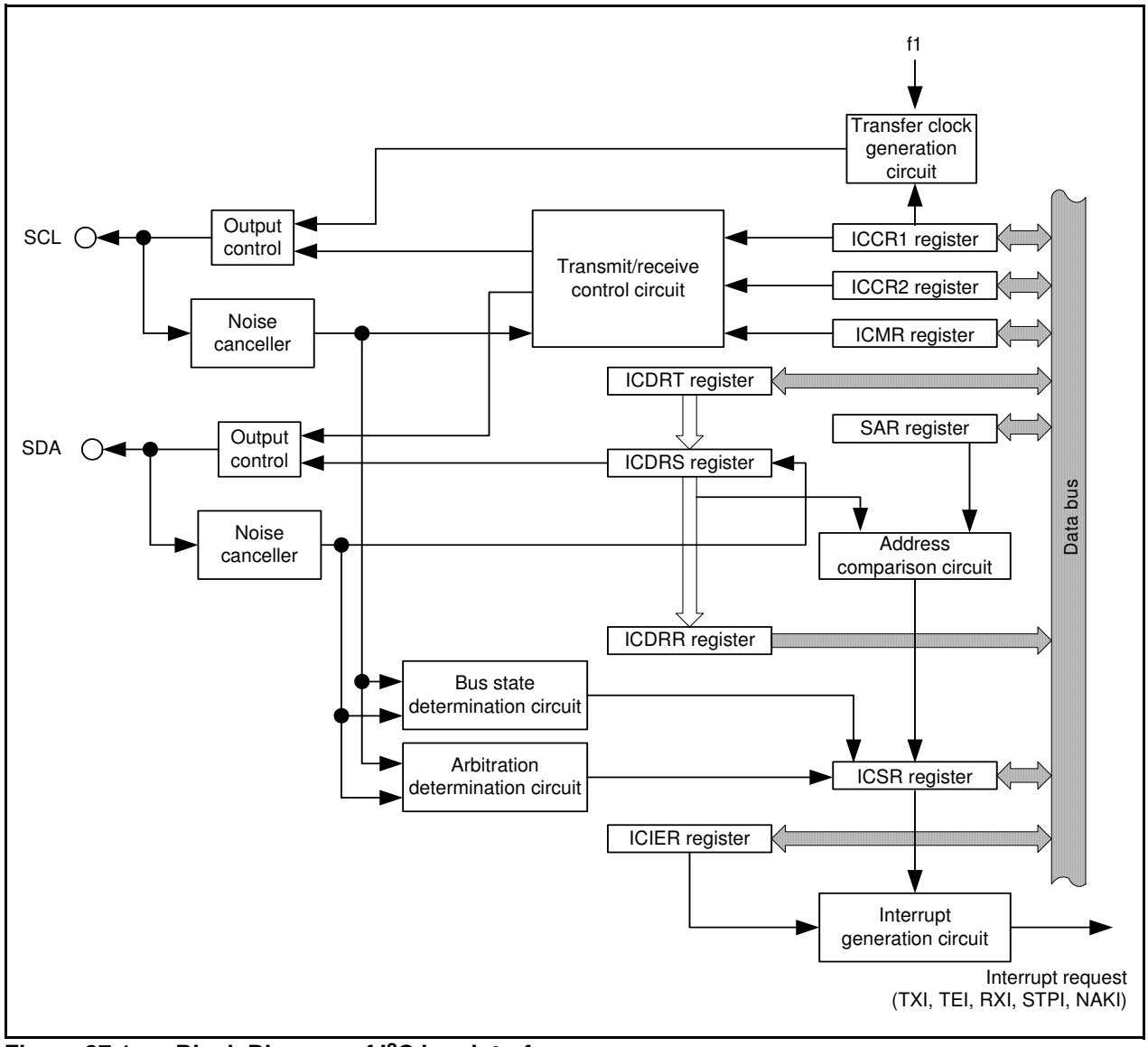


Figure 27.1 Block Diagram of I2C bus interface

Table 27.2 I2C bus Interface Pin Configuration

Pin Name	Assigned Pin	Function
SCL	P11_0	Clock I/O
SDA	P11_2	Data I/O

29.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). The register where the result is stored varies depending on the A/D operating mode used. The contents of the ADi register are undefined after reset. Values cannot be written to the ADi register.

In repeat mode 0, no interrupt request is generated. After the first AD conversion is completed, determine if the A/D conversion time has elapsed by a program.
In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).
However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.

In one-shot mode and single sweep mode, when bits ADCAP1 to ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.

During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

29.3.5 Low-Current-Consumption Function

When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for one ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during the A/D conversion.

29.3.6 Extended Analog Input Pins

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as analog input.
Any variation in VREF can be confirmed using the on-chip reference voltage. Use the ADEX0 bit in the ADCON1 register and the OCVREFAN bit in the OCVREFCR register to select the on-chip reference voltage.
The A/D conversion result of the on-chip reference voltage in one-shot mode or in repeat mode 0 is stored in the AD0 register.

29.3.7 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is incorporated to fix the electric charge on the chopper amp capacitor to the predetermined state (AVCC or GND) before starting conversion.
This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins.
Figure 29.5 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) and Figure 29.6 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected).

32.5 LCD Drive Waveform

32.5.1 Segment Panel Control Waveform

Figures 32.6 to 32.17 show the LCD drive waveform corresponding to each duty and bias for segment panel control (LWAV = 0).

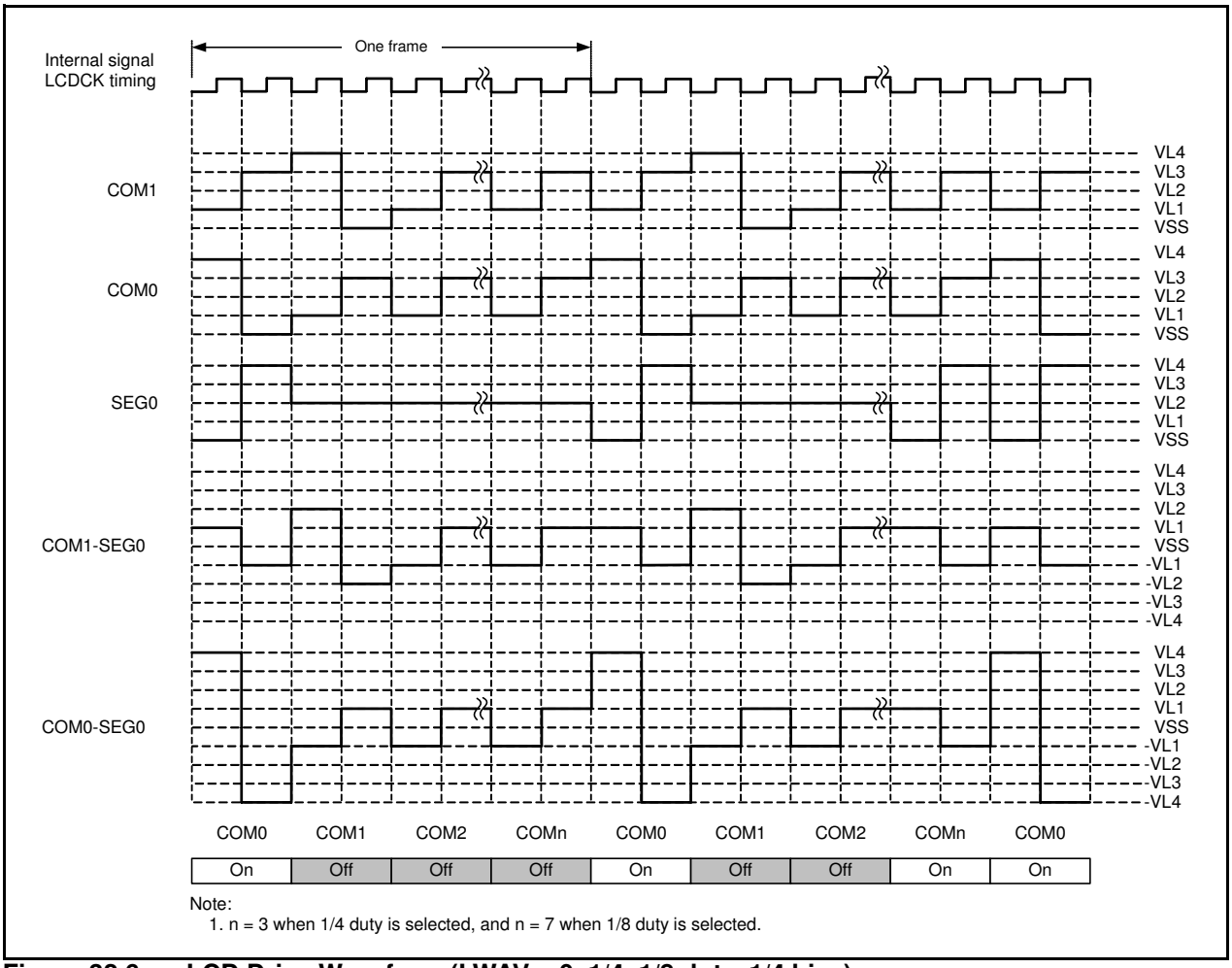


Figure 32.6 LCD Drive Waveform (LWAV = 0, 1/4, 1/8 duty, 1/4 bias)

Table 34.8 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
–	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	–	30	100	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	3	–	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
–	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	–	30	100	µs
–	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	–	2	–	µA

Table 34.9 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on (1)		–	–	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 34.10 LCD Drive Control Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL4	2.2	–	5.5	V
VL3	VL3 voltage		VL2	–	VL4	V
VL2	VL2 voltage	R8C/L35A, R8C/L35B	VL1	–	VL4	V
		R8C/L36A, R8C/L36B, R8C/L38A, R8C/L38B, R8C/L3AA, R8C/L3AB	VL1	–	VL3	V
VL1	VL1 voltage		1	–	VL2	V
–	VL1 internally-generated voltage accuracy (1)		Setting voltage −0.4	Setting voltage	Setting voltage +0.4	V
f(FR)	Frame frequency		50	–	180	Hz
ILCD	LCD drive control circuit current		–	(Note 2)	–	µA

Notes:
1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to Table 34.13 DC Characteristics (2), Table 34.15 DC Characteristics (4), and Table 34.17 DC Characteristics (6).

Table 34.11 Power-Off Mode Characteristics (VCC = 2.2 to 5.5 V, VSS = 0 V, and Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	Power-off mode operating supply voltage		2.2	–	5.5	V

Table 34.22 Timing Requirements of Serial Interface
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	300	–	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	150	–	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	150	–	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	–	80	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	0	–	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	70	–	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	90	–	90	–	ns

i = 0 to 2

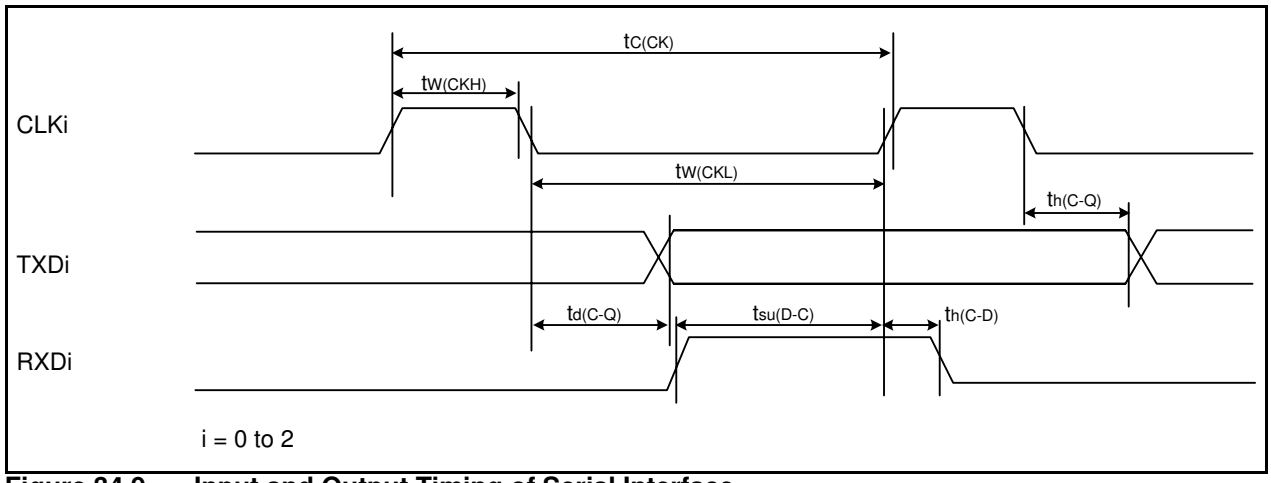


Figure 34.9 Input and Output Timing of Serial Interface

Table 34.23 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 7) and Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	–	380 (1)	–	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	–	380 (2)	–	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

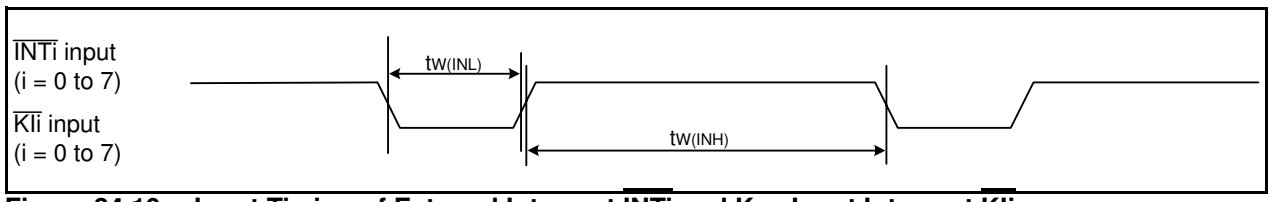
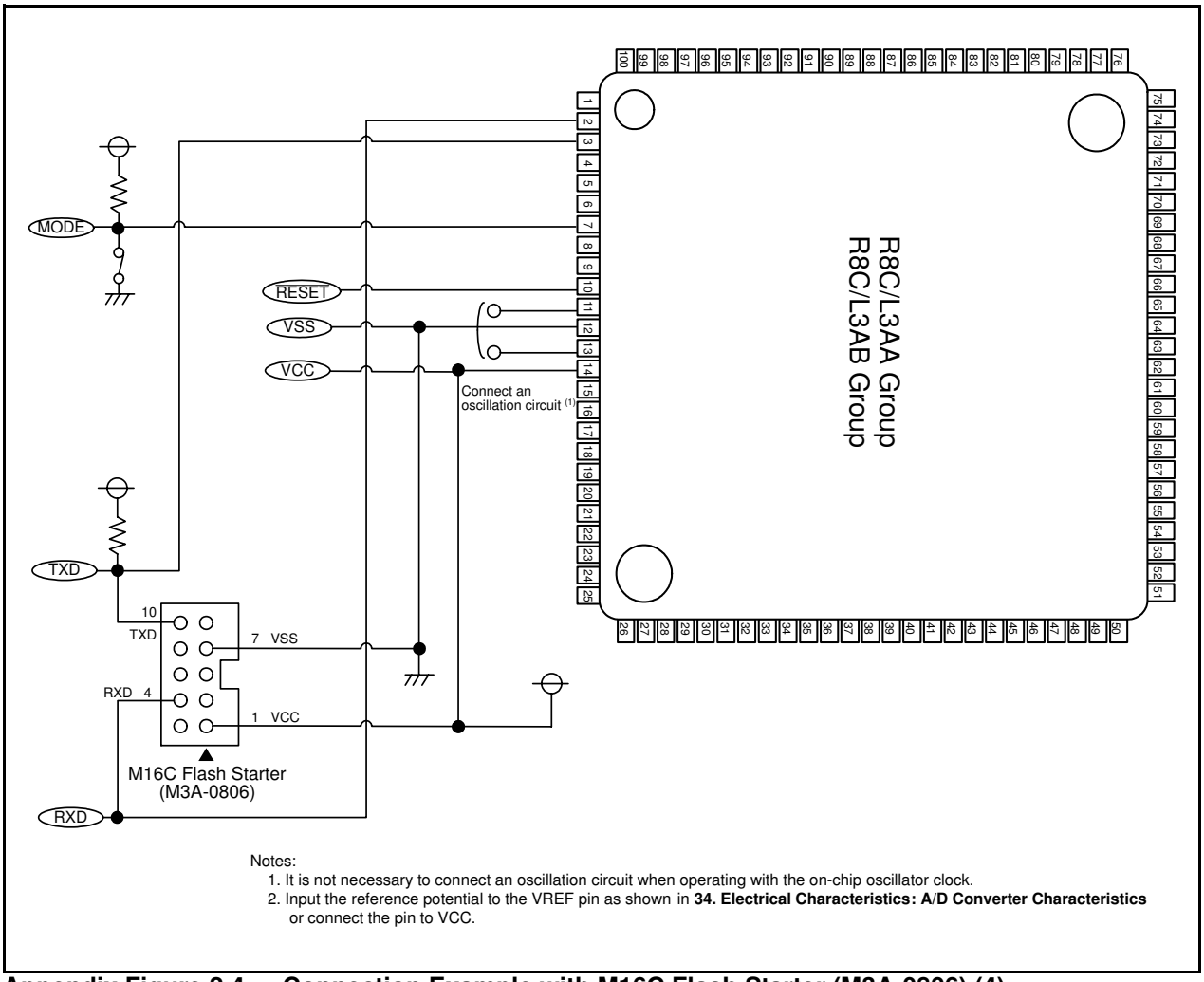


Figure 34.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$



Notes:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.
2. Input the reference potential to the VREF pin as shown in **34. Electrical Characteristics: A/D Converter Characteristics** or connect the pin to VCC.

Appendix Figure 2.4 Connection Example with M16C Flash Starter (M3A-0806) (4)