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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b, 18x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51qm128vlh

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog, $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
VREGIN	Regulator input	–0.3	6.0	V

5 General

5.1 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

5.2 Nonswitching electrical specifications

5.2.1 Voltage and Current Operating Requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage				1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	0.7 × V_{DD}	—	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	0.75 × V_{DD}	—	V	
V_{IL}	Input low voltage				2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.35 × V_{DD}	V	
	• 1.7 V ≤ V_{DD} ≤ 2.7 V	—	0.3 × V_{DD}	V	
I_{IC}	DC injection current — single pin				3
	• V_{IN} > V_{DD}	0	2	mA	
	• V_{IN} < V_{SS}	0	–0.2	mA	
	DC injection current — total MCU limit, includes sum of all stressed pins				3
	• V_{IN} > V_{DD}	0	25	mA	
	• V_{IN} < V_{SS}	0	–5	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. The device always interprets an input as a 1 when the input is greater than or equal to V_{IH} (min.) and less than or equal to V_{IH} (max.), regardless of whether input hysteresis is turned on.
2. The device always interprets an input as a 0 when the input is less than or equal to V_{IL} (max.) and greater than or equal to V_{IL} (min.), regardless of whether input hysteresis is turned on.
3. All functional non-supply pins are internally clamped to VSS and VDD. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values. Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (VIn > VDD) is greater than IDD, the injection current may flow out of VDD and could result in external power supply going out of regulation. Ensure external VDD load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

5.2.2 LVD and POR operating requirements

Table 2. LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

5.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = - 9 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	µA	1
	• @ 25 °C	—	0.1	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	µA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and Mini-FlexBus clocks) = 25 MHz

5.3.1 General Switching Specifications

These general purpose specifications apply to all signals configured for EGPIO, MTIM, CMT, PDB, IRQ, and I^2C signals. The conditions are 50 pf load, V_{DD} = 1.71 V to 3.6 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 9. EGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
G1	Bus clock from CLK_OUT pin high to GPIO output valid	—	32	ns
G2	Bus clock from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
G3	GPIO input valid to bus clock high	28	—	ns
G4	Bus clock from CLK_OUT pin high to GPIO input invalid	—	4	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled) Synchronous path[1]	1.5	—	Bus clock cycles
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) Asynchronous path[2]	100	—	ns
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) Asynchronous path[2]	50	—	ns
	External reset pulse width (digital glitch filter disabled)	100	—	ns
	Mode select (MS) hold time after reset deassertion	2	—	Bus clock cycles

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

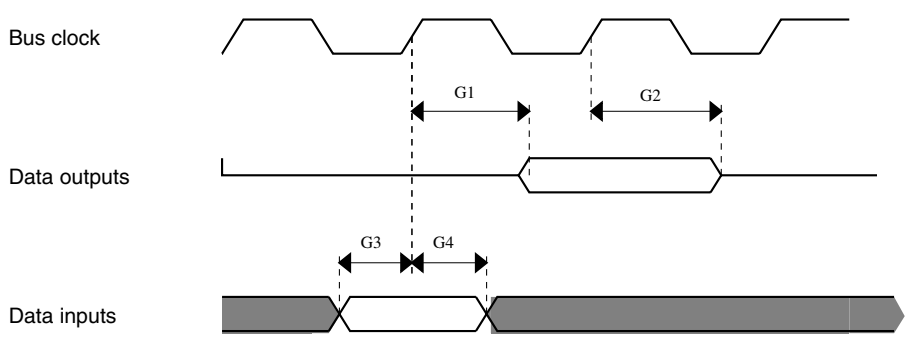


Figure 3. EGPIO timing diagram

5.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	44 Laminate QFN	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	73	79	108	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	54	55	69	33	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	61	66	91	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	48	63	28	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	37	34	44	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	20	31	2.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5.0	4.0	6.0	6.0	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug specifications

Table 12. Background debug mode (BDM) timing

Number	Symbol	Description	Min.	Max.	Unit
1	t_{MSSU}	BKGD/MS setup time after issuing background debug force reset to enter user mode or BDM	500	—	ns
2	t_{MSH}	BKGD/MS hold time after issuing background debug force reset to enter user mode or BDM[1]	100	—	µs

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.4 Memories and memory interfaces

6.4.1 Flash (FTFL) electrical specifications

This section describes the electrical characteristics of the FTFL module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write\_efficiency} \times n_{\text{nvmcycd}}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location
- EEPROM — allocated FlexNVM based on DEPART; entered with Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance

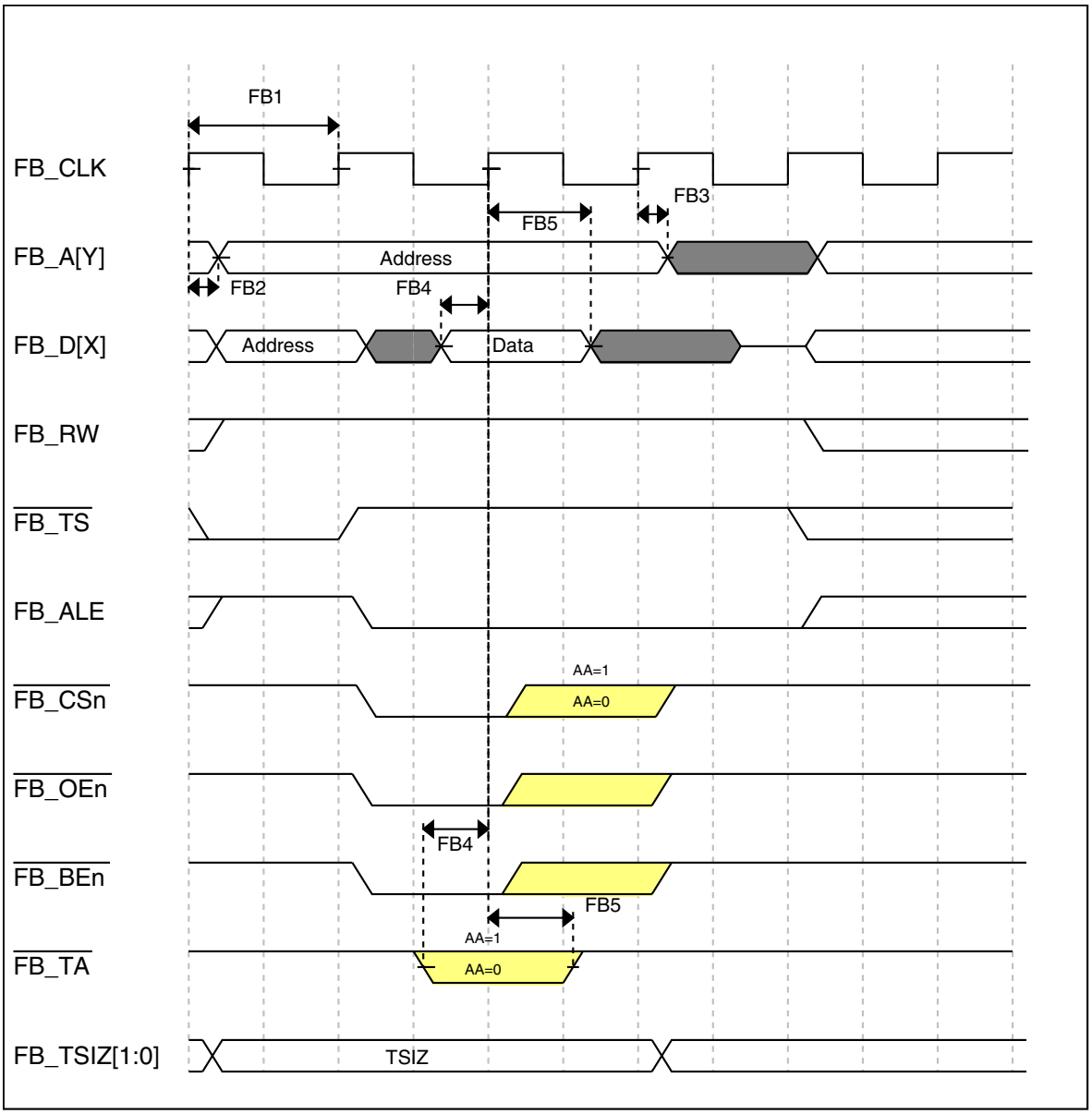


Figure 7. Mini-FlexBus read timing diagram

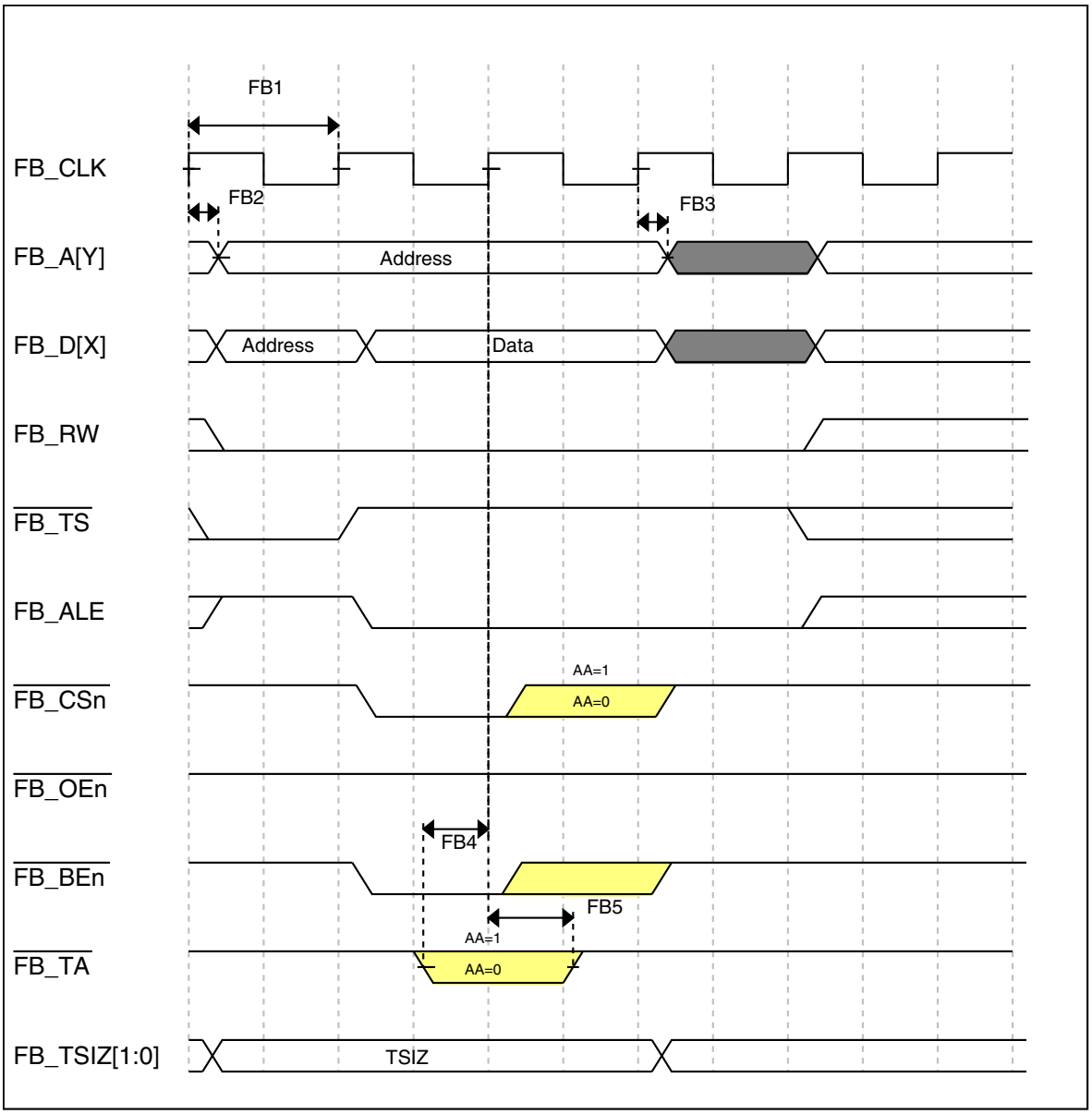


Figure 8. Mini-FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	7
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

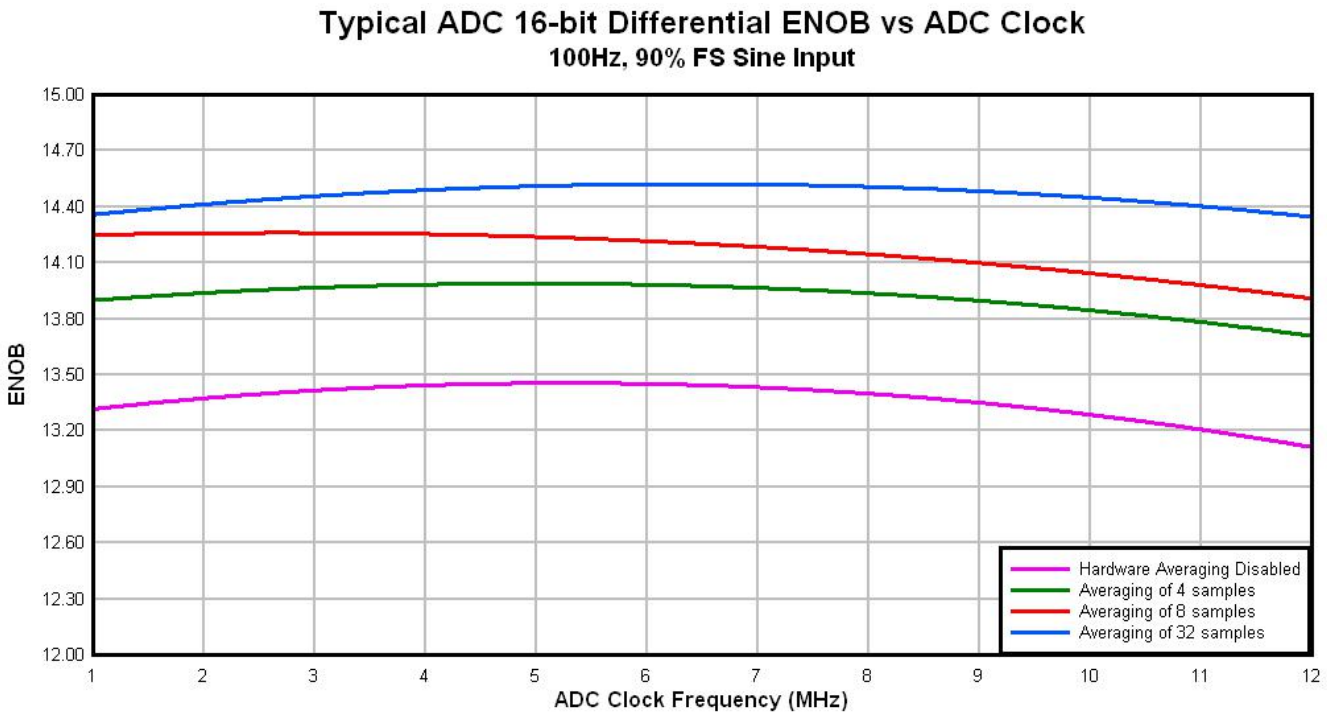


Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode

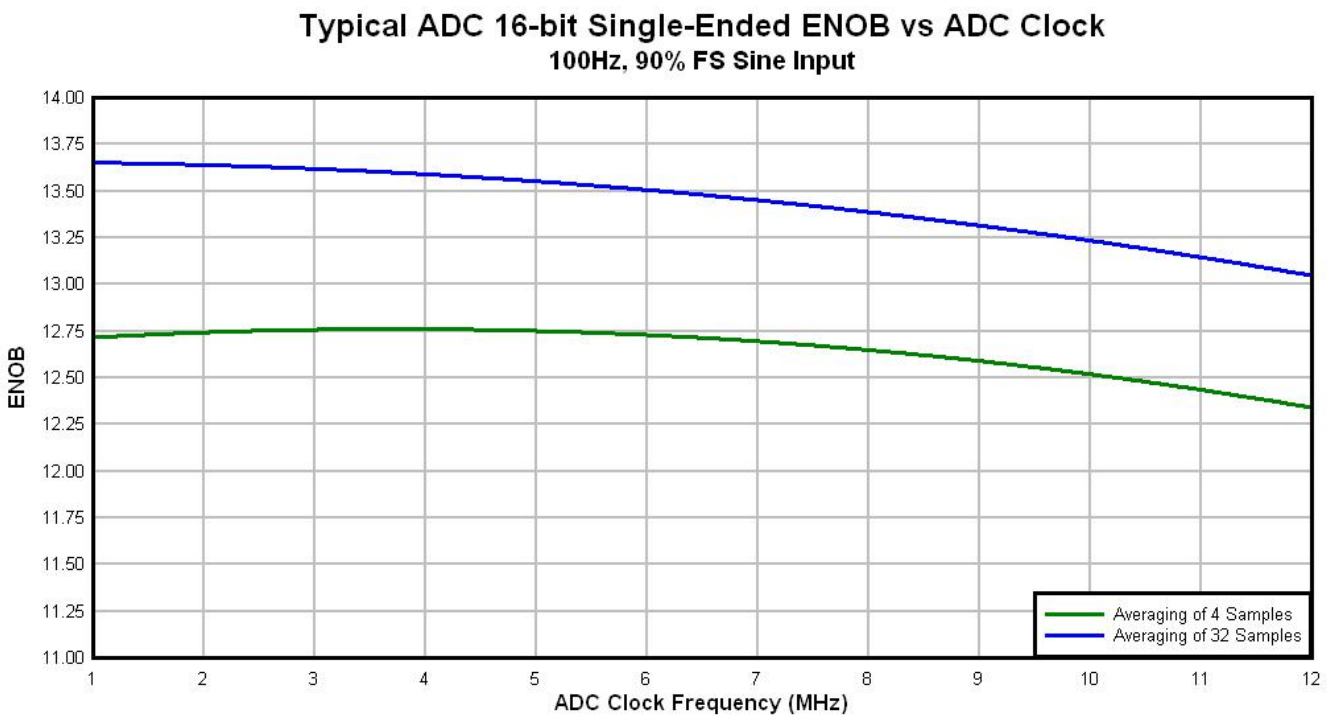


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.2 CMP and 6-bit DAC electrical specifications

Table 25. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

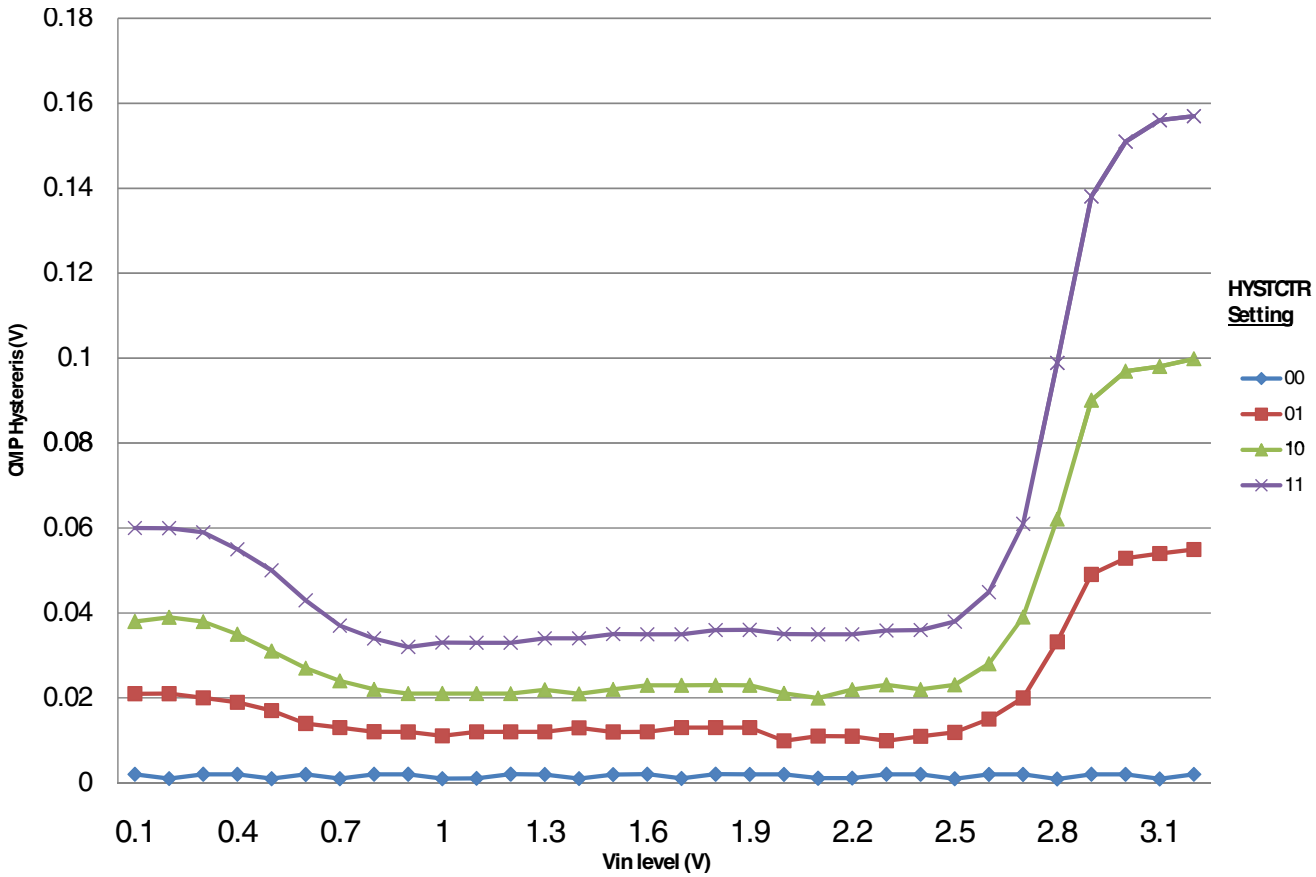


Figure 13. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 26. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

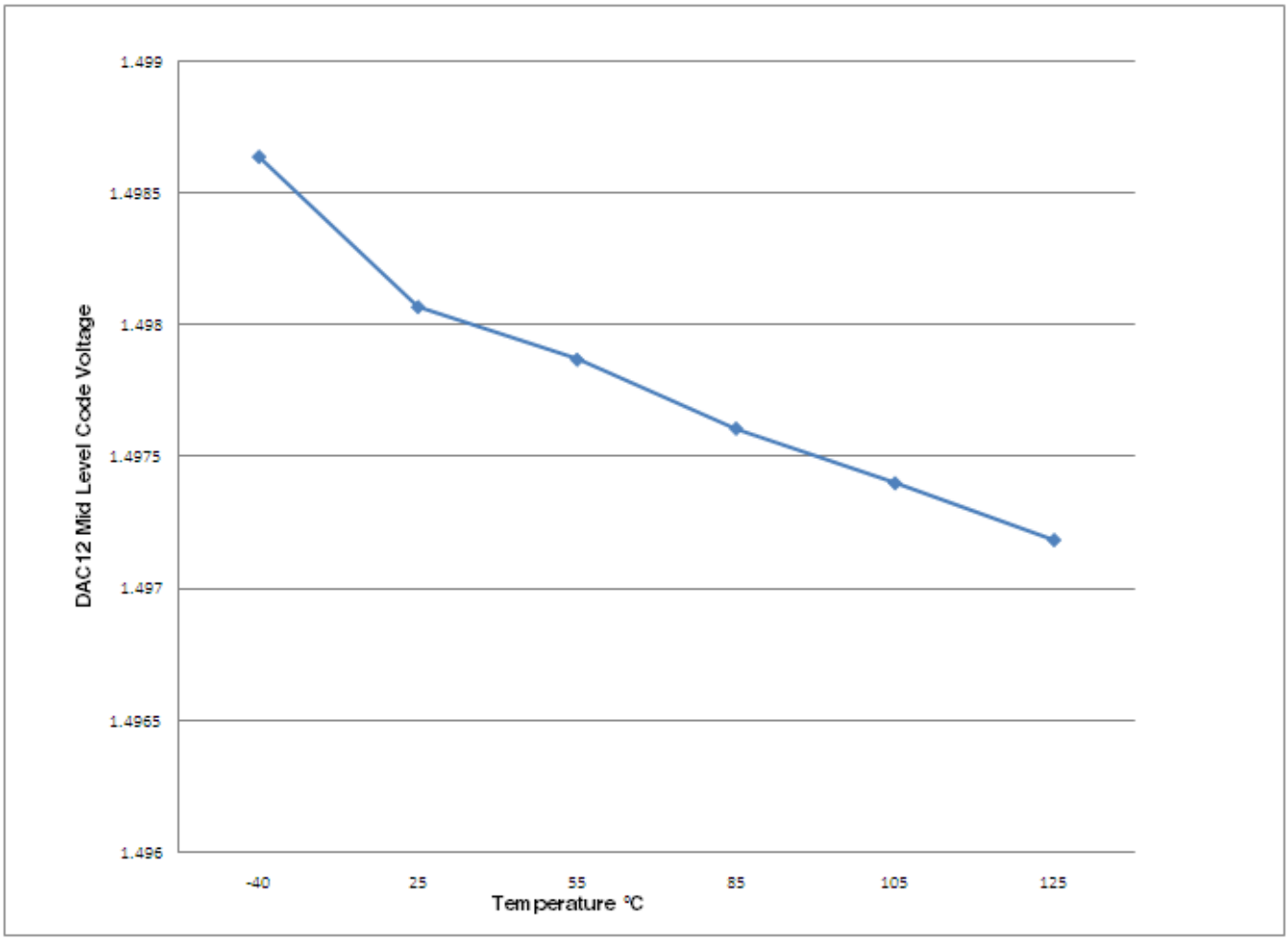


Figure 15. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 28. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	1

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

Table 29. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1965	1.2	1.2027	V	
V_{out}	Voltage reference output with— factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.198	—	1.202	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only (MODE_LV = 00) current	—	—	80	µA	
I_{tr}	Tight-regulation buffer (MODE_LV =10) current	—	—	1.1	mA	
ΔV_{LOAD}	Load regulation (MODE_LV = 10) • current = + 1.0 mA • current = - 1.0 mA	 — —	 2 5	 — —	mV	1
T_{stup}	Buffer startup time	—	—	100	µs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range) (MODE_LV = 10, REGEN = 1)	—	2	—	mV	

1. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 30. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 31. VREF limited-range operating behaviors

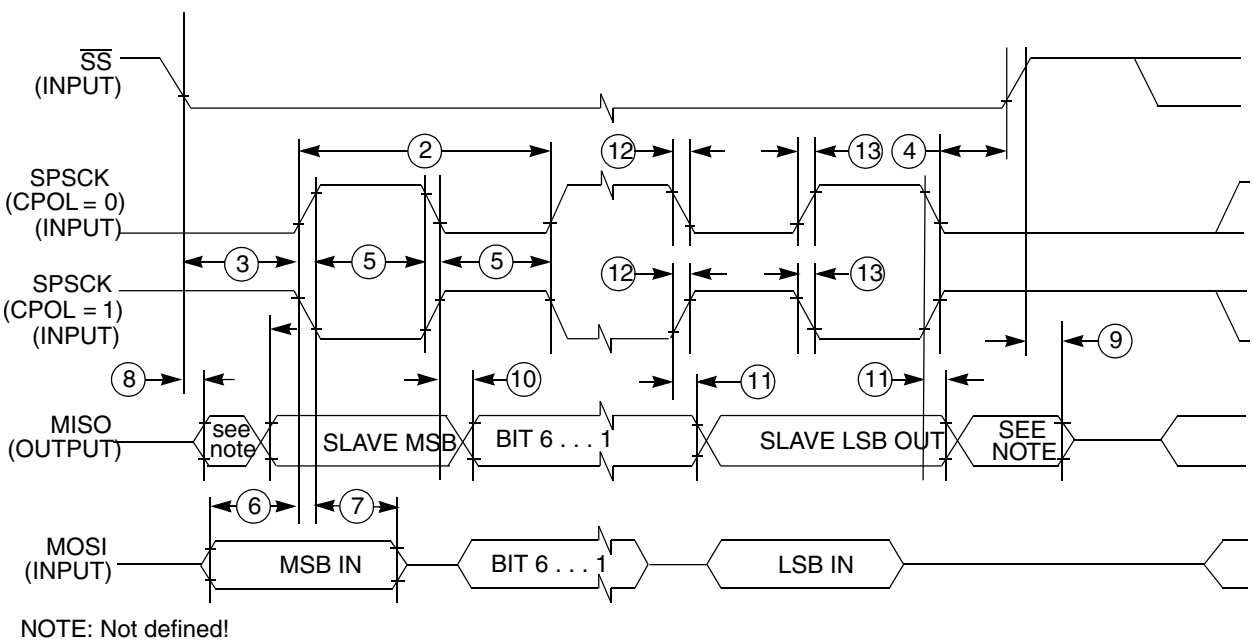
Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General Switching Specifications.

Table 33. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
2	t_{SPSCK}	SPSCK period	4 x t_{BUS}	—	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedanc e state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedanc e state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 18. SPI slave mode timing (CPHA=0)

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
39	27	25	19	PTB2	PTE3
41	29			PTE4	PTE4
42	30			PTE5	PTE5
43				PTE6	PTE6
44	31	27		PTE7	PTE7
PTF					
53				PTF0	PTF0
54				PTF1	PTF1
55				PTF2	PTF2
56	40	36		PTF3	PTF3
58	42	38		PTF4	PTF4
59	43	39		PTF5	PTF5
60	44	40		PTF6	PTF6
61	45	41		PTF7	PTF7
5 V VREG					
22	18	16	13		VOUT33
21	17	15	12		VREGIN
ADC0					
19	15	13	10		ADC0_DP0/ ADC0_SE0
20	16	14	11		ADC0_DM0/ ADC0_SE1
11	7	5	5	PTA4	ADC0_DP1/ ADC0_SE2
12	8	6	6	PTA5	ADC0_DM1/ ADC0_SE3
25	21	19	15	PTA6	ADC0_SE8
26				PTD2	ADC0_SE9
27	22	20		PTD3	ADC0_SE10
28				PTD4	ADC0_SE11
29				PTD5	ADC0_SE12
30	23	21	16	PTA7	ADC0_SE13
31	24	22		PTD6	ADC0_SE14
32				PTD7	ADC0_SE15
38				PTE3	ADC0_SE16
39	27	25	19	PTB2	ADC0_SE17

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
39	27	25	19	PTB2	TSI0_CH13
40	28	26	20	PTB3	TSI0_CH14
41	29			PTE4	TSI0_CH15
PDB0					
44	31	27		PTE7	PDB0_EXTRG
63	47	43	31	PTC4	PDB0_EXTRG
FTM0					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2 / FTM0_QD_PHB
26				PTD2	FTM0_CH0/ FTM0_QD_PHA
27	22	20		PTD3	FTM0_CH1 / FTM0_QD_PHB
30	23	21	16	PTA7	FTM0_QD_PHA
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
FTM1					
34				PTE1	FTM_FLT0
25	21	19	15	PTA6	FTM_FLT1
36	26	24	18	PTB1	FTM_FLT2
7	3	1	1	PTA0	FTM1_CH0
8	4	2	2	PTA1	FTM1_CH1
9	5	3	3	PTA2	FTM1_CH2
10	6	4	4	PTA3	FTM1_CH3
11	7	5	5	PTA4	FTM1_CH4
12	8	6	6	PTA5	FTM1_CH5
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
MTIM					
51	38	34	27	PTC0	TMR_CLKIN0
50	37	33	26	PTB7	TMR_CLKIN1
Mini-FlexBus					
36	26	24	18	PTB1	FB_CLKOUT
27	22	20		PTD3	FBa_AD0

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
41	29			PTE4	FBa_AD1
42	30			PTE5	FBa_AD2
43				PTE6	FBa_AD3
44	31	27		PTE7	FBa_AD4
53				PTF0	FBa_AD5
54				PTF1	FBa_AD6
55				PTF2	FBa_AD7
56	40	36		PTF3	FBa_AD8
60	44	40		PTF6	FBa_AD9
61	45	41		PTF7	FBa_AD10
3				PTC6	FBa_AD11
4				PTC7	FBa_AD12
5	1			PTD0	FBa_AD13
6	2			PTD1	FBa_AD14
7	3	1	1	PTA0	FBa_AD15
8	4	2	2	PTA1	FBa_AD16
25	21	19	15	PTA6	FBa_AD17
57	41	37	29	PTC2	FBa_AD18
58	42	38		PTF4	FBa_AD19
40	28	26	20	PTB3	FBa_ALE
39	27	25	19	PTB2	FBa_CS0_b
37				PTE2	FBa_D0
34				PTE1	FBa_D1
33				PTE0	FBa_D2
32				PTD7	FBa_D3
31	24	22		PTD6	FBa_D4
30	23	21	16	PTA7	FBa_D5
29				PTD5	FBa_D6
28				PTD4	FBa_D7
38				PTE3	FBa_OE_b
59	43	39		PTF5	FBa_RW_b
DATA_BUS					
8	4	2	2	PTA1	FBa_AD16
39	27	25	19	PTB2	FBa_CS0_b
61	45	41		PTF7	FBa_D0

Table continues on the next page...