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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b, 18x16b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51qm128vlhr

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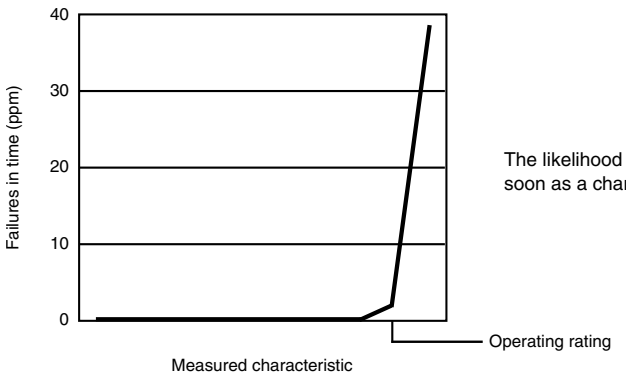
3.4.1 Example

This is an example of an operating rating:

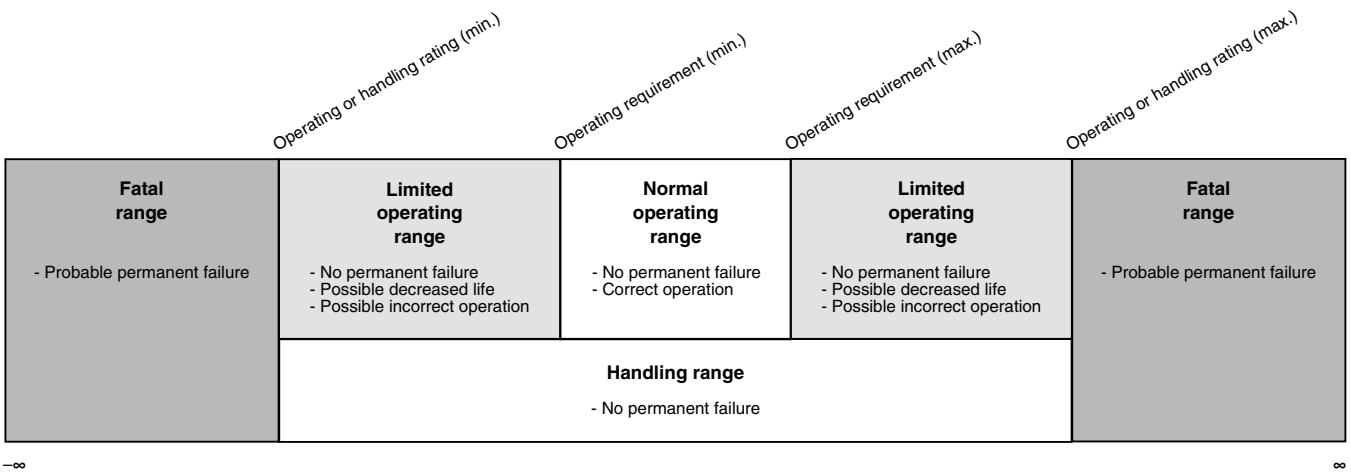
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

5.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = - 9 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	µA	1
	• @ 25 °C	—	0.1	µA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	µA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx-RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock (and flash and Mini-FlexBus clocks) = 25 MHz

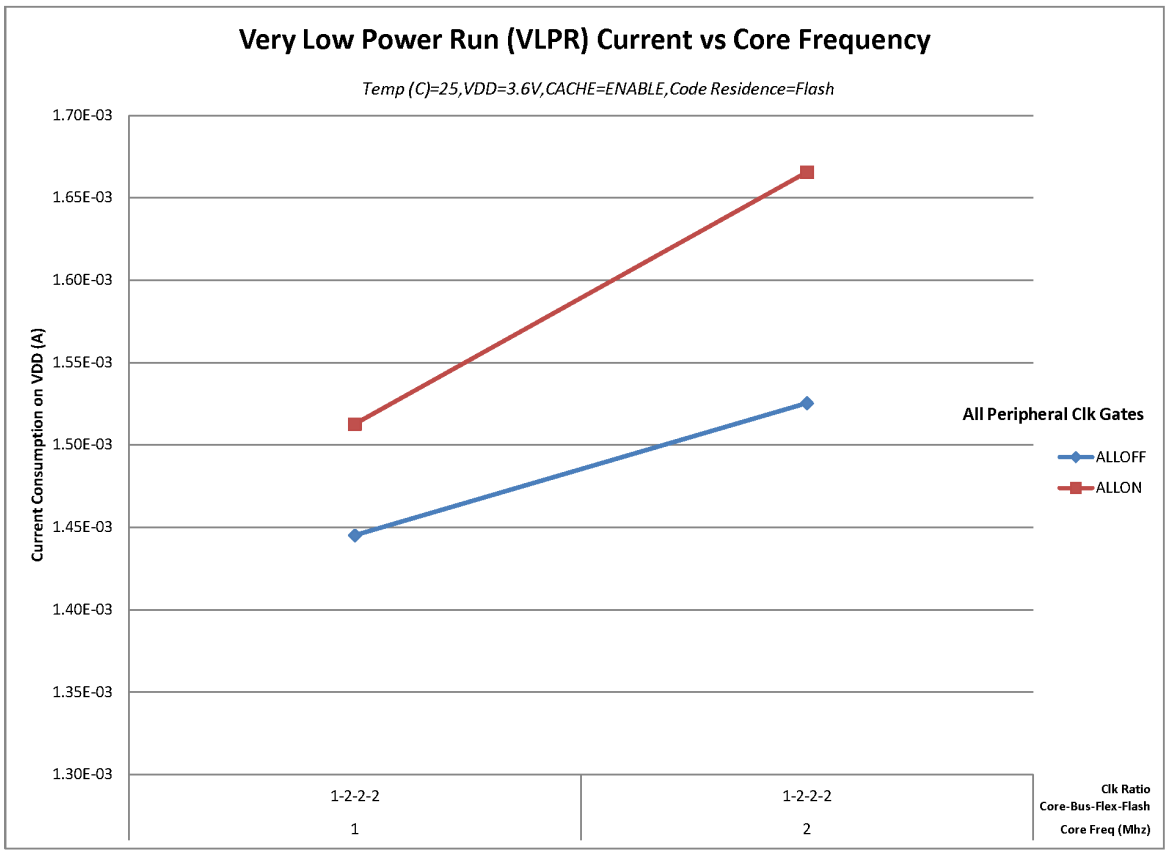


Figure 2. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	19		
V_{RE3}	Radiated emissions voltage, band 3	150–500	17		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16		
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

2. V_{DD} = 3 V, T_A = 25 °C, f_{OSC} = 32 kHz (crystal), f_{BUS} = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching electrical specifications

Table 8. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus clock	—	25	MHz	
FB_CLK	Mini-FlexBus clock	—	25	MHz	1
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	2	MHz	
f_{BUS}	Bus clock	—	1	MHz	
FB_CLK	Mini-FlexBus clock	—	1	MHz	1
f_{LPTMR}	LPTMR clock[2]	—	25	MHz	

1. When the Mini-FlexBus is enabled, its clock frequency is always the same as the bus clock frequency.
2. A maximum frequency of 25 MHz for the LPTMR in VLPR mode is possible when the LPTMR is configured for pulse counting mode and is driven externally via the LPTMR_ALT1, LPTMR_ALT2, or LPTMR_ALT3 pin.

6.3 Clock modules

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 10	—	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 1.0	± 4.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	3.3	4	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	

Table continues on the next page...

Table 18. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	µs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash (FTFL) current and power specfications

Table 19. Flash (FTFL) current and power specfications

Symbol	Description	Typ.	Unit
I_{DD_PGM}	Worst case programming current in program flash	10	mA

Table 22. Flexbus switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB2	Address, data, and control output valid	—	20	ns	1
FB3	Address, data, and control output hold	1	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	20	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	10	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_CS}}n$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0].

Note

The following diagrams refer to signal names that may not be included on your particular device. Ignore these extraneous signals.

Also, ignore the AA=0 portions of the diagrams because this setting is not supported in the Mini-FlexBus.

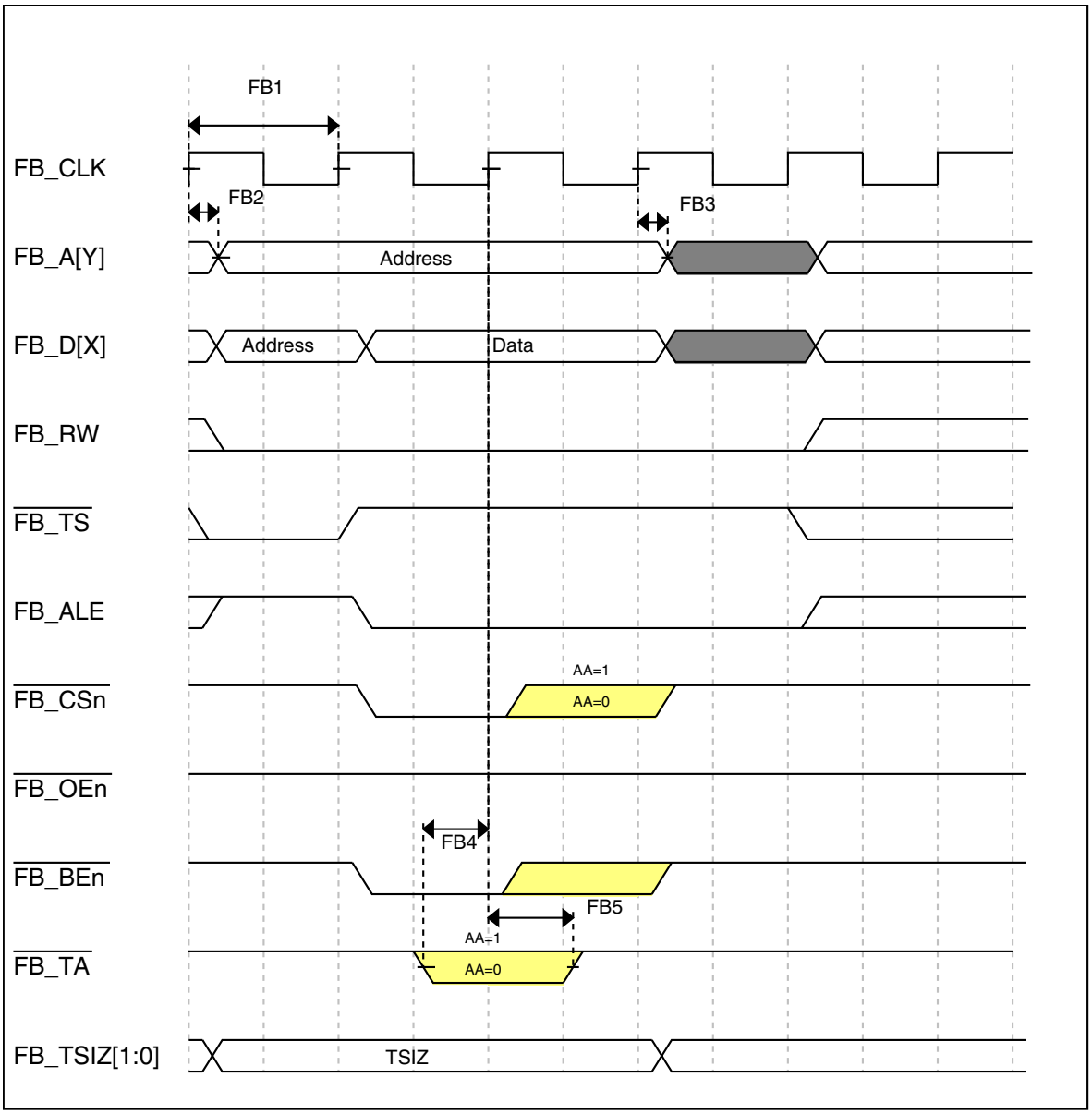


Figure 8. Mini-FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32	82	95	—	dB	7
		16 bit single-ended mode • Avg=32	78	90	—	dB	
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	719	—	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

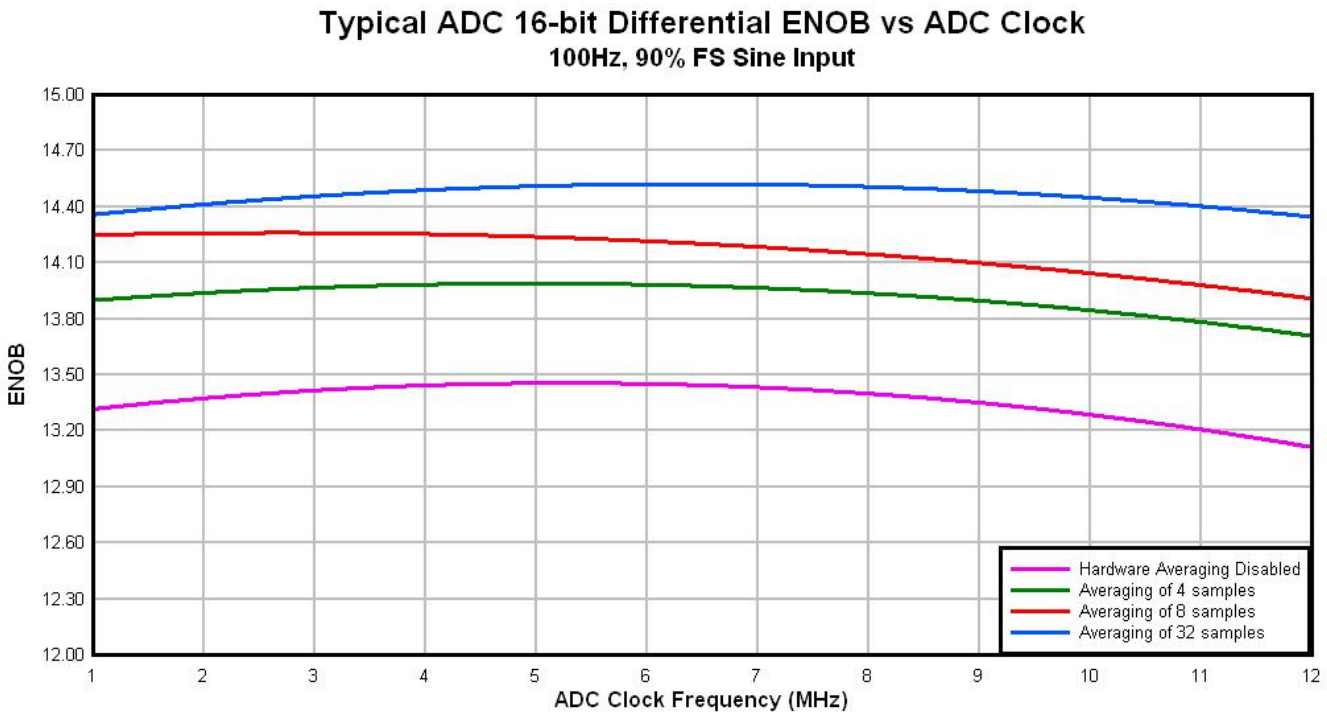


Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode

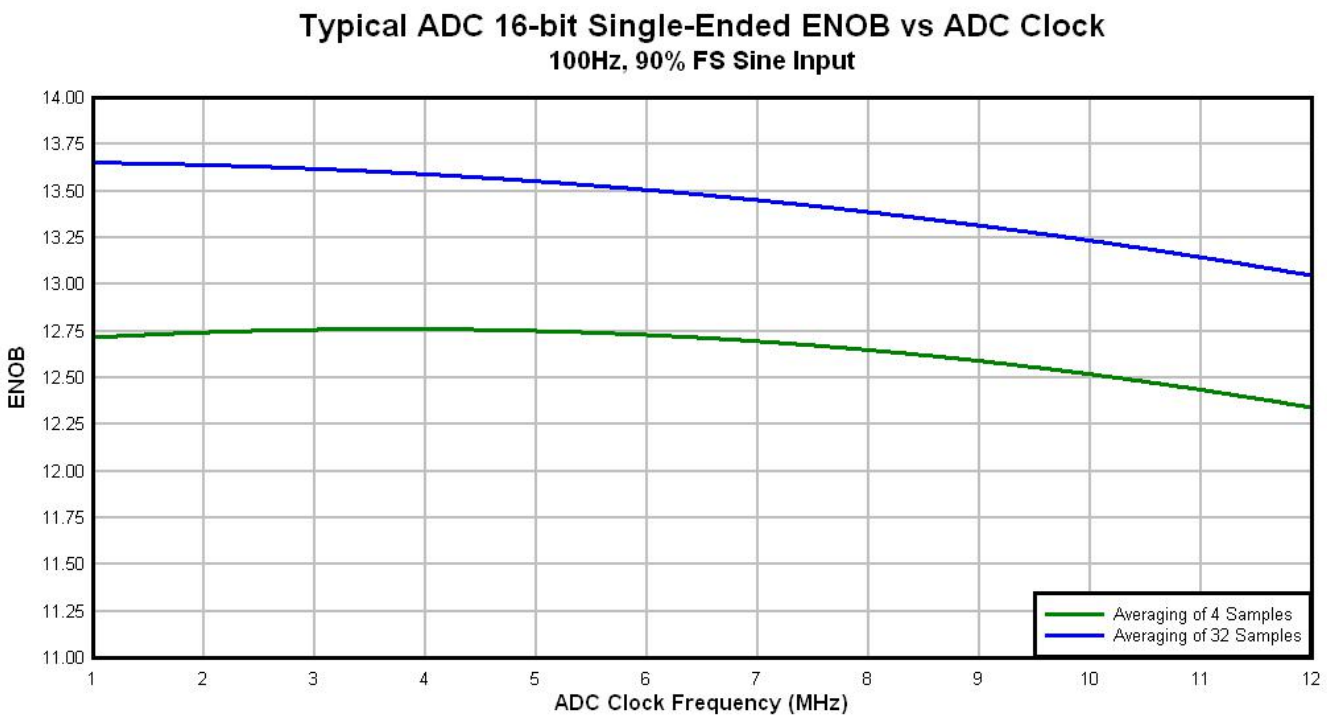


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.2 CMP and 6-bit DAC electrical specifications

Table 25. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

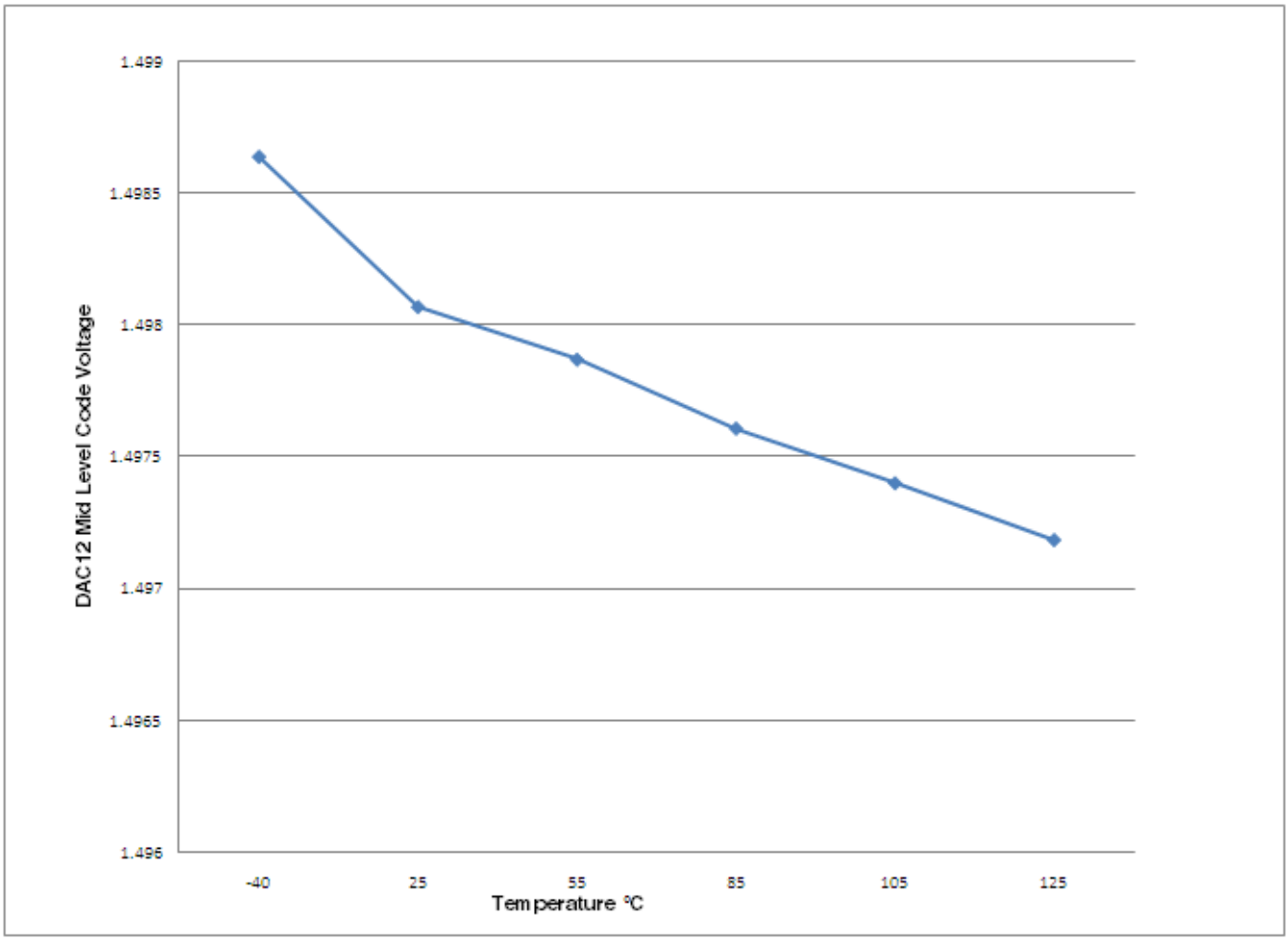


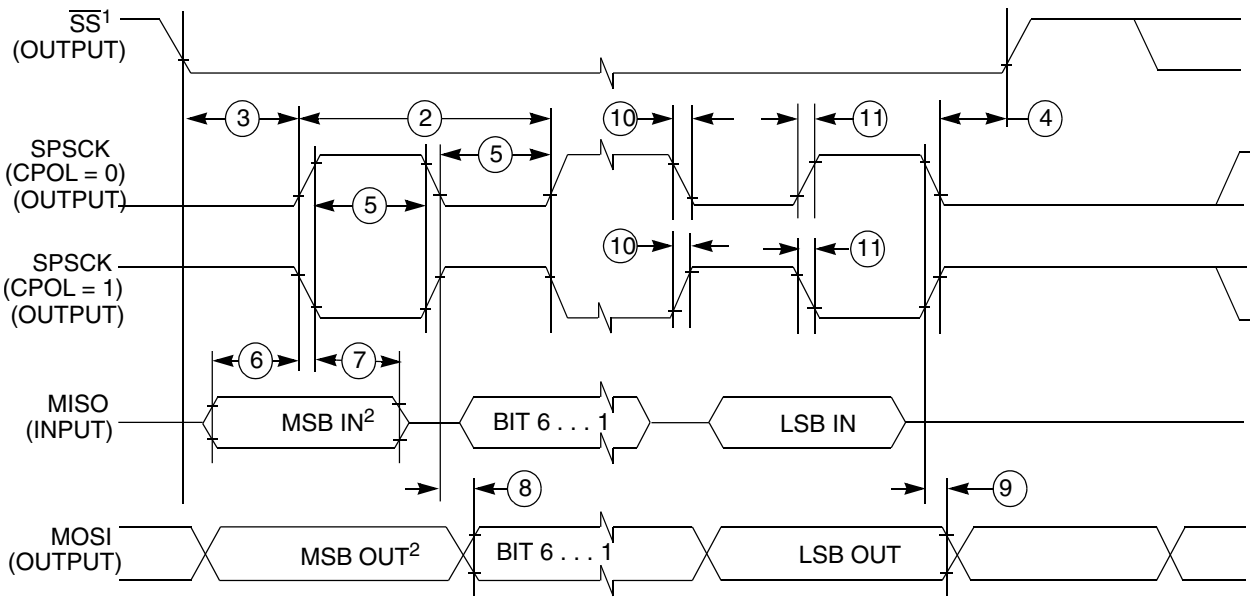
Figure 15. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 28. VREF full-range operating requirements

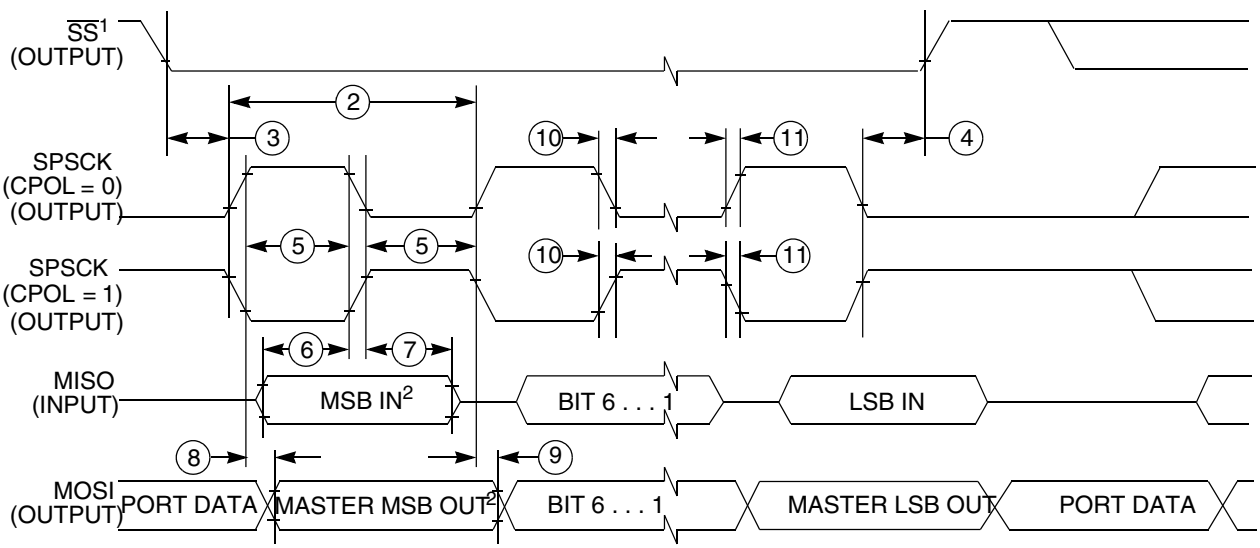
Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	1

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI master mode timing (CPHA=0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=1)

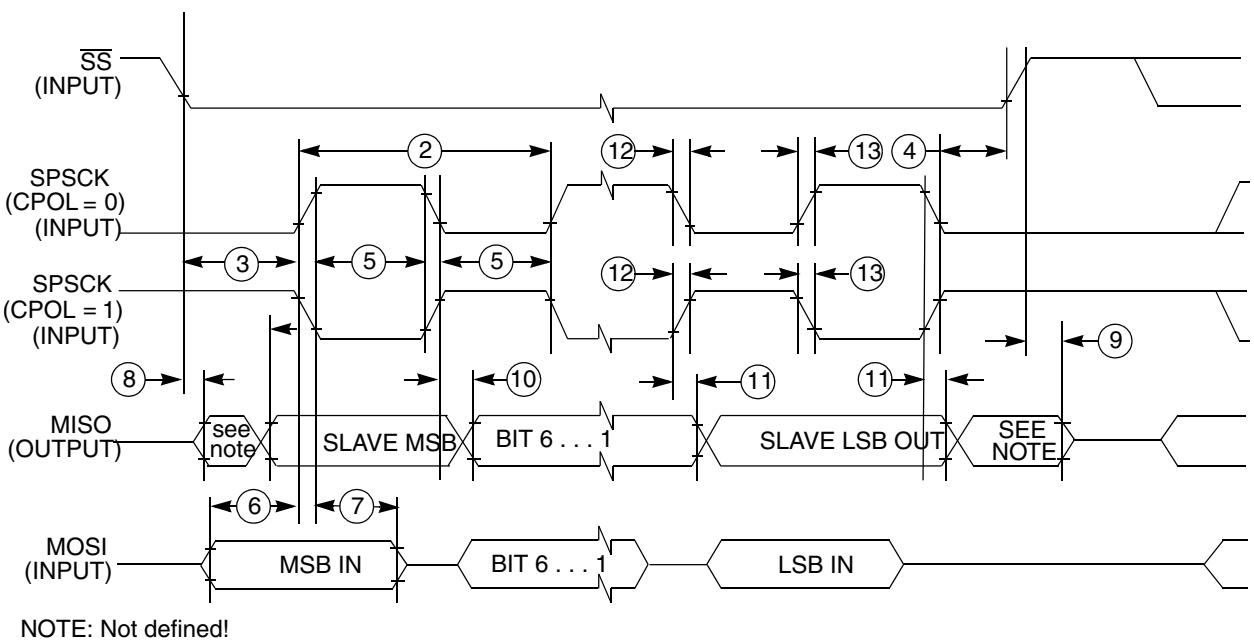
Table 33. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{BUS}/4$	Hz	f_{BUS} is the bus clock as defined in Table 8.

Table continues on the next page...

Table 33. SPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
2	t_{SPSCK}	SPSCK period	4 x t_{BUS}	—	ns	t_{BUS} = 1/ f_{BUS}
3	t_{Lead}	Enable lead time	1	—	t_{BUS}	—
4	t_{Lag}	Enable lag time	1	—	t_{BUS}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{BUS} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	19.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_a	Slave access time	—	t_{BUS}	ns	Time to data active from high-impedanc e state
9	t_{dis}	Slave MISO disable time	—	t_{BUS}	ns	Hold time to high-impedanc e state
10	t_v	Data valid (after SPSCK edge)	—	27	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{BUS} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



NOTE: Not defined!

Figure 18. SPI slave mode timing (CPHA=0)

8 Pinout

8.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Mux Control module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- On PTB0, EZP_MS_b is active only during reset. Refer to the detailed boot description.
- PTC1 is open drain.

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	—	—	—	VDD	VDD								
2	—	—	—	VSS	VSS								
3	—	—	—	Disabled	Disabled	PTC6	UART0_TX	I2C0_SCL	RGPIO6	SPI1_MOSI	FBa_AD11		
4	—	—	—	Disabled	Disabled	PTC7	UART0_RX	I2C0_SDA	RGPIO7	SPI1_MISO	FBa_AD12		
5	1	—	—	Disabled	Disabled	PTD0	UART0_CTS_b	I2C1_SDA	RGPIO8	SPI1_SCLK	FBa_AD13		
6	2	—	—	Disabled	Disabled	PTD1	UART0_RTS_b	I2C1_SCL	RGPIO9	SPI1_SS	FBa_AD14		
7	3	1	1	Disabled	Disabled	PTA0		I2C2_SCL	FTM1_CH0	SPI0_SS	FBa_AD15		
8	4	2	2	Disabled	Disabled	PTA1		I2C2_SDA	FTM1_CH1		FBa_AD16		
9	5	3	3	Disabled	Disabled	PTA2	UART1_TX		FTM1_CH2	SPI1_SS			
10	6	4	4	Disabled	Disabled	PTA3	UART1_RX		FTM1_CH3	SPI1_SCLK			EZP_CLK
11	7	5	5	ADC0_DP1/ ADC0_SE2	ADC0_DP1/ ADC0_SE2	PTA4	UART1_CTS_b	I2C2_SCL	FTM1_CH4	SPI1_MISO			EZP_DI
12	8	6	6	ADC0_DM1/ ADC0_SE3	ADC0_DM1/ ADC0_SE3	PTA5	UART1_RTS_b	I2C2_SDA	FTM1_CH5	SPI1_MOSI	CLKOUT		EZP_DO
13	9	7	7	VDDA	VDDA								
14	10	8	—	VREFH	VREFH								
15	11	9	—	VREF_OUT	VREF_OUT								
16	12	10	—	VREFL	VREFL								
17	13	11	8	VSSA	VSSA								
18	14	12	9	DAC0_OUT	DAC0_OUT								
19	15	13	10	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0								
20	16	14	11	ADC0_DM0/ ADC0_SE1	ADC0_DM0/ ADC0_SE1								
21	17	15	12	VREGIN	VREGIN								
22	18	16	13	VOUT33	VOUT33								

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
23	19	17	14	VSS	VSS								
24	20	18	—	VDD	VDD								
25	21	19	15	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTA6		LPTMR_ALT1	FTM_FLT1	FBa_D7	FBa_AD17		
26	—	—	—	ADC0_SE9/ TSI0_CH1	ADC0_SE9/ TSI0_CH1	PTD2	FTM0_QD_PHA	RGPIO10	FTM0_CH0				
27	22	20	—	ADC0_SE10/TSI0_CH2	ADC0_SE10/TSI0_CH2	PTD3	FTM0_QD_PHB	RGPIO11	FTM0_CH1	FBa_D6	FBa_AD0		
28	—	—	—	ADC0_SE11/TSI0_CH3	ADC0_SE11/TSI0_CH3	PTD4		RGPIO12			FBa_D7		
29	—	—	—	ADC0_SE12/TSI0_CH4	ADC0_SE12/TSI0_CH4	PTD5		RGPIO13			FBa_D6		
30	23	21	16	ADC0_SE13/TSI0_CH5	ADC0_SE13/TSI0_CH5	PTA7	UART0_TX		FTM0_QD_PHA		FBa_D5		
31	24	22	—	ADC0_SE14/TSI0_CH6	ADC0_SE14/TSI0_CH6	PTD6	UART0_RX	RGPIO14			FBa_D4		
32	—	—	—	ADC0_SE15/TSI0_CH7	ADC0_SE15/TSI0_CH7	PTD7	UART0_CTS_b	I2C3_SCL	RGPIO15		FBa_D3		
33	—	—	—	TSI0_CH8	TSI0_CH8	PTE0	UART0_RTS_b	I2C3_SDA			FBa_D2		
34	—	—	—	TSI0_CH9	TSI0_CH9	PTE1	SPI0_SS		FTM_FLT0		FBa_D1		
35	25	23	17	IRQ/ EZP_MS_b	Disabled	PTB0		I2C0_SCL		IRQ/ EZP_MS_b			EZP_CS_b
36	26	24	18	TSI0_CH10	TSI0_CH10	PTB1	SPI0_SCLK	I2C0_SDA	FTM_FLT2	LPTMR_ALT2	FTM0_QD_PHB	FB_CLKOUT	
37	—	—	—	TSI0_CH11	TSI0_CH11	PTE2		I2C3_SCL			FBa_D0		
38	—	—	—	ADC0_SE16/ TSI0_CH12	ADC0_SE16/ TSI0_CH12	PTE3	SPI0_MOSI	I2C3_SDA			FBa_OE_b		
39	27	25	19	ADC0_SE17/ TSI0_CH13	ADC0_SE17/ TSI0_CH13	PTB2	SPI0_MISO				FBa_CS0_b		
40	28	26	20	ADC0_SE18/ TSI0_CH14	ADC0_SE18/ TSI0_CH14	PTB3	SPI0_MOSI			FBa_CS1_b	FBa_ALE		
41	29	—	—	ADC0_SE19/ TSI0_CH15	ADC0_SE19/ TSI0_CH15	PTE4	UART0_RTS_b	LPTMR_ALT3	SPI1_SS		FBa_AD1		
42	30	—	—	ADC0_SE20	ADC0_SE20	PTE5	UART0_CTS_b	I2C1_SCL	SPI1_SCLK		FBa_AD2		
43	—	—	—	ADC0_SE21	ADC0_SE21	PTE6	UART0_RX	I2C1_SDA	SPI1_MISO		FBa_AD3		
44	31	27	—	ADC0_SE22	ADC0_SE22	PTE7	UART0_TX	PDB0_EXTRG	SPI1_MOSI	FBa_RW_b	FBa_AD4		
45	32	28	21	BKGD/MS	Disabled	PTB4	BKGD/MS						
46	33	29	22	XTAL2	XTAL2	PTB5							
47	34	30	23	EXTAL2	EXTAL2	PTB6							

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
48	35	31	24		VDD
2					VSS
23	19	17	14		VSS
49	36	32	25		VSS
System					
45	32	28	21	PTB4	BKGD/MS
12	8	6	6	PTA5	CLKOUT
62	46	42	30	PTC3	CLKOUT
10	6	4	4	PTA3	EZP_CLK
11	7	5	5	PTA4	EZP_DI
12	8	6	6	PTA5	EZP_DO
35	25	23	17	PTB0	IRQ/EZP_MS_b, EZP_CS_b
52	39	35	28	PTC1	RESET_b
OSC					
50	37	33	26	PTB7	EXTAL1
47	34	30	23	PTB6	EXTAL2
51	38	34	27	PTC0	XTAL1
46	33	29	22	PTB5	XTAL2
LLWU					
4				PTC7	LLWU_P0
6	2			PTD1	LLWU_P1
12	8	6	6	PTA5	LLWU_P2
30	23	21	16	PTA7	LLWU_P3
32				PTD7	LLWU_P4
35	25	23	17	PTB0	LLWU_P5
36	26	24	18	PTB1	LLWU_P6
39	27	25	19	PTB2	LLWU_P7
44	31	27		PTE7	LLWU_P8
45	32	28	21	PTB4	LLWU_P9
55				PTF2	LLWU_P10
56	40	36		PTF3	LLWU_P11
57	41	37	29	PTC2	LLWU_P12
59	43	39		PTF5	LLWU_P13
62	46	42	30	PTC3	LLWU_P14

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
63	47	43	31	PTC4	LLWU_P15
RGPIO					
51	38	34	27	PTC0	RGPIO0
56	40	36		PTF3	RGPIO1
57	41	37	29	PTC2	RGPIO2
62	46	42	30	PTC3	RGPIO3
63	47	43	31	PTC4	RGPIO4
64	48	44	32	PTC5	RGPIO5
3				PTC6	RGPIO6
4				PTC7	RGPIO7
5	1			PTD0	RGPIO8
6	2			PTD1	RGPIO9
26				PTD2	RGPIO10
27	22	20		PTD3	RGPIO11
28				PTD4	RGPIO12
29				PTD5	RGPIO13
31	24	22		PTD6	RGPIO14
32				PTD7	RGPIO15
LPTMR					
25	21	19	15	PTA6	LPTMR_ALT1
36	26	24	18	PTB1	LPTMR_ALT2
41	29			PTE4	LPTMR_ALT3
LPTMR-TOD					
50	37	33	26	PTB7	EXTAL1
47	34	30	23	PTB6	EXTAL2
25	21	19	15	PTA6	LPTMR_ALT1
36	26	24	18	PTB1	LPTMR_ALT2
41	29			PTE4	LPTMR_ALT3
51	38	34	27	PTC0	XTAL1
46	33	29	22	PTB5	XTAL2
PTA					
7	3	1	1	PTA0	PTA0
8	4	2	2	PTA1	PTA1
9	5	3	3	PTA2	PTA2
10	6	4	4	PTA3	PTA3

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
39	27	25	19	PTB2	PTE3
41	29			PTE4	PTE4
42	30			PTE5	PTE5
43				PTE6	PTE6
44	31	27		PTE7	PTE7
PTF					
53				PTF0	PTF0
54				PTF1	PTF1
55				PTF2	PTF2
56	40	36		PTF3	PTF3
58	42	38		PTF4	PTF4
59	43	39		PTF5	PTF5
60	44	40		PTF6	PTF6
61	45	41		PTF7	PTF7
5 V VREG					
22	18	16	13		VOUT33
21	17	15	12		VREGIN
ADC0					
19	15	13	10		ADC0_DP0/ ADC0_SE0
20	16	14	11		ADC0_DM0/ ADC0_SE1
11	7	5	5	PTA4	ADC0_DP1/ ADC0_SE2
12	8	6	6	PTA5	ADC0_DM1/ ADC0_SE3
25	21	19	15	PTA6	ADC0_SE8
26				PTD2	ADC0_SE9
27	22	20		PTD3	ADC0_SE10
28				PTD4	ADC0_SE11
29				PTD5	ADC0_SE12
30	23	21	16	PTA7	ADC0_SE13
31	24	22		PTD6	ADC0_SE14
32				PTD7	ADC0_SE15
38				PTE3	ADC0_SE16
39	27	25	19	PTB2	ADC0_SE17

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