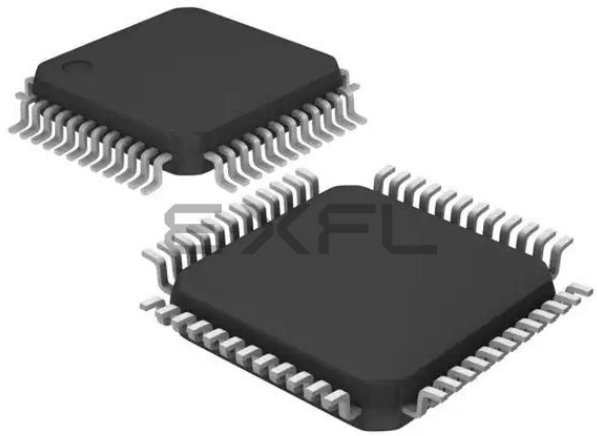

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 14x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf51qm64vlf

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device:

1. Go to http://www.freescale.com.
2. Perform a part number search for the following partial device numbers: PCF51QM and MCF51QM.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q CCCC DD MMM T PP

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
CCCC	Core code	CF51 = ColdFire V1
DD	Device number	JF, JU, QF, QH, QM, QU

Table continues on the next page...

Field	Description	Values
MMM	Memory size (program flash memory)[1]	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB
T	Temperature range, ambient (°C)	V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • HS = 44 Laminate QFN (5 mm x 5 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)

1. All parts also have FlexNVM, FlexRAM, and RAM.

2.4 Example

This is an example part number:

MCF51QM128VLH

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

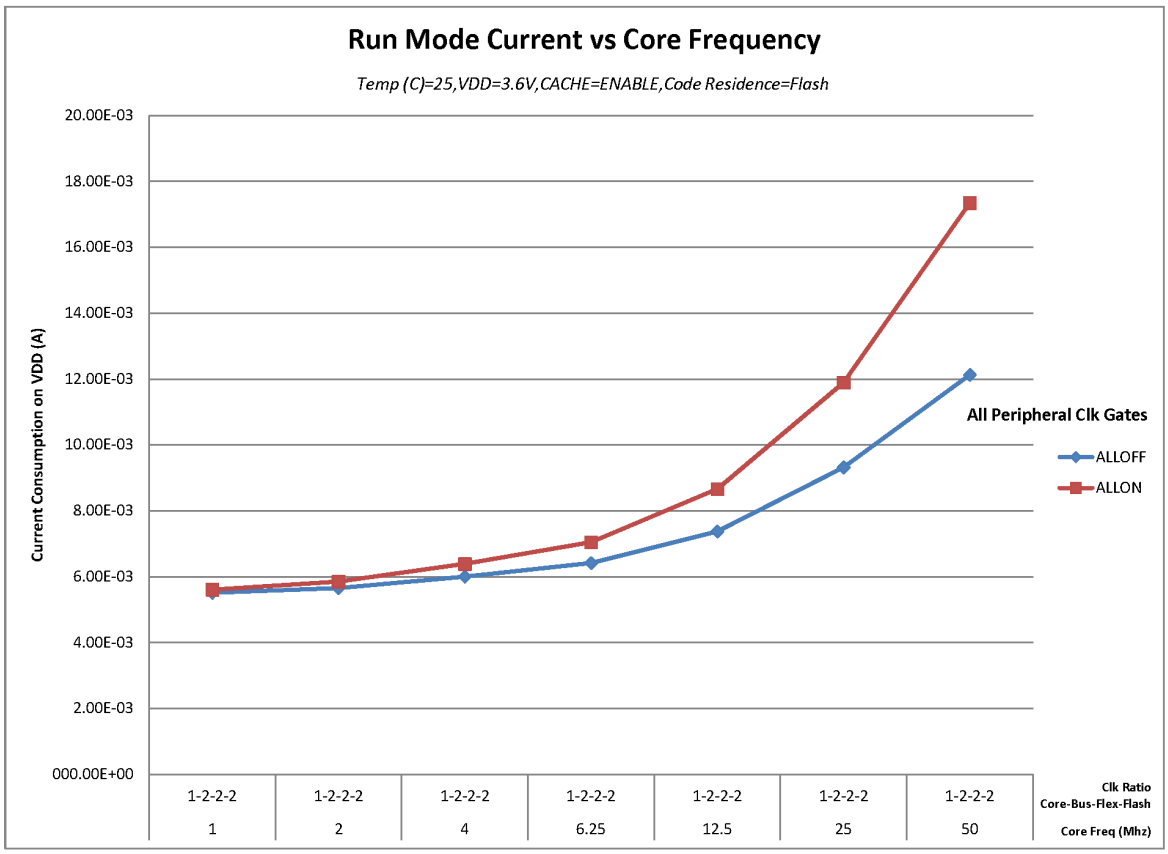

Figure 1. Run mode supply current vs. core frequency

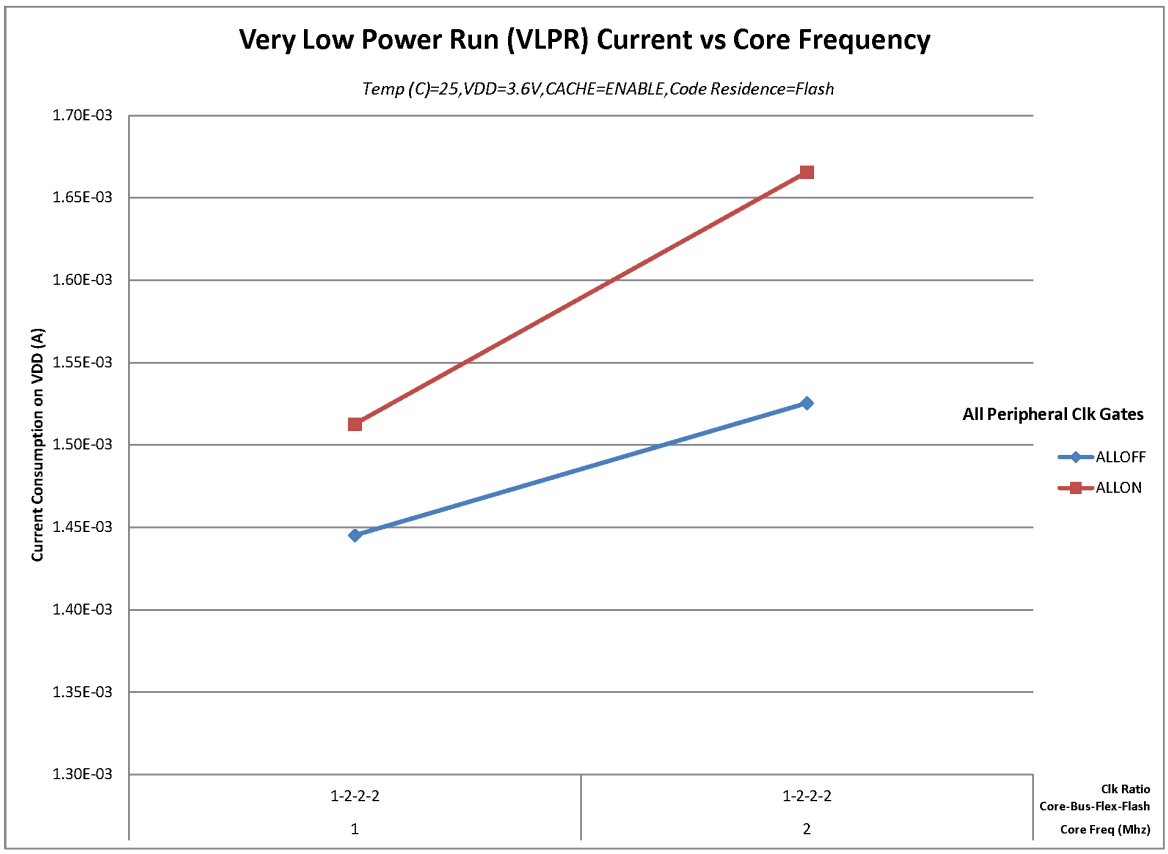

Figure 2. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 6. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	19		
V_{RE3}	Radiated emissions voltage, band 3	150–500	17		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	16		
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

2. V_{DD} = 3 V, T_A = 25 °C, f_{OSC} = 32 kHz (crystal), f_{BUS} = 24 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*.

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching electrical specifications

Table 8. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus clock	—	25	MHz	
FB_CLK	Mini-FlexBus clock	—	25	MHz	1
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode					
f_{SYS}	System and core clock	—	2	MHz	
f_{BUS}	Bus clock	—	1	MHz	
FB_CLK	Mini-FlexBus clock	—	1	MHz	1
f_{LPTMR}	LPTMR clock[2]	—	25	MHz	

1. When the Mini-FlexBus is enabled, its clock frequency is always the same as the bus clock frequency.
2. A maximum frequency of 25 MHz for the LPTMR in VLPR mode is possible when the LPTMR is configured for pulse counting mode and is driven externally via the LPTMR_ALT1, LPTMR_ALT2, or LPTMR_ALT3 pin.

The following general purpose specifications apply to all signals configured for RGPIO, FTM, and UART. The conditions are 25 pf load, V_{DD} = 3.6 V to 1.71 V, and full temperature range. The GPIO are set for high drive, no slew rate control, and no input filter, digital or analog, unless otherwise specified.

Table 10. RGPIO General Control Timing

Symbol	Description	Min.	Max.	Unit
R1	CPUCLK from CLK_OUT pin high to GPIO output valid	—	16	ns
R2	CPUCLK from CLK_OUT pin high to GPIO output invalid (output hold)	1	—	ns
R3	GPIO input valid to bus clock high	17	—	ns
R4	CPUCLK from CLK_OUT pin high to GPIO input invalid	—	2	ns

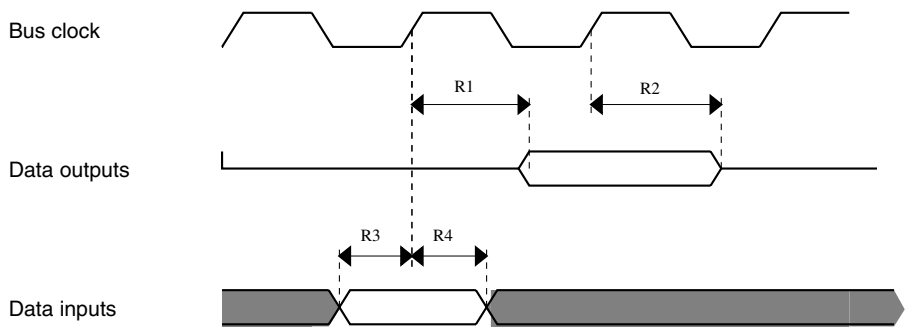

Figure 4. RGPIO timing diagram

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	115	°C
T_A	Ambient temperature	–40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	64 LQFP	48 LQFP	44 Laminate QFN	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	73	79	108	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	54	55	69	33	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	61	66	91	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	48	48	63	28	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	37	34	44	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	20	31	2.2	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5.0	4.0	6.0	6.0	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions —Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions —Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug specifications

Table 12. Background debug mode (BDM) timing

Number	Symbol	Description	Min.	Max.	Unit
1	t_{MSSU}	BKGD/MS setup time after issuing background debug force reset to enter user mode or BDM	500	—	ns
2	t_{MSH}	BKGD/MS hold time after issuing background debug force reset to enter user mode or BDM[1]	100	—	µs

6.3 Clock modules

6.3.1 MCG specifications

Table 14. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 10	—	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 1.0	± 4.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	3.3	4	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 50	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	1350 600	— —	ps ps	8
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	150×10^{-6} + 1075(1/f_{pll_ref})	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.

Table 17. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	208	1808	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 18. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk128k}$	• 128 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (data flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk128k}$	• 128 KB program flash	—	220	1850	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 B flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	275	2350	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	

Table continues on the next page...

Table 18. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	µs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash (FTFL) current and power specfications

Table 19. Flash (FTFL) current and power specfications

Symbol	Description	Typ.	Unit
I_{DD_PGM}	Worst case programming current in program flash	10	mA

Table 22. Flexbus switching specifications (continued)

Num	Description	Min.	Max.	Unit	Notes
FB2	Address, data, and control output valid	—	20	ns	1
FB3	Address, data, and control output hold	1	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	20	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	10	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_CS}}n$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0].

Note

The following diagrams refer to signal names that may not be included on your particular device. Ignore these extraneous signals.

Also, ignore the AA=0 portions of the diagrams because this setting is not supported in the Mini-FlexBus.

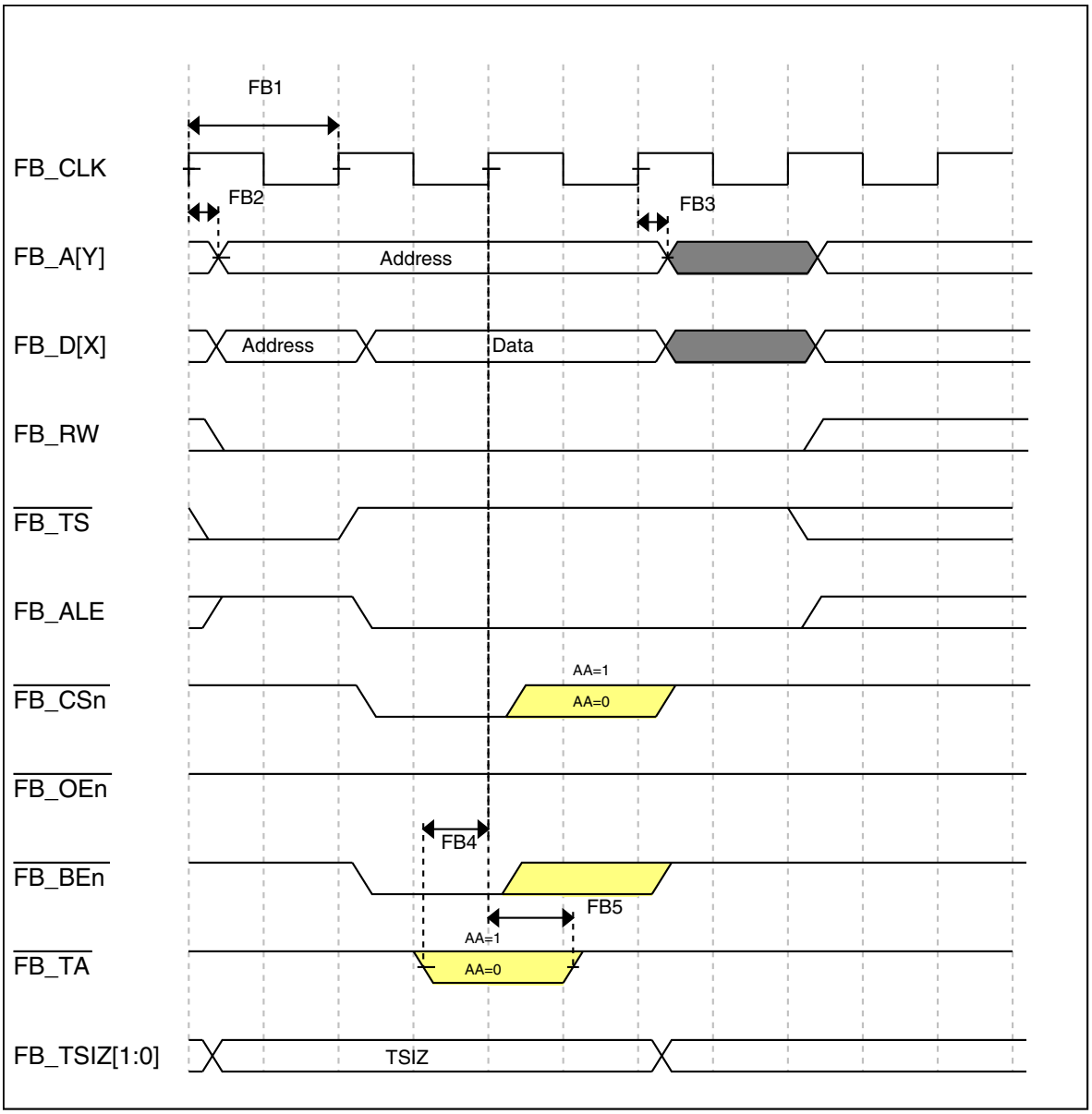

Figure 8. Mini-FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

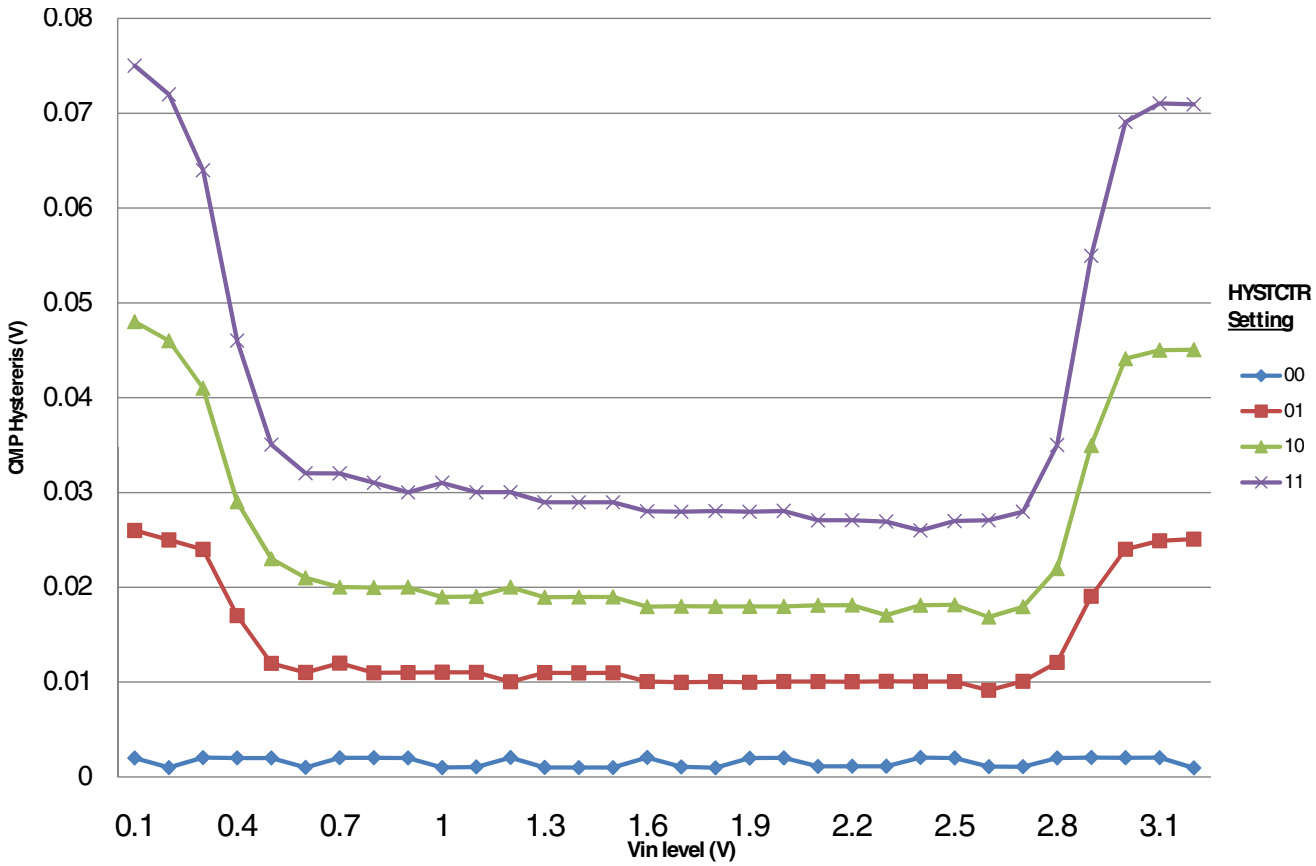

Figure 12. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

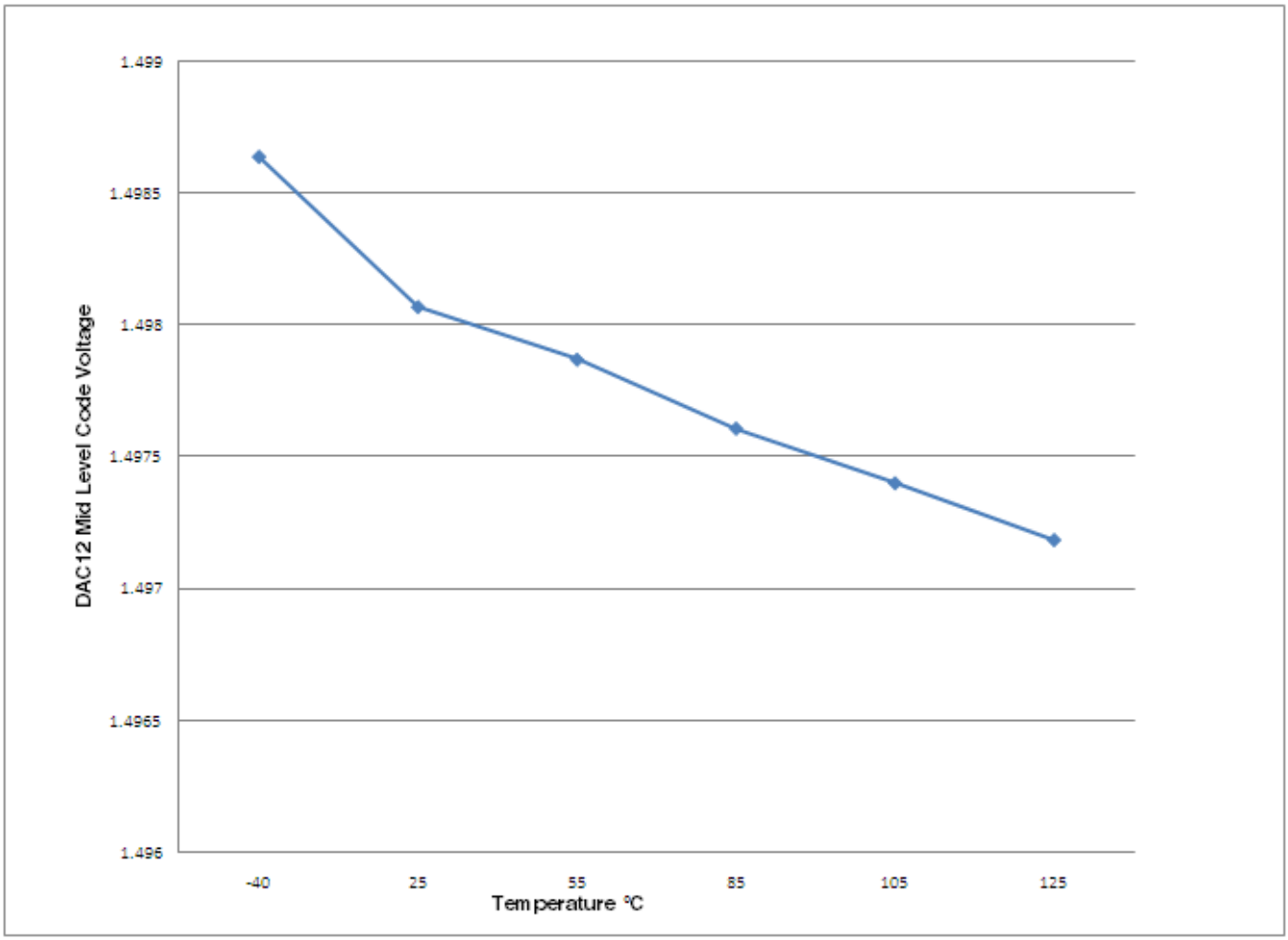

Figure 15. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 28. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	1

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.

Table 29. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1965	1.2	1.2027	V	
V_{out}	Voltage reference output with— factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.198	—	1.202	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only (MODE_LV = 00) current	—	—	80	µA	
I_{tr}	Tight-regulation buffer (MODE_LV =10) current	—	—	1.1	mA	
ΔV_{LOAD}	Load regulation (MODE_LV = 10) • current = + 1.0 mA • current = - 1.0 mA	 — —	 2 5	 — —	mV	1
T_{stup}	Buffer startup time	—	—	100	µs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range) (MODE_LV = 10, REGEN = 1)	—	2	—	mV	

1. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 30. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 31. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General Switching Specifications.

64-pin	48-pin	44-pin	32-pin	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
48	35	31	24	VDD	VDD								
49	36	32	25	VSS	VSS								
50	37	33	26	EXTAL1	EXTAL1	PTB7		I2C1_SDA	TMR_CLKIN1				
51	38	34	27	XTAL1	XTAL1	PTC0		I2C1_SCL	TMR_CLKIN0	RGPIO0			
52	39	35	28	RESET_b	Disabled	PTC1	RESET_b						
53	—	—	—	CMP0_IN0	CMP0_IN0	PTF0	SPI0_SS				FBa_AD5		
54	—	—	—	Disabled	Disabled	PTF1	SPI0_SCLK			CMP0_OUT	FBa_AD6		
55	—	—	—	CMP0_IN1	CMP0_IN1	PTF2	SPI0_MISO				FBa_AD7		
56	40	36	—	CMP0_IN2	CMP0_IN2	PTF3	SPI0_MOSI			RGPIO1	FBa_AD8		
57	41	37	29	CMP0_IN3	CMP0_IN3	PTC2	UART1_RTS_b	SPI1_SS		RGPIO2	FBa_AD18		
58	42	38	—	Disabled	Disabled	PTF4	UART1_CTS_b	SPI1_SCLK		FBa_D3	FBa_AD19		
59	43	39	—	Disabled	Disabled	PTF5	UART1_RX	SPI1_MISO		FBa_D2	FBa_RW_b		
60	44	40	—	Disabled	Disabled	PTF6	UART1_TX	SPI1_MOSI		FBa_D1	FBa_AD9		
61	45	41	—	Disabled	Disabled	PTF7	UART0_RTS_b		SPI0_SS	FBa_D0	FBa_AD10		
62	46	42	30	Disabled	Disabled	PTC3	UART0_CTS_b	RGPIO3	SPI0_SCLK	CLKOUT			
63	47	43	31	Disabled	Disabled	PTC4	UART0_RX	RGPIO4	SPI0_MISO	PDB0_EXTRG			
64	48	44	32	Disabled	Disabled	PTC5	UART0_TX	RGPIO5	SPI0_MOSI	CMT_IRO			

8.2 Pinout diagrams

The following diagrams show pinouts for the 64-pin, 48-pin, 44-pin, and 32-pin packages. These diagrams are representations for ease of reference. See the package drawings for mechanical details.

For each pin, the diagrams show the default function or (when disabled is the default) the ALT1 signal for a GPIO function. However, many signals may be multiplexed onto a single pin.

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
39	27	25	19	PTB2	PTE3
41	29			PTE4	PTE4
42	30			PTE5	PTE5
43				PTE6	PTE6
44	31	27		PTE7	PTE7
PTF					
53				PTF0	PTF0
54				PTF1	PTF1
55				PTF2	PTF2
56	40	36		PTF3	PTF3
58	42	38		PTF4	PTF4
59	43	39		PTF5	PTF5
60	44	40		PTF6	PTF6
61	45	41		PTF7	PTF7
5 V VREG					
22	18	16	13		VOUT33
21	17	15	12		VREGIN
ADC0					
19	15	13	10		ADC0_DP0/ ADC0_SE0
20	16	14	11		ADC0_DM0/ ADC0_SE1
11	7	5	5	PTA4	ADC0_DP1/ ADC0_SE2
12	8	6	6	PTA5	ADC0_DM1/ ADC0_SE3
25	21	19	15	PTA6	ADC0_SE8
26				PTD2	ADC0_SE9
27	22	20		PTD3	ADC0_SE10
28				PTD4	ADC0_SE11
29				PTD5	ADC0_SE12
30	23	21	16	PTA7	ADC0_SE13
31	24	22		PTD6	ADC0_SE14
32				PTD7	ADC0_SE15
38				PTE3	ADC0_SE16
39	27	25	19	PTB2	ADC0_SE17

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
40	28	26	20	PTB3	ADC0_SE18
41	29			PTE4	ADC0_SE19
42	30			PTE5	ADC0_SE20
43				PTE6	ADC0_SE21
44	31	27		PTE7	ADC0_SE22
13	9	7	7		VDDA
14	10	8			VREFH
16	12	10			VREFL
17	13	11	8		VSSA
DAC0					
18	14	12	9		DAC0_OUT
VREF					
15	11	9			VREF_OUT
CMP0					
53				PTF0	CMP0_IN0
55				PTF2	CMP0_IN1
56	40	36		PTF3	CMP0_IN2
57	41	37	29	PTC2	CMP0_IN3
54				PTF1	CMP0_OUT
CMT					
64	48	44	32	PTC5	CMT_IRO
TSI0					
25	21	19	15	PTA6	TSI0_CH0
26				PTD2	TSI0_CH1
27	22	20		PTD3	TSI0_CH2
28				PTD4	TSI0_CH3
29				PTD5	TSI0_CH4
30	23	21	16	PTA7	TSI0_CH5
31	24	22		PTD6	TSI0_CH6
32				PTD7	TSI0_CH7
33				PTE0	TSI0_CH8
34				PTE1	TSI0_CH9
36	26	24	18	PTB1	TSI0_CH10
37				PTE2	TSI0_CH11
38				PTE3	TSI0_CH12

Table continues on the next page...

Table 35. Module signals by GPIO port and pin (continued)

64-pin	48-pin	44-pin	32-pin	Port	Module signal(s)
60	44	40		PTF6	FBa_D1
59	43	39		PTF5	FBa_D2
58	42	38		PTF4	FBa_D3
31	24	22		PTD6	FBa_D4
30	23	21	16	PTA7	FBa_D5
27	22	20		PTD3	FBa_D6
25	21	19	15	PTA6	FBa_D7
44	31	27		PTE7	FBa_RW_b
I2C0 and I2C1					
3				PTC6	I2C0_SCL
35	25	23	17	PTB0	I2C0_SCL
4				PTC7	I2C0_SDA
36	26	24	18	PTB1	I2C0_SDA
6	2			PTD1	I2C1_SCL
42	30			PTE5	I2C1_SCL
51	38	34	27	PTC0	I2C1_SCL
5	1			PTD0	I2C1_SDA
43				PTE6	I2C1_SDA
50	37	33	26	PTB7	I2C1_SDA
I2C2 and I2C3					
7	3	1	1	PTA0	I2C2_SCL
11	7	5	5	PTA4	I2C2_SCL
8	4	2	2	PTA1	I2C2_SDA
12	8	6	6	PTA5	I2C2_SDA
32				PTD7	I2C3_SCL
37				PTE2	I2C3_SCL
33				PTE0	I2C3_SDA
38				PTE3	I2C3_SDA
SPI0					
39	27	25	19	PTB2	SPI0_MISO
55				PTF2	SPI0_MISO
63	47	43	31	PTC4	SPI0_MISO
38				PTE3	SPI0_MOSI
40	28	26	20	PTB3	SPI0_MOSI
56	40	36		PTF3	SPI0_MOSI

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