Renesas Electronics America Inc - R5F113THLFB#V5 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, CSI, I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	130
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 31x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f113thlfb-v5

(j) STOPST

This is a STOP status output pin.

(k) CTXD1

This is a serial data output pin of the CAN.

(i) CRXD1

This is a serial data intput pin of the CAN.

2.2.5 P40 to P47 (Port 4)

P40 to P47 function as an I/O port. These pins also function as data I/O for a flash memory programmer/debugger, timer I/O, comparator output, external interrupt request input, SNOOZE status output, and LIN serial data I/O. P42 and P43 are provided only in the 144-pin, 100-pin, 80-pin, and 64-pin products. P44 to P47 are provided only in the 144-pin, 100-pin, and 80-pin products.

Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

For the P43 pin, the input threshold level can be specified using the port input threshold control register 4 (PITHL4).

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P47 function as an I/O port. These pins can be set to input or output port in 1-bit units using port mode register 4 (PM4).

(2) Control mode

P40 to P47 function as data I/O for a flash memory programmer/debugger, timer I/O, comparator output, external interrupt request input, SNOOZE status output, and LIN serial data I/O.

(a) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

(b) TI07, TI10, TI12

These are pins for inputting an external count clock/capture trigger to 16-bit timers.

(c) TO07, TO10, TO12

These are timer output pins of 16-bit timers.

(d) TRJIO0

This is a timer I/O pin of timer RJ.

(e) VCOUT0

This is a comparator output pin.

(f) INTP13

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(g) SNZOUT2

This is a SNOOZE status output pin.

Table 4-12. Settings of Registers When Using Port 7 (2/2)

Pin Name		PM7x	PIM7x	POM7x	PMC7x	PITHL7x	Alternate Function Setting	Remark
Name	I/O							
P75	Input	1	–	–	–	0	×	CMOS input (Schmitt1 input)
						1	×	CMOS input (Schmitt3 input)
	Output	0	–	–	–	×	×	
P76	Input	1	–	–	–	0	×	CMOS input (Schmitt1 input)
						1	×	CMOS input (Schmitt3 input)
	Output	0	–	–	–	×	($\overline{\text{SCK10}}$ output = 1 Note 4)	
P77	Input	1	–	–	–	0	×	CMOS input (Schmitt1 input)
						1	×	CMOS input (Schmitt3 input)
	Output	0	–	–	–	×	×	

Notes 1. When a pin sharing the serial array unit function is to be used as a general-purpose port pin, the SOmn bit of the serial output register m (SOm), the SOEmn bit of the serial output enable register m (SOEm), and the SEmn bit of the serial channel enable status register m (SEm) corresponding to the target unit and channel must have the same setting as its initial value (m = 0, 1, 2, n = 0, 1).

2. When a pin sharing a timer output function of the timer array unit is to be used as a general-purpose port pin, the TOmn bit of the timer output register m (TOm) and the TOEmn bit of the timer output enable register m (TOEm) corresponding to the target unit and channel must have the same setting as in the initial state (m = 0, 1, 2, n = 0 to 7).

3. When a pin sharing the SNOOZE status output function is to be used as a general-purpose port pin, the OUTEN0 to OUTEN7 bits of the SNOOZE status output control registers 0, 1, 2, 3 (PSNZCNT0, 1, 2, 3) must have the same setting as its initial value.

4. When a pin sharing the serial array unit function is to be used as a general-purpose port pin, the CKOmn bit of the serial output register m (SOm), the SOEmn bit of the serial output enable register m (SOEm), and the SEmn bit of the serial channel enable status register m (SEm) corresponding to the target unit and channel must have the same setting as its initial value (m = 0, 1, 2, n = 0, 1).

5. When a pin sharing the serial data output function of the CAN is to be used as a general-purpose port pin, operation of the corresponding CAN must be stopped.

6. Functions in parentheses can be assigned via settings in the peripheral I/O redirection register 4 (PIOR4).

Remark ×: Don't care
PM7x: Port mode register 7
PIM7x: Port input mode register 7
POM7x: Port output mode register 7
PMC7x: Port mode control register 7
PITHL7x: Port input threshold control register 7

4.3.11 Peripheral I/O redirection register 2 (PIOR2)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.

PIOR2 enables or disables redirection of the timer array unit functions; that is, it specifies which I/O port is assigned to each input pin of timer array unit 1.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 4-102. Format of Peripheral I/O Redirection Register 2 (PIOR2)

Address: F0018H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR2	PIOR27	PIOR26	PIOR25	PIOR24	PIOR23	PIOR22	PIOR21	PIOR20

Bit	Function	144-pin		100-pin		80-pin	
		Setting value		Setting value		Setting value	
		0	1	0	1	0	1
PIOR27	TI17	P71	P57	P71	P57	P71	P57
PIOR26	TI16	P32	P65	P32	P65	P32	P65
PIOR25	TI15	P70	P56	P70	P56	P70	P56
PIOR24	TI14	P31	P64	P31	P64	P31	P64
PIOR23	TI13	P10	P55	P10	P55	P10	P55
PIOR22	TI12	P11	P46	P11	P46	P11	P46
PIOR21	TI11	P12	P54	P12	P54	P12	P54
PIOR20	TI10	P41	P45	P41	P45	P41	P45

Caution The 64-, and 48-pin products do not have the PIOR2 register.

Figure 5-7. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFFA3H After reset: 07H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

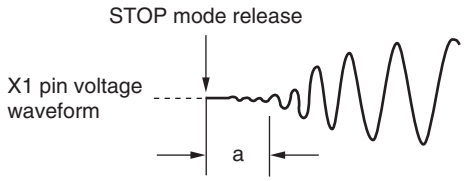
OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection		
				f_X = 10 MHz	f_X = 20 MHz
0	0	0	$2^8/f_X$	25.6 μs	12.8 μs
0	0	1	$2^9/f_X$	51.2 μs	25.6 μs
0	1	0	$2^{10}/f_X$	102.4 μs	51.2 μs
0	1	1	$2^{11}/f_X$	204.8 μs	102.4 μs
1	0	0	$2^{13}/f_X$	819.2 μs	409.6 μs
1	0	1	$2^{15}/f_X$	3.27 ms	1.63 ms
1	1	0	$2^{17}/f_X$	13.10 ms	6.55 ms
1	1	1	$2^{18}/f_X$	26.21 ms	13.10 ms

Cautions

1. **To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.**
2. **Change the setting of the OSTS register before setting the MSTOP bit of the clock operation status control register (CSC) to 0.**
3. **Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.**
4. **The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register.**

   In the following cases, set the oscillation stabilization time of the OSTS register to the value equal to or greater than the count value which is to be checked by the OSTC register after the oscillation starts.

   - **If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.**
   - **If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)**
5. **The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).**



6.3.19 PWM output delay control register 2 (PWMDLY2)

This register controls output delay of PWM output signal output from the TO1n pin.

Set the PWMDLY2 register by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Address: F022DH After reset: 00H R/W

Symbol	15	14	13	12	11	10	9	8
PWMDLY2	TO171	TO170	TO161	TO160	TO151	TO150	TO141	TO140

Address: F022CH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PWMDLY2	TO131	TO130	TO121	TO120	TO111	TO110	0	0

TO1n1	TO1n0	PWM output delay control of timer array unit 1 TO1n
0	0	No delay
0	1	Delayed by one cycle of the CPU/peripheral hardware clock (f_{CLK}).
1	0	Delayed by two cycles of the CPU/peripheral hardware clock (f_{CLK}).
1	1	Delayed by three cycles of the CPU/peripheral hardware clock (f_{CLK}).

Remark n: Channel number (n = 1 to 7)

Cautions

1. **Set this register before outputting a PWM output signal (do not change the setting during operation).**
2. **Set this register with a 16-bit memory manipulation instruction. Do not set this register with a 1-bit or 8-bit memory manipulation instruction.**
3. **If this register is not used for PWM output, it should be cleared to 0.**
4. **When setting this register after the PWM output is stopped, wait for four cycles of the CPU/peripheral hardware clock (f_{CLK}) before the setting.**
5. **Even if this register is set for a delay, this doesn't affect the operation of other pin functions multiplexed on the same pin as the TO1n pin function (n = 1 to 7).**

Figure 6-48 Operation Procedure of Interval Timer/Square Wave Output Function (2/2)

	Software Operation	Hardware Status
TAU stop	To hold the TOmn pin output level Clears the TOmn bit to 0 after the value to be held is set to the port register. →	The TOmn pin output level is held by port function.
	When holding the TOmn pin output level is not necessary Setting not required.	
	The TAUmEN bit of the PER0, PER1 register is cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmn bit is cleared to 0 and the TOmn pin is set to port mode.)

Remark 144-pin products m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 7)
100-pin, 80-pin, 64-pin, and 48-pin products m: Unit number (m = 0 and 1), n: Channel number (n = 0 to 7)

6.8.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor 1 [%] = {Set value of TDRmp (slave 1)}/{Set value of TDRmn (master) + 1} × 100
Duty factor 2 [%] = {Set value of TDRmq (slave 2)}/{Set value of TDRmn (master) + 1} × 100

Remark Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer count register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

When channel 0 is used as the master channel as above, up to three types of PWM signals can be output at the same time.

Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).

Remark 144-pin products m: Unit number (m = 0 to 2), n: Master Channel number (n = 0, 2, 4)
100-pin, 80-pin, 64-pin, and 48-pin products m: Unit number (m = 0 and 1), n: Master Channel number (n = 0, 2, 4)
p: Slave channel number 1, q: Slave channel number 2
$n < p < q \leq 7$ (Where p and q are integers greater than n)

4. The operation of the watchdog timer in the HALT, STOP, and SNOOZE modes differs as follows depending on the set value of bit 0 (WDSTBYON) and bit 4 (WDTON) of the option byte (000C0H).

	WDTON = 1 and WDSTBYON = 0	WDTON = 1 and WDSTBYON = 1
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		
In SNOOZE mode		

If WDSTBYON = 0, the watchdog timer resumes counting after the HALT, STOP, or SNOOZE modes is released. At this time, the counter is cleared to 0 and counting starts.
When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer counter is to be cleared after the STOP mode release by an interval interrupt.

11.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to the watchdog timer enable register (WDTE) during the window open period before the overflow time.

The following overflow times can be set.

Table 11-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer (f_{WDT} = 17.25 kHz (MAX.))
0	0	0	$2^6/f_{WDT}$ (3.71 ms)
0	0	1	$2^7/f_{WDT}$ (7.42 ms)
0	1	0	$2^8/f_{WDT}$ (14.84 ms)
0	1	1	$2^9/f_{WDT}$ (29.68 ms)
1	0	0	$2^{11}/f_{WDT}$ (118.72 ms)
1	0	1	$2^{13}/f_{WDT}$ Note (474.89 ms)
1	1	0	$2^{14}/f_{WDT}$ Note (949.79 ms)
1	1	1	$2^{16}/f_{WDT}$ Note (3799.18 ms)

Note When the interval interrupt of watchdog timer is used, do not set the overflow time to $2^{13}/f_{WDT}$, $2^{14}/f_{WDT}$ or $2^{16}/f_{WDT}$.

Remark f_{WDT}: WDT-dedicated low-speed on-chip oscillator clock frequency

12.3.8 Conversion result comparison upper limit setting register (ADUL)

This register is used to specify the setting for checking the upper limit of the A/D conversion results.

The A/D conversion results and ADUL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 12-8**).

The ADUL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 12-12. Format of Conversion Result Comparison Upper Limit Setting Register (ADUL)

Address: F0011H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
ADUL	ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0

Cautions 1. When A/D conversion with 10-bit resolution is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the value in the ADUL register.

2. Writing new values to the ADUL and ADLL registers is prohibited while conversion is enabled. Write new values to these registers while conversion is stopped (ADCE = 0).

3. The setting of the ADUL registers must be greater than that of the ADLL register.

12.3.9 Conversion result comparison lower limit setting register (ADLL)

This register is used to specify the setting for checking the lower limit of the A/D conversion results.

The A/D conversion results and ADLL register value are compared, and interrupt signal (INTAD) generation is controlled in the range specified for the ADRCK bit of A/D converter mode register 2 (ADM2) (shown in **Figure 12-8**).

The ADLL register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 12-13. Format of Conversion Result Comparison Lower Limit Setting Register (ADLL)

Address: F0012H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADLL	ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0

Cautions 1. When A/D conversion with 10-bit resolution is selected, the higher eight bits of the 10-bit A/D conversion result register (ADCR) are compared with the value in the ADLL register.

2. Writing new values to the ADUL and ADLL registers is prohibited while conversion is enabled. Write new values to these registers while conversion is stopped (ADCE = 0).

3. The setting of the ADUL registers must be greater than that of the ADLL register.

15.5.9 Procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) communication

The procedure for processing errors that occurred during 3-wire serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) communication is described in Figure 15-107.

Figure 15-107. Processing Procedure in Case of Overrun Error

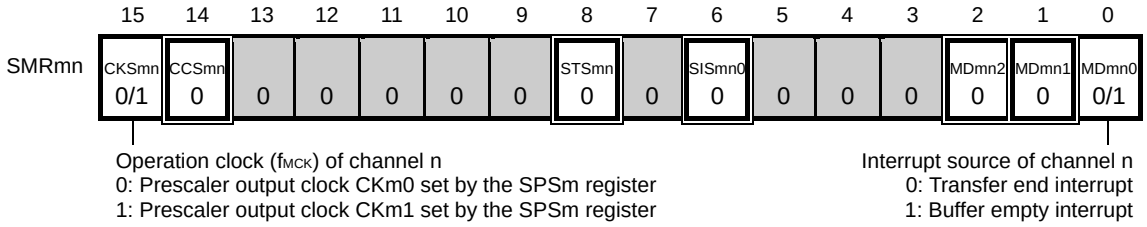
Software Manipulation	Hardware Status	Remark
Reads serial data register mn (SDRmn). →	The BFFmn bit of the SSRmn register is set to 0 and channel n is enabled to receive data.	This is to prevent an overrun error if the next reception is completed during error processing.
Reads serial status register mn (SSRmn).		Error type is identified and the read value is used to clear error flag.
Writes 1 to serial flag clear trigger register mn (SIRmn). →	Error flag is cleared.	Error can be cleared only during reading, by writing the value read from the SSRmn register to the SIRmn register without modification.

Remark m: Unit number (m = 0-2), n: Channel number (n = 0, 1), mn = 00, 01, 10, 11, 20, 21

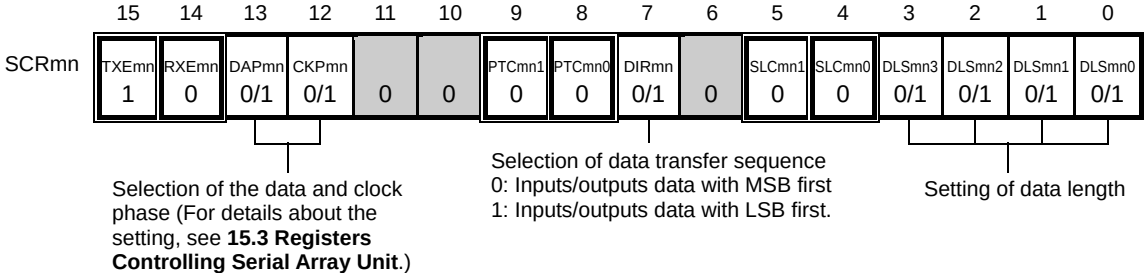
(1) Register setting

Figure 15-110. Example of Contents of Registers for Master Transmission of SPI Function (CSI00, CSI01, CSI10, CSI11) (1/2)

(a) Serial mode register mn (SMRmn)

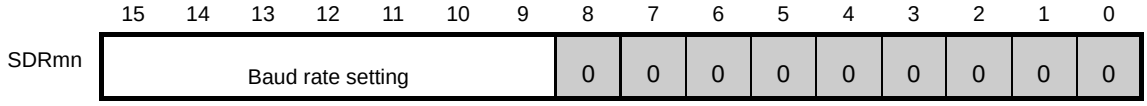


(b) Serial communication operation setting register mn (SCRmn)

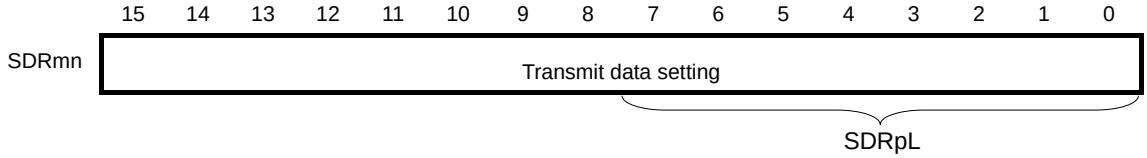


(c) Serial data register mn (SDRmn)

(1) When operation is stopped (SEmn = 0)



(2) When operation is in progress (SEmn = 1) (Lower 8 bits: SDRpL)

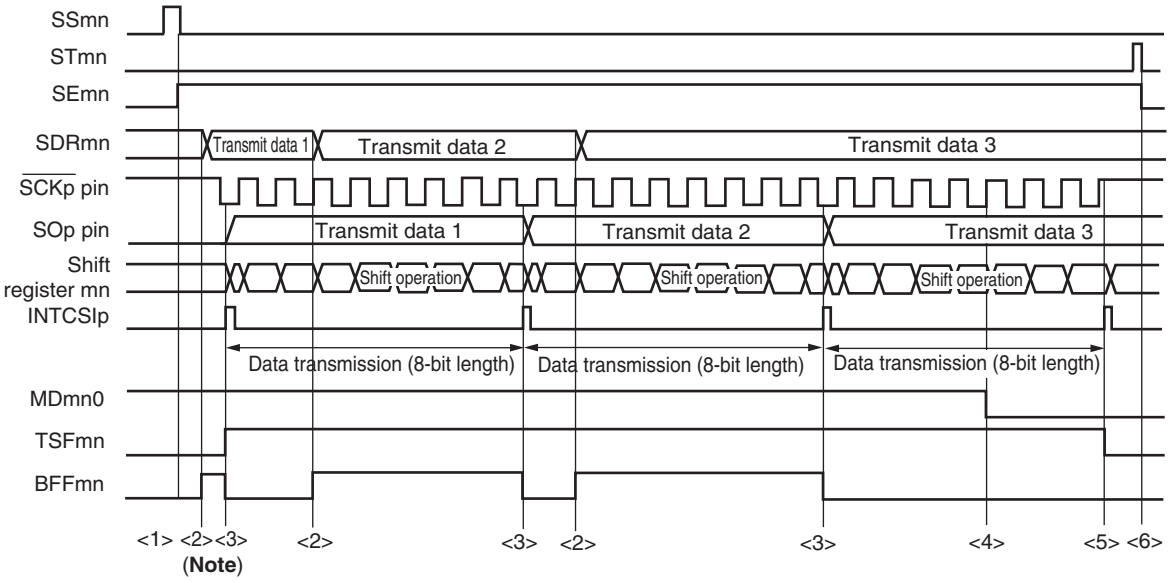


Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01, 10, 11), mn = 00, 01, 10, 11

2. ☐: Setting is fixed in the CSI master transmission mode, ▒: Setting disabled (set to the initial value)
0/1: Set to 0 or 1 depending on the usage of the user

(4) Processing flow (in continuous transmission mode)

Figure 15-140. Timing Chart of Slave Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)

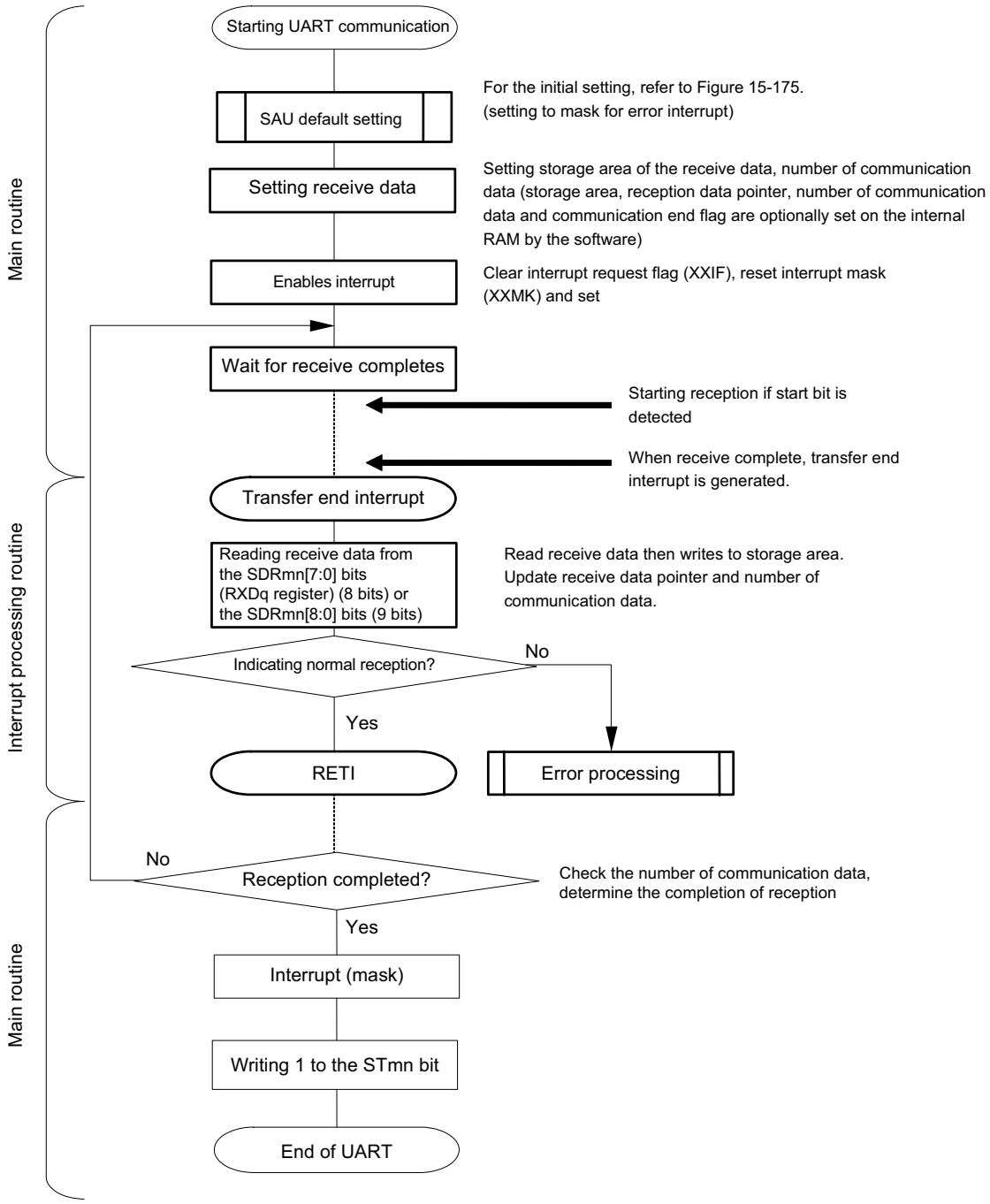


Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 1), p: CSI number (p = 00, 01, 10, 11), mn = 00, 01, 10, 11

Figure 15-180. Flowchart of UART Reception (UART2)



Caution For the UART reception, set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more f_{MCK} clocks have elapsed.

Remark m: Unit number (m = 2), n: Channel number (n = 1), mn = 21, r: Channel number (r = n – 1), q: UART number (q = 2)

UEBDCE bit (expansion bit/data comparison enable bit)

The UEBDCE bit enables or disables comparison between the 8-bit received data excluding the expansion bits and the value of LIDBn register after detection of the expansion bit.

With 0 set, comparison between the received data in the LURDRn register and the LIDBn register value is disabled after detection of the expansion bit value selected by the UEBDL bit as the expansion bit.

With 1 set, comparison between the received data in the LURDRn register and the LIDBn register value is enabled after detection of the expansion bit value selected by the UEBDL bit as the expansion bit.

Set this bit when the OMM0 bit in the LMSTn register is 0 (LIN reset mode).

Do not set this bit to 1 with the UEBE bit set to 0 (expansion bit operation disabled).

Do not set this bit to 1 with the UECD bit set to 1 (expansion bit comparison disabled).

Do not set this bit to 1 when the UART buffer is in use.

Do not set this bit to 1 with the UWC bit in the LUSCn register set to 1 (start of reception from STOP mode enabled).

UTIGTS bit (transmission interrupt generation timing select bit)

The UTIGTS bit sets the generation timing of the transmission interrupt.

With 0 set, the transmission interrupt is generated at the start of transmission.

With 1 set, the transmission interrupt is generated at the completion of transmission.

When transmission from the UART buffer is performed with 0 set, the transmission interrupt is generated only at the start of the transmission of the last data of the data length set with the MDL bits in the LDFCn register.

When transmission from the UART buffer is performed with 1 set, the transmission interrupt is generated only at the completion of the transmission of the last data of the data length set with the MDL bits in the LDFCn register.

UECD bit (expansion bit comparison disable bit)

The UECD bit enables or disables comparison between the received expansion bit and the UEBDL bit value when the UEBE bit is 1 (expansion bit operation is enabled).

With 0 set, comparison between the received expansion bit and the UEBDL bit value is enabled when the expansion bit is received.

With 1 set, comparison between the received expansion bit and the UEBDL bit value is disabled when the expansion bit is received.

Set this bit when the OMM0 bit in the LMSTn register is 0 (LIN reset mode).

Do not set this bit to 1 when the UART buffer is in use.

Do not set this bit to 1 with the UEBDCE bit set to 1 (data comparison after expansion bit detection is enabled).

Table 18-3. List of CAN Module Registers (7/37)

Address	Special Function Register (SFR) Name	Symbol		R/W	Access Size			After Reset
					1 bit	8 bits	16 bits	
F03DAH	CAN receive rule entry register 4CH[Note 1]	GAFLPH4L	GAFLPH4	R/W	—	√	√	0000H
F03DBH		GAFLPH4H			—	√		
F03DAH	CAN receive buffer register 3CH[Note 2]	RMDF13L	RMDF13	R	—	√	√	0000H
F03DBH		RMDF13H			—	√		
F03DCH	CAN receive rule entry register 5AL[Note 1]	GAFLIDL5L	GAFLIDL5	R/W	—	√	√	0000H
F03DDH		GAFLIDL5H			—	√		
F03DCH	CAN receive buffer register 3DL[Note 2]	RMDF23L	RMDF23	R	—	√	√	0000H
F03DDH		RMDF23H			—	√		
F03DEH	CAN receive rule entry register 5AH[Note 1]	GAFLIDH5L	GAFLIDH5	R/W	—	√	√	0000H
F03DFH		GAFLIDH5H			—	√		
F03DEH	CAN receive buffer register 3DH[Note 2]	RMDF33L	RMDF33	R	—	√	√	0000H
F03DFH		RMDF33H			—	√		
F03E0H	CAN receive rule entry register 5BL[Note 1]	GAFLML5L	GAFLML5	R/W	—	√	√	0000H
F03E1H		GAFLML5H			—	√		
F03E0H	CAN receive buffer register 4AL[Note 2]	RMIDL4L	RMIDL4	R	—	√	√	0000H
F03E1H		RMIDL4H			—	√		
F03E2H	CAN receive rule entry register 5BH[Note 1]	GAFLMH5L	GAFLMH5	R/W	—	√	√	0000H
F03E3H		GAFLMH5H			—	√		
F03E2H	CAN receive buffer register 4AH[Note 2]	RMIDH4L	RMIDH4	R	—	√	√	0000H
F03E3H		RMIDH4H			—	√		
F03E4H	CAN receive rule entry register 5CL[Note 1]	GAFLPL5L	GAFLPL5	R/W	—	√	√	0000H
F03E5H		GAFLPL5H			—	√		
F03E4H	CAN receive buffer register 4BL[Note 2]	RMTS4L	RMTS4	R	—	√	√	0000H
F03E5H		RMTS4H			—	√		
F03E6H	CAN receive rule entry register 5CH[Note 1]	GAFLPH5L	GAFLPH5	R/W	—	√	√	0000H
F03E7H		GAFLPH5H			—	√		
F03E6H	CAN receive buffer register 4BH[Note 2]	RMPTR4L	RMPTR4	R	—	√	√	0000H
F03E7H		RMPTR4H			—	√		
F03E8H	CAN receive rule entry register 6AL[Note 1]	GAFLIDL6L	GAFLIDL6	R/W	—	√	√	0000H
F03E9H		GAFLIDL6H			—	√		
F03E8H	CAN receive buffer register 4CL[Note 2]	RMDF04L	RMDF04	R	—	√	√	0000H
F03E9H		RMDF04H			—	√		
F03EAH	CAN receive rule entry register 6AH[Note 1]	GAFLIDH6L	GAFLIDH6	R/W	—	√	√	0000H
F03EBH		GAFLIDH6H			—	√		
F03EAH	CAN receive buffer register 4CH[Note 2]	RMDF14L	RMDF14	R	—	√	√	0000H
F03EBH		RMDF14H			—	√		
F03ECH	CAN receive rule entry register 6BL[Note 1]	GAFLML6L	GAFLML6	R/W	—	√	√	0000H
F03EDH		GAFLML6H			—	√		
F03ECH	CAN receive buffer register 4DL[Note 2]	RMDF24L	RMDF24	R	—	√	√	0000H
F03EDH		RMDF24H			—	√		
F03EEH	CAN receive rule entry register 6BH[Note 1]	GAFLMH6L	GAFLMH6	R/W	—	√	√	0000H
F03EFH		GAFLMH6H			—	√		
F03EEH	CAN receive buffer register 4DH[Note 2]	RMDF34L	RMDF34	R	—	√	√	0000H
F03EFH		RMDF34H			—	√		

Notes 1. These registers are allocated to RAM window 0 for the CAN module (receive rules and CAN RAM test register). When setting these registers, set the RPAGE bit in the GRWCR register to 0.

2. These registers are allocated to RAM window 1 for the CAN module (receive buffer, receive FIFO buffer, transmit/receive FIFO buffer, transmit buffer, and transmit history data). When setting these registers, set the RPAGE bit in the GRWCR register to 1.

Table 22-2. Flags Corresponding to Interrupt Request Sources (2/5)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	144-pin	100-pin	80-pin	64-pin	48-pin
INTP13	PIF13	IF0H	PMK13	MK0H	PPR013, PPR113	PR00H, PR10H	√	√	√	–	–
INTCLM	CLMIF		CLMMK		CLMPR0, CLMPR1		√	√	√	√	√
INTST0	STIF0		STMK0		STPR00, STPR10		√	√	√	√	√
INTCSI00	IICIF00		CSIMK00		CSIPR000, CSIPR100		√	√	√	√	√
INTIIC00	IICIF00		IICMK00		IICPR000, IICPR100		√	√	√	√	√
INTSR0	SRIF0		SRMK0		SRPR00, SRPR10		√	√	√	√	√
INTCSI01	CSIIF01		CSIMK01		CSIPR001, CSIPR101		√	√	√	√	√
INTIIC01	IICIF01		IICMK01		IICPR001, IICPR101		√	√	√	√	√
INTTRD0	TRDIF0		TRDMK0		TRDPR00, TRDPR10		√	√	√	√	√
INTTRD1	TRDIF1		TRDMK1		TRDPR01, TRDPR11		√	√	√	√	√
INTTRJ0	TRJIF0		TRJMK0		TRJPR00, TRJPR10		√	√	√	√	√
INTRAM	RAMIF		RAMMK		RAMPR0, RAMPR1		√	√	√	√	√
INTLIN0TRM	LIN0TRMIF		LIN0TRMMK		LIN0TRMPR0, LIN0TRMPR1		√	√	√	√	√

Cautions 1. If one of the interrupt sources INTST0, INTCSI00, and INTIIC00 is generated, bit 1 of the IF0H register is set to 1. Bit 1 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

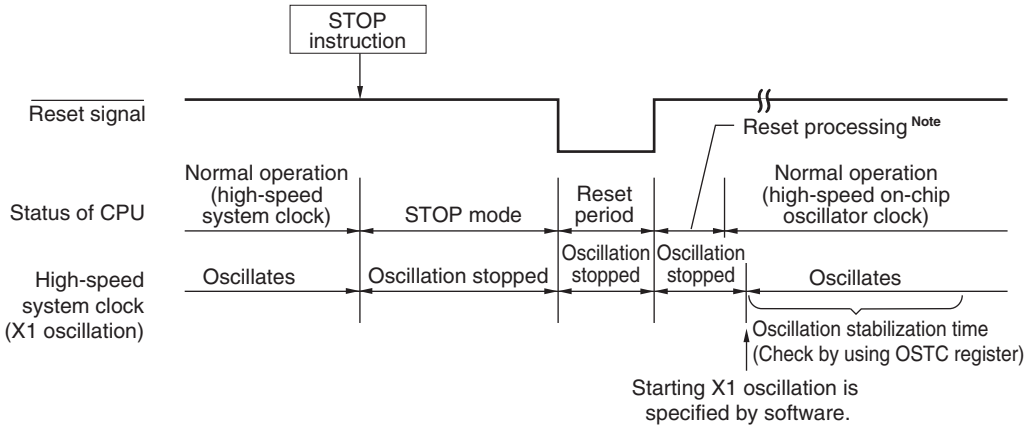
2. If one of the interrupt sources INTSR0, INTCSI01, and INTIIC01 is generated, bit 2 of the IF0H register is set to 1. Bit 2 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

(b) Release by reset signal generation

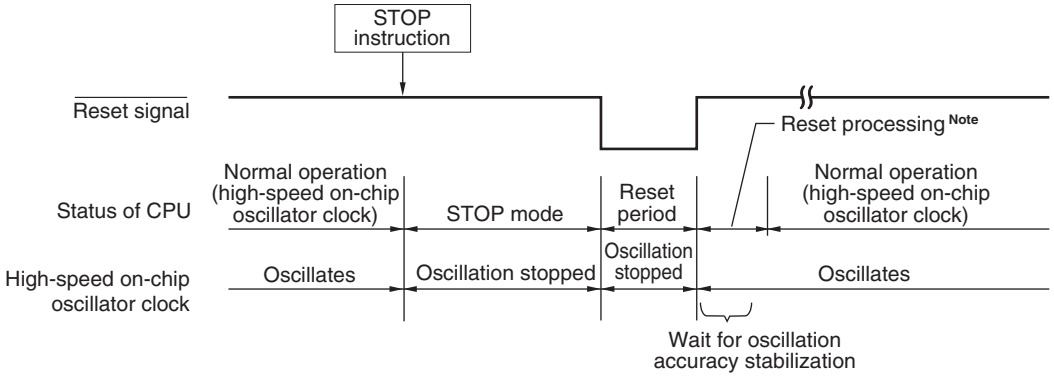
When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 24-7. STOP Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



(2) When high-speed on-chip oscillator clock is used as CPU clock



Note For the reset processing time, see **CHAPTER 26 POWER-ON-RESET CIRCUIT**.

Item \ STOP Mode Setting		During a period in STOP mode, input of a timer trigger signal for the A/D converter, reception of a data signal for the LIN/UART module in the UART mode, or the generation of an interrupt signal for DTC activation
		When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})
Power-on-reset function		Operable
Voltage detection function		
External interrupt		
Key interrupt function		
CRC operation function	High-speed CRC	Operation stopped
	General-purpose CRC	
Illegal-memory access detection function		
RAM2 bit error detection function		
RAM guard function		
SFR guard function		
CPU stack pointer monitor function		Operation stopped (operation can continue during vectored interrupt servicing)

Remark Operation stopped: Operation is automatically stopped before switching to the STOP mode.
Operation disabled: Operation is stopped before switching to the STOP mode.

f_{IH}: High-speed on-chip oscillator clock f_{IL}: Low-speed on-chip oscillator clock
f_X: X1 clock f_{EX}: External main system clock
f_{XT}: XT1 clock f_{EXS}: External subsystem clock
f_{PLL}: PLL clock
f_{WDT}: WDT-dedicated low-speed on-chip oscillator clock

(2) SNOOZE mode status output (SNOOZEST)

This function is used to output the status of the SNOOZE mode (in any mode other than the SNOOZE mode or in the SNOOZE mode) on the specified pin.

This function is executed by f_{SL} (sub/low-speed on-chip oscillator select clock), timer RD0, event link controller (ELC), A/D converter, and ports simultaneously. f_{SL} is used as the count source for the timer RD0. By using the PWM function of the timer mode, the timer RD0 sets a period in the TRDGRA0 register and generates a compare match signal in the TRDGRB0 and TRDGRC0 registers. The compare match signal of the TRDGRB0 register is used as the operation trigger of the A/D converter via the ELC. After receiving this operation trigger, the A/D converter performs A/D conversion in SNOOZE mode. After the compare match signal of the TRDGRC0 register is received, SNOOZE status is output from the SNZOUTn (n = 0 to 7) pin selected by the PSNZCNT0 to PSNZCNT3 registers.

TRDIOC0 cannot be output when SNOOZE status is output.

Figure 30-3. Format of Option Byte (000C2H/020C2H)

Address: 000C2H/020C2H[Note 1] After reset: — (user setting value [Note 2])

7	6	5	4	3	2	1	0
1	1	RESOUTB	FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

RESOUTB	RESOUTB output function
0	Selects P130 as the RESOUT pin • The low level is output during a reset. • The high level is automatically output upon release from the reset state. • The output latch value has no effect on the output.
1	Selects P130 as a general port pin (output only) • The low level is output during a reset. • The output latch value is output upon release from the reset state.

FRQSEL4	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator clock
1	1	0	0	0	64 MHz
1	0	0	0	0	48 MHz
0	1	0	0	0	32 MHz
0	0	0	0	0	24 MHz
0	1	0	0	1	16 MHz
0	0	0	0	1	12 MHz
0	1	0	1	0	8 MHz
0	1	0	1	1	4 MHz
0	1	1	0	1	1 MHz
Other than above					Setting prohibited

Notes 1. Set the same value as 000C2H to 020C2H when the boot swap operation is used because 000C2H is replaced by 020C2H.

2. The setting at shipment of the user option byte is FFH.