Renesas Electronics America Inc - R5F113THLFB#X0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, CSI, I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	130
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 31x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f113thlfb-x0

2.1.6 Pins for each product (pins other than port pins)

This subchapter shows the pins other than the ports shown in tables 2-2.

√ indicates the pin that is provided in the product and — indicates the pin that is not provided.

Table 2-2. List of RL78/F15 Pins Other than Port Pins (1/5)

Pin Function	I/O	Function	Pin Count				
			144-pin	100-pin	80-pin	64-pin	48-pin
ANI0	Input	A/D converter analog input (V_{DD} connection)	√	√	√	√	√
ANI1	Input		√	√	√	√	√
ANI2	Input		√	√	√	√	√
ANI3	Input		√	√	√	√	√
ANI4	Input		√	√	√	√	√
ANI5	Input		√	√	√	√	√
ANI6	Input		√	√	√	√	√
ANI7	Input		√	√	√	√	√
ANI8	Input		√	√	√	√	√
ANI9	Input		√	√	√	√	√
ANI10	Input		√	√	√	√	√
ANI11	Input		√	√	√	√	√
ANI12	Input		√	√	√	√	√
ANI13	Input		√	√	√	√	—
ANI14	Input		√	√	√	√	—
ANI15	Input		√	√	√	√	—
ANI16	Input		√	√	√	√	—
ANI17	Input		√	√	√	—	—
ANI18	Input		√	√	—	—	—
ANI19	Input		√	√	—	—	—
ANI20	Input		√	√	—	—	—
ANI21	Input		√	√	—	—	—
ANI22	Input		√	√	—	—	—
ANI23	Input		√	√	—	—	—
ANI24	Input	A/D converter analog input (EV_{DD} connection)	√	√	√	√	√
ANI25	Input		√	√	√	√	√
ANI26	Input		√	√	√	√	√
ANI27	Input		√	√	√	—	√
ANI28	Input		√	√	√	—	√
ANI29	Input		√	√	√	—	—
ANI30	Input		√	√	√	—	—
IVCMP00	Input	Comparator analog voltage input	√	√	√	√	√
IVCMP01	Input		√	√	√	√	√
IVCMP02	Input		√	√	√	√	√
IVCMP03	Input		√	√	√	√	√
IVREF0	Input	Comparator reference voltage input	√	√	√	√	√

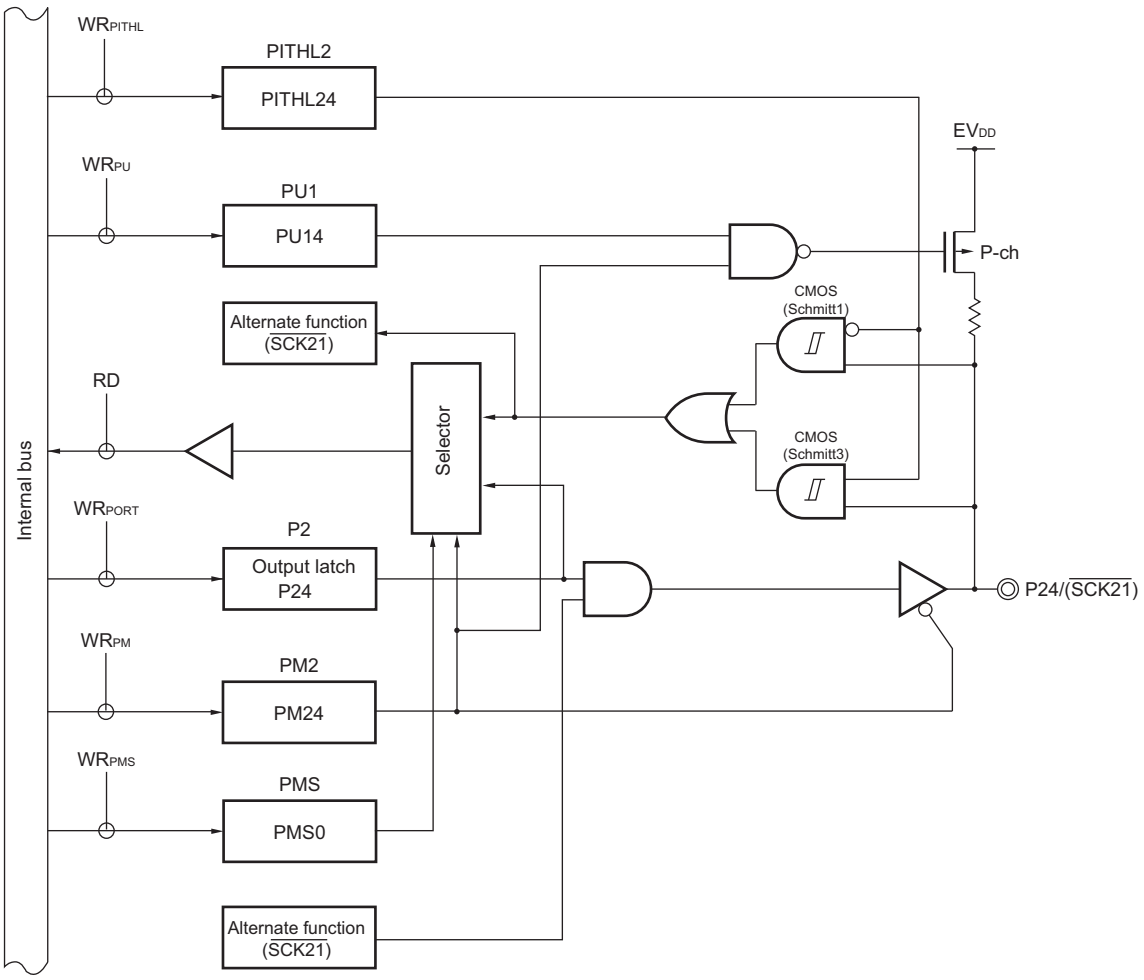
Table 3-6. Extended SFR (2nd SFR) List (19/52)

Address	Special Function Register (2nd SFR) Name	Symbol		R/W	Manipulable Bit Range			After reset
					1-bit	8-bit	16-bit	
F03D4H	CAN receive buffer register 3BL Note 2	RMTS3L	RMTS3	R	–	√	√	0000H
F03D5H		RMTS3H			–	√		
F03D6H	CAN receive rule entry register 4BH Note 1	GAFLMH4L	GAFLMH4	R/W	–	√	√	0000H
F03D7H		GAFLMH4H			–	√		
F03D6H	CAN receive buffer register 3BH Note 2	RMPTR3L	RMPTR3	R	–	√	√	0000H
F03D7H		RMPTR3H			–	√		
F03D8H	CAN receive rule entry register 4CL Note 1	GAFLPL4L	GAFLPL4	R/W	–	√	√	0000H
F03D9H		GAFLPL4H			–	√		
F03D8H	CAN receive buffer register 3CL Note 2	RMDF03L	RMDF03	R	–	√	√	0000H
F03D9H		RMDF03H			–	√		
F03DAH	CAN receive rule entry register 4CH Note 1	GAFLPH4L	GAFLPH4	R/W	–	√	√	0000H
F03DBH		GAFLPH4H			–	√		
F03DAH	CAN receive buffer register 3CH Note 2	RMDF13L	RMDF13	R	–	√	√	0000H
F03DBH		RMDF13H			–	√		
F03DCH	CAN receive rule entry register 5AL Note 1	GAFLIDL5L	GAFLIDL5	R/W	–	√	√	0000H
F03DDH		GAFLIDL5H			–	√		
F03DCH	CAN receive buffer register 3DL Note 2	RMDF23L	RMDF23	R	–	√	√	0000H
F03DDH		RMDF23H			–	√		
F03DEH	CAN receive rule entry register 5AH Note 1	GAFLIDH5L	GAFLIDH5	R/W	–	√	√	0000H
F03DFH		GAFLIDH5H			–	√		
F03DEH	CAN receive buffer register 3DH Note 2	RMDF33L	RMDF33	R	–	√	√	0000H
F03DFH		RMDF33H			–	√		
F03E0H	CAN receive rule entry register 5BL Note 1	GAFLML5L	GAFLML5	R/W	–	√	√	0000H
F03E1H		GAFLML5H			–	√		
F03E0H	CAN receive buffer register 4AL Note 2	RMIDL4L	RMIDL4	R	–	√	√	0000H
F03E1H		RMIDL4H			–	√		
F03E2H	CAN receive rule entry register 5BH Note 1	GAFLMH5L	GAFLMH5	R/W	–	√	√	0000H
F03E3H		GAFLMH5H			–	√		
F03E2H	CAN receive buffer register 4AH Note 2	RMIDH4L	RMIDH4	R	–	√	√	0000H
F03E3H		RMIDH4H			–	√		
F03E4H	CAN receive rule entry register 5CL Note 1	GAFLPL5L	GAFLPL5	R/W	–	√	√	0000H
F03E5H		GAFLPL5H			–	√		
F03E4H	CAN receive buffer register 4BL Note 2	RMTS4L	RMTS4	R	–	√	√	0000H
F03E5H		RMTS4H			–	√		
F03E6H	CAN receive rule entry register 5CH Note 1	GAFLPH5L	GAFLPH5	R/W	–	√	√	0000H
F03E7H		GAFLPH5H			–	√		
F03E6H	CAN receive buffer register 4BH Note 2	RMPTR4L	RMPTR4	R	–	√	√	0000H
F03E7H		RMPTR4H			–	√		
F03E8H	CAN receive rule entry register 6AL Note 1	GAFLIDL6L	GAFLIDL6	R/W	–	√	√	0000H
F03E9H		GAFLIDL6H			–	√		
F03E8H	CAN receive buffer register 4CL Note 2	RMDF04L	RMDF04	R	–	√	√	0000H
F03E9H		RMDF04H			–	√		
F03EAH	CAN receive rule entry register 6AH Note 1	GAFLIDH6L	GAFLIDH6	R/W	–	√	√	0000H
F03EBH		GAFLIDH6H			–	√		

Notes 1. These registers are allocated to the RAM window 0 for the CAN module (receive rule and CAN RAM test register). When setting these registers, set the RPAGE bit in the GRWCR register to 0.

2. These registers are allocated to the RAM window 1 for the CAN module (receive buffer, receive FIFO buffer, transmit/receive FIFO buffer, transmit buffer, and transmit history data). When setting these registers, set the RPAGE bit in the GRWCR register to 1.

Figure 4-19. Block Diagram of P24



P2: Port register 2
PU2: Pull-up resistor option register 2
PM2: Port mode register 2
PMS: Port mode select register
PITHL2: Port input threshold control register 2
RD: Read signal
WRxx: Write signal

4.3.9 Peripheral I/O redirection register 0 (PIOR0)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.

PIOR0 enables or disables redirection of the timer array unit functions; that is, it specifies which I/O port is assigned to each input pin of timer array unit 0.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 4-100. Format of Peripheral I/O Redirection Register 0 (PIOR0)

Address: F0016H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR0	PIOR07	PIOR06	PIOR05	PIOR04	PIOR03	PIOR02	PIOR01	PIOR00

Bit	Function	144-pin		100-pin		80-pin		64-pin		48-pin	
		Setting value		Setting value		Setting value		Setting value		Setting value	
		0	1	0	1	0	1	0	1	0	1
PIOR07	TI07	P120	P44	P120	P44	P120	P44	P120	—	P120	—
PIOR06	TI06	P14	P02	P14	P02	P14	P02	P14	—	P14	—
PIOR05	TI05	P15	P00	P15	P00	P15	P00	P15	P00	P15	P00
PIOR04	TI04	P13	P01	P13	P01	P13	P01	P13	—	P13	—
PIOR03	TI03	P125	P127	P125	P127	P125	—	P125	—	P125	—
PIOR02	TI02	P16	P67	P16	P67	P16	P67	P16	—	P16	—
PIOR01	TI01	P30	P126	P30	P126	P30	P126	P30	—	P30	—
PIOR00	TI00	P17	P66	P17	P66	P17	P66	P17	—	P17	—

(3) Change the CPU from operating with the high-speed on-chip oscillator clock (B) or operating with the high-speed system clock (C) to operating with the subsystem clock (D).

- Set the RTCLPC bit of the OSMC register.
- Set the SELLOSC bit of the CKSEL register to 0.
- Set the CMC register (EXCLKS = x, OSCSELS = 1, AMPHS[1:0] = xx). **Note**
- Set the XTSTOP bit of the CSC register to 0.
- Wait for oscillation stabilization.
- Set the CSS bit of the CKC register to 1.
- Confirm that the CLS bit of the CKC register is set to 1.

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

(4) Change the CPU from operating with the high-speed on-chip oscillator clock (B) or operating with the high-speed system clock (C) to operating with the low-speed on-chip oscillator clock (M).

- Set the SELLOSC bit of the CKSEL register to 1.
- Set the CMC register (EXCLKS = x, OSCSELS = 1). **Note**
- Set the CSS bit of the CKC register to 1.
- Confirm that the CLS bit of the CKC register is set to 1.

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

(5) Change the CPU from operating with the high-speed on-chip oscillator clock (B) or operating with the high-speed system clock (C) to operating with the PLL clock (K).

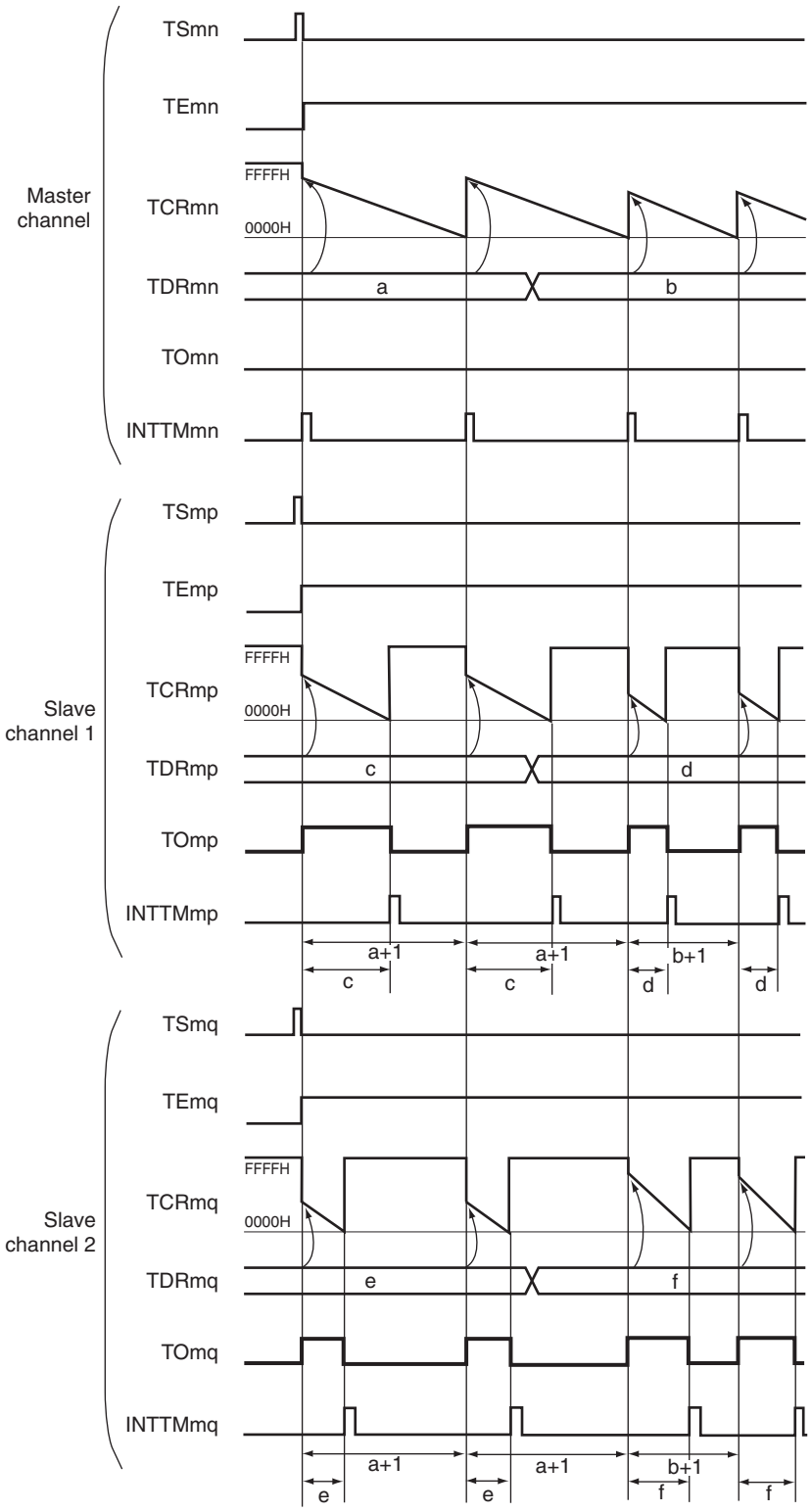
- Set the PLLCTL register (PLLDIV1 = x, LCKSEL[1:0] = xx, PLLDIV0 = x, PLLMUL = x).
- Wait for the selection of the PLL multiplication value to become effective (After setting the PLLMUL bit, wait for at least 1 μs).
- Set the PLLON bit of the PLLCTL register to 1.
- Confirm that the LOCK bit of the PLLSTS register is set to 1 (checking PLL locked state).
- Set the MDIV [2:0] bits of the MDIV register.
- Set the SELPLL bit of the PLLCTL register to 1.
- Confirm that the SELPLLS bit of the PLLSTS register is set to 1.

(6) Change the CPU from operating with the high-speed system clock (C) to operating with the high-speed on-chip oscillator clock (B).

- Set the HIOSTOP bit of the CSC register to 0. **Note**
- Set the MCM0 bit of the CKC register to 0.
- Confirm that the MCS bit of the CKC register is set to 0.

Note When oscillation starts from a high-speed on-chip oscillator clock stop state (HIOSTOP = 1), have the software wait for the following oscillation accuracy stabilization time, and then change the clock.
FRQSEL4 of the user option byte (000C2H/020C2H) = 0: 18 μs to 65 μs
FRQSEL4 of the user option byte (000C2H/020C2H) = 1: 18 μs to 105 μs

Figure 6-80 Example of Basic Timing of Operation as Multiple PWM Output Function (Output two types of PWMs)



(**Remarks** are listed on the next page.)

8.2.9 Timer RD Output Master Enable Register 2 (TRDOER2)

Figure 8-10. Format of Timer RD Output Master Enable Register 2 (TRDOER2)
[PWM Function, Reset Synchronous PWM Mode, Complementary PWM Mode, and PWM3 Mode]

Address: F0268H After Reset: 00H [Note 1]

Symbol	<7>	6	5	4	3	2	1	<0>
TRDOER2	TRDPTO	0	0	0	0	0	0	TRDSHUTS

TRDPTO	INTP0 of pulse output forced cutoff signal input enabled [Note 2]	R/W
0	Pulse output forced cutoff input disabled	R/W
1	Pulse output forced cutoff input enabled (The TRDSHUTS bit is set to 1 when a low level is applied to the INTP0 pin.)	

Bits 6 to 1	Nothing is assigned	R/W
—	The write value must be 0. The read value is 0.	R

TRDSHUTS	Forced cutoff flag	R/W
0	Not forcibly cut off	R/W
1	Forcibly cut off	
This bit is set to 1 when the pulse is forcibly cut off by an INTP0 or ELC input event. This bit is not automatically cleared. To stop the forced cutoff of the pulse, write 0 to this bit while the count is stopped (TSTARTi = 0). The pulse is also forcibly cut off when 1 is written to the TRDSHUTS bit in an enabled mode.		

Notes 1. The value after reset is undefined when FRQSEL4 = 1 in the user option byte (000C2H/020C2H) and TRD0EN = 0 in the PER1 register. If it is necessary to read the initial value, set f_{CLK} to f_{IH} and TRD0EN = 1 before reading.

2. See **8.3.1 (4) Pulse Output Forced Cutoff**.

14.2.5 A/D port configuration register (ADPC)

This register switches the ANI0/P33 to ANI23/P105 pins to digital I/O of port or analog input.

When the comparator is in use, set the pins selected from among P81/ANI3/IVCMP00, P82/ANI4/IVCMP01, P83/ANI5/IVCMP02, P84/ANI6/IVCMP03, and P85/ANI7/IVREF0 to analog input by using the ADPC register.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 14-6. Format of A/D Port Configuration Register (ADPC)

Address: F0076H After reset: 00H

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching																							
					ANI23/P105	ANI22/P104	ANI21/P103	ANI20/P102	ANI19/P101	ANI18/P100	ANI17/P97	ANI16/P96	ANI15/P95	ANI14/P94	ANI13/P93	ANI12/P92	ANI11/P91	ANI10/P90	ANI9/P87	ANI8/P86	ANI7/IVREF0/P85	ANI6/IVCMP03/P84	ANI5/IVCMP02/P83	ANI4/IVCMP01/P82	ANI3/IVCMP00/P81	ANI2/ANO0/P80	ANI1/P34	ANI0/P33
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A
0	0	0	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A
0	0	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A
0	0	1	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A
0	0	1	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A
0	0	1	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A
0	1	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A
0	1	0	0	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A
0	1	0	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A
0	1	0	1	1	D	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A
0	1	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A
0	1	1	0	1	D	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A
0	1	1	1	0	D	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A
0	1	1	1	1	D	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	0	0	0	D	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	0	0	1	D	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	0	1	0	D	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	0	1	1	D	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	1	0	0	D	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	1	0	1	D	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	1	1	0	D	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	0	1	1	1	D	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
1	1	0	0	0	D	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Other than above					Setting prohibited																							

Caution Set the pins to be used for the comparator (P81/ANI3/IVCMP00, P82/ANI4/IVCMP01, P83/ANI5/IVCMP02, P84/ANI6/IVCMP03, and P85/ANI7/IVREF0) to the input mode by using port mode registers 8 (PM8).

16.4.2 Setting transfer clock by using IICWL0 and IICWH0 registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{MCK}}{IICWL0 + IICWH0 + f_{MCK}(t_R + t_F)}$$

At this time, the optimal setting values of the IICWL0 and IICWH0 registers are as follows.
(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$IICWL0 = \frac{0.52}{\text{Transfer clock}} \times f_{MCK}$$
$$IICWH0 = (\frac{0.48}{\text{Transfer clock}} - t_R - t_F) \times f_{MCK}$$

- When the normal mode

$$IICWL0 = \frac{0.47}{\text{Transfer clock}} \times f_{MCK}$$
$$IICWH0 = (\frac{0.53}{\text{Transfer clock}} - t_R - t_F) \times f_{MCK}$$

- When the fast mode plus

$$IICWL0 = \frac{0.50}{\text{Transfer clock}} \times f_{MCK}$$
$$IICWH0 = (\frac{0.50}{\text{Transfer clock}} - t_R - t_F) \times f_{MCK}$$

(2) Setting IICWL0 and IICWH0 registers on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$IICWL0 = 1.3\ \mu s \times f_{MCK}$$
$$IICWH0 = (1.2\ \mu s - t_R - t_F) \times f_{MCK}$$

- When the normal mode

$$IICWL0 = 4.7\ \mu s \times f_{MCK}$$
$$IICWH0 = (5.3\ \mu s - t_R - t_F) \times f_{MCK}$$

- When the fast mode plus

$$IICWL0 = 0.50\ \mu s \times f_{MCK}$$
$$IICWH0 = (0.50\ \mu s - t_R - t_F) \times f_{MCK}$$

(**Cautions** and **Remarks** are listed on the next page.)

(16) LIN/UART Control Register (LCUCn)

Address: F06CEH

	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	OM1	OM0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
0	OM0	LIN Reset	0: LIN reset mode is caused. 1: LIN reset mode is canceled.	R/W
1	OM1	LIN Mode Select	0: LIN wake-up mode is caused. 1: LIN operation mode is caused.	R/W
7 to 2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Set the LCUCn register to 01H to cause a transition to LIN wake-up mode after canceling LIN reset mode, and set the LCUCn register to 03H to cause a transition to LIN operation mode.
In LIN self-test mode, set the LCUCn register to 03H after a transition to LIN self-test mode is completed.
After a value is written to this register, confirm that the value written is actually indicated in the LMSTn register before writing another value.

OM0 bit (LIN reset bit)
The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode.
With 0 set, LIN reset mode is caused.
With 1 set, LIN reset mode is canceled.

OM1 bit (LIN mode select bit)
The OM1 bit selects the specific operation mode (either LIN wake-up mode or LIN operation mode) after canceling LIN reset mode.
With 0 set, LIN wake-up mode is caused.
With 1 set, LIN operation mode is caused.
This register is valid only when the OMM0 bit in the LMSTn register is 1.
Writing a value to this bit is disabled while the FTS bit in the LTRCn register is 1.

(15) LIN/UART Control Register (LCUCn)

Address: F06CEH

	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	OM1	OM0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
0	OM0	LIN Reset	0: LIN reset mode is caused. 1: LIN reset mode is canceled.	R/W
1	OM1	LIN Mode Select	0: LIN wake-up mode is caused. 1: LIN operation mode is caused.	R/W
7 to 2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Set the LCUCn register to 01H to cause a transition to LIN wake-up mode after canceling LIN reset mode, and set the LCUCn register to 03H to cause a transition to LIN operation mode.
In LIN self-test mode, set the LCUCn register to 03H after a transition to LIN self-test mode is completed.
When the LIN/UART module makes a transition from the LIN operating mode to the LIN reset mode while operating as a LIN slave (at a fixed baud rate), write 1 to the LIN0EN bit (or the LIN1EN bit) in the PER2 register after having cleared the given bit to 0.
After a value is written to this register, confirm that the value written is actually indicated in the LMSTn register before writing another value.

OM0 bit (LIN reset bit)
The OM0 bit selects either causing a transition to LIN reset mode or canceling LIN reset mode.
With 0 set, LIN reset mode is caused.
With 1 set, LIN reset mode is canceled.

OM1 bit (LIN mode select bit)
The OM1 bit selects the specific operation mode (either LIN wake-up mode or LIN operation mode) after canceling LIN reset mode.
With 0 set, LIN wake-up mode is caused.
With 1 set, LIN operation mode is caused.
This register is valid only when the OMM0 bit in the LMSTn register is 1.
Writing a value to this bit is disabled while the FTS bit in the LTRCn register is 1.

(23) LIN/UART Data Buffer m Register (LDBnm) (m = 1 to 8)

Address: LDBn1 F06D8H, LDBn2 F06D9H, LDBn3 F06DAH, LDBn4 F06DBH, LDBn5 F06DCH, LDBn6 F06DDH, LDBn7 F06DEH, LDBn8 F06DFH

	7	6	5	4	3	2	1	0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
7 to 0	Sets the data to be transmitted or allows the received data to be read.	00H to FFH	R/W

For response transmission:
These registers set the data to be transmitted in the response field.
Set these registers when the RTS bit is 0 (response reception/transmission is halted).

For response reception:
These registers hold the data received in the response field.
The received data is overwritten. If an error is detected, the data prior to reception interruption is stored in the register.
Do not read these registers when the RTS bit is 1 (response transmission/reception is started)

In LIN self-test mode, this register operates as follows:
Write the value to be transmitted before communication. The reversed value of the value received can be read from the register after frame transmission/reception is completed (after loopback).
For details of LIN self-test mode, refer to **17.6 LIN Self-Test Mode**.

Figure 22-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H, MK3L, MK3H) (2/2)

Address: FFFD7H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK3H	–	–	–	PMK14 LIN2WUPMK	CAN1TRMMK	CAN1CFRMK	CAN1WUPMK	CAN1ERRMK

MKxx	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution The above is the bit layout for the 144-pin. The available bits differ depending on the product. For details about the bits available for each product, see Table 22-2. Be sure to set bits that are not available to 1.

Table 24-1. Operating Statuses in HALT Mode (2/2)

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock		When HALT Instruction Is Executed While CPU Is Operating on Low-speed On-chip Oscillator Clock (f_{IL})
			When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})	
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Operation disabled		
		f_X			
		f_{EX}			
		f_{PLL}			
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped)	Cannot operate	Cannot operate
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped)	
	f_{IL}		Set by bit 1 (HPIEN) of on-chip debug option byte (000C3H/020C3H), bit 0 (SELLOSC) of the CKSEL register, and bit 4 (WUTMMCK0) of the OSMC register. • WUTMMCK0 = 1: Oscillates • WUTMMCK0 = 0 and SELLOSC = 1: Oscillates • WUTMMCK0 = 0, SELLOSC = 0, and HPIEN = 1: Oscillates • WUTMMCK0 = 0, SELLOSC = 0, and HPIEN = 0: Stops		
f_{WDT}			Set by bits 0 (WDSTBYON) and 4 (WDTON) of user option byte (000C0H/020C0H) • WDTON = 0: Stops • WDTON = 1 and WDSTBYON = 1: Oscillates • WDTON = 1 and WDSTBYON = 0: Stops		
CPU			Operation stopped		
Code flash memory					
Data flash memory					
RAM			Operation stopped (operation can continue during DTC transfer)		
Port (latch)			Status before HALT mode was set is retained		
Timer array unit			Operable (Operation is disabled while in the low consumption RTC mode)		
Real-time clock (RTC)			Operable		
Watchdog timer			See **CHAPTER 11 WATCHDOG TIMER**		
Clock monitor			Operation stopped		
Timer RJ			Operable (Operation is disabled while in the low consumption RTC mode)		
Timer RD					
Clock output/buzzer output					
A/D converter			Operation disabled		
D/A converter					
Comparator					
Serial array unit (SAU)			Operable (Operation is disabled while in the low consumption RTC mode)		
Serial interface (IICA)			Operation disabled		
DTC			Operable		
ELC			Linking between operational function blocks is possible.		
LIN/UART module (RLIN3)			Operation disabled		
CAN interface (RS-CAN lite)					
IEBus Controller					
Power-on-reset function			Operable		
Voltage detection function					
External interrupt					
Key interrupt function					

CHAPTER 26 POWER-ON-RESET CIRCUIT

26.1 Functions of Power-on-reset Circuit

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on.
  The reset signal is released when the supply voltage (V_{DD}) exceeds 1.56 V (typ.).

- Compares supply voltage (V_{DD}) and detection voltage (V_{PDR} = 1.55 V (typ.)), generates internal reset signal when $V_{DD} < V_{PDR}$.

Caution If an internal reset signal is generated in the POR circuit, the POCRES_0 and CLKRF flags of the POR/CLM reset confirmation register (POCRES) and the TRAP, WDCLRF, IAWRF, and LVIRF flags of the reset control flag register (RESF) are cleared (00H).

Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the RESF and POCRES registers for when an internal reset signal is generated by the power-on reset (POR), watchdog timer (WDT), clock monitor, voltage detector (LVD), illegal instruction execution, or illegal-memory access. The RESF register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the watchdog timer (WDT), voltage detector (LVD), illegal instruction execution, clock monitor, or illegal-memory access. The POCRES register is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by the clock monitor.
For details of the POCRES and RESF registers, see **CHAPTER 25 RESET FUNCTION**.

28.3.4 CPU stack pointer monitor function

The CPU stack pointer monitor is used to detect overflows and underflows of the stack pointer and to generate interrupts in response.

Caution The CPU stack pointer monitor function is disabled during on-chip debugging.

<Configuration>

This function has the following functions.

- SP overflow/underflow detection function
- SP overflow/underflow interrupt output function

When the SPM enable bit (SPMEN) is 1, an interrupt signal (INTSPM) is generated if the monitored stack pointer value is greater than the specified SFR value (SPOFR) or smaller than the specified SFR value (SPUFR).

When the SPM enable bit (SPMEN) is 1, writing to the SPOFR and SPUFR registers is invalid.

<Register setting method>

Figure 28-14 shows the register setting method of this function.

Figure 28-14. Register Setting Flow

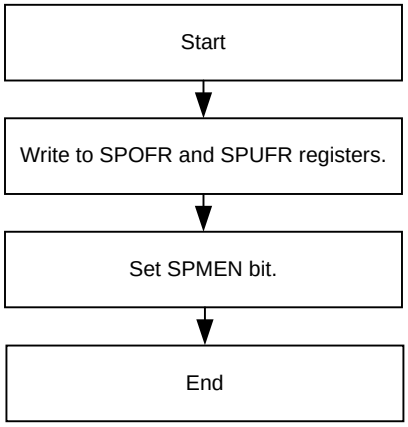


Table 34-5. Operation List (17/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
Stack manipulate	PUSH	PSW	2	1	–	(SP – 1) ← PSW, (SP – 2) ← 00H, SP ← SP–2			
		rp	1	1	–	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
	POP	PSW	2	3	–	PSW ← (SP+1), SP ← SP + 2	R	R	R
		rp	1	1	–	rp_L ←(SP), rp_H ← (SP+1), SP ← SP + 2			
	MOVW	SP, #word	4	1	–	SP ← word			
		SP, AX	2	1	–	SP ← AX			
		AX, SP	2	1	–	AX ← SP			
		HL, SP	3	1	–	HL ← SP			
		BC, SP	3	1	–	BC ← SP			
		DE, SP	3	1	–	DE ← SP			
	ADDW	SP, #byte	2	1	–	SP ← SP + byte			
	SUBW	SP, #byte	2	1	–	SP ← SP – byte			
Unconditional branch	BR	AX	2	3	–	PC ← CS, AX			
		$addr20	2	3	–	PC ← PC + 2 + jdisp8			
		$!addr20	3	3	–	PC ← PC + 3 + jdisp16			
		!addr16	3	3	–	PC ← 0000, addr16			
		!!addr20	4	3	–	PC ← addr20			
Conditional branch	BC	$addr20	2	2/4 Note3	–	PC ← PC + 2 + jdisp8 if CY = 1			
	BNC	$addr20	2	2/4 Note3	–	PC ← PC + 2 + jdisp8 if CY = 0			
	BZ	$addr20	2	2/4 Note3	–	PC ← PC + 2 + jdisp8 if Z = 1			
	BNZ	$addr20	2	2/4 Note3	–	PC ← PC + 2 + jdisp8 if Z = 0			
	BH	$addr20	3	2/4 Note3	–	PC ← PC + 3 + jdisp8 if (Z∨CY)=0			
	BNH	$addr20	3	2/4 Note3	–	PC ← PC + 3 + jdisp8 if (Z∨CY)=1			
	BT	saddr.bit, $addr20	4	3/5 Note3	–	PC ← PC + 4 + jdisp8 if (saddr).bit = 1			
		sfr.bit, $addr20	4	3/5 Note3	–	PC ← PC + 4 + jdisp8 if sfr.bit = 1			
		A.bit, $addr20	3	3/5 Note3	–	PC ← PC + 3 + jdisp8 if A.bit = 1			
		PSW.bit, $addr20	4	3/5 Note3	–	PC ← PC + 4 + jdisp8 if PSW.bit = 1			
		[HL].bit, $addr20	3	3/5 Note3	6/7	PC ← PC + 3 + jdisp8 if (HL).bit = 1			
		ES:[HL].bit, $addr20	4	4/6 Note3	7/8	PC ← PC + 4 + jdisp8 if (ES, HL).bit = 1			

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

3. This indicates the number of clocks “when condition is not met/when condition is met”.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

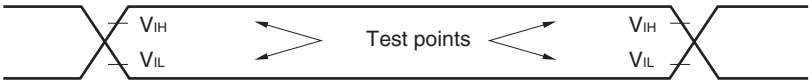
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Port output rise time, port output fall time	t_{RO}, t_{FO}	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to 157, P160 to 167 (normal slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			25	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V		25 Note	60	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			100	ns

Note T_A = +25°C, EV_{DD0} = 5.0 V

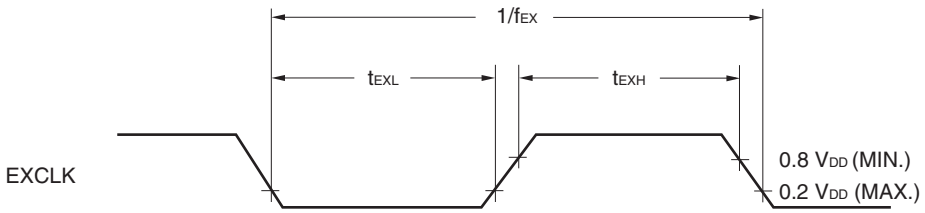
Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency

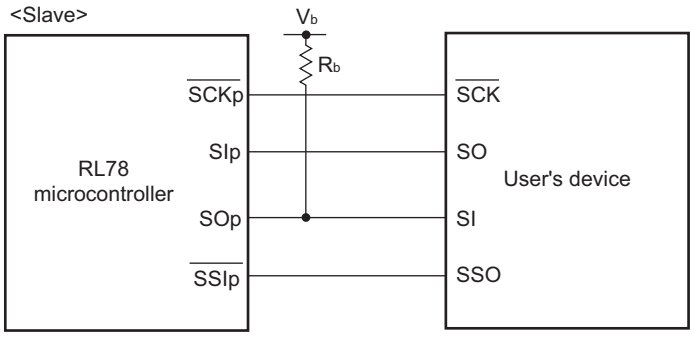
AC Timing Test Points



External System Clock Timing



CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp, $\overline{\text{SCKp}}$ and $\overline{\text{SSIp}}$ pins and N-ch open-drain output mode for the SOp pin.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V