Renesas Electronics America Inc - R5F113TJLFB#V5 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, CSI, I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	130
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 31x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f113tjlfb-v5

4.6.2 Notes on specifying the pin settings

For an output pin to which multiple functions are assigned, the output of the unused alternate functions must be set to its initial state so as to prevent conflicting outputs. This also applies to the functions assigned by using the peripheral I/O redirection register (PIOR). For details about the alternate function output, see **4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function**.

Set PIOR register before the target function is enabled.

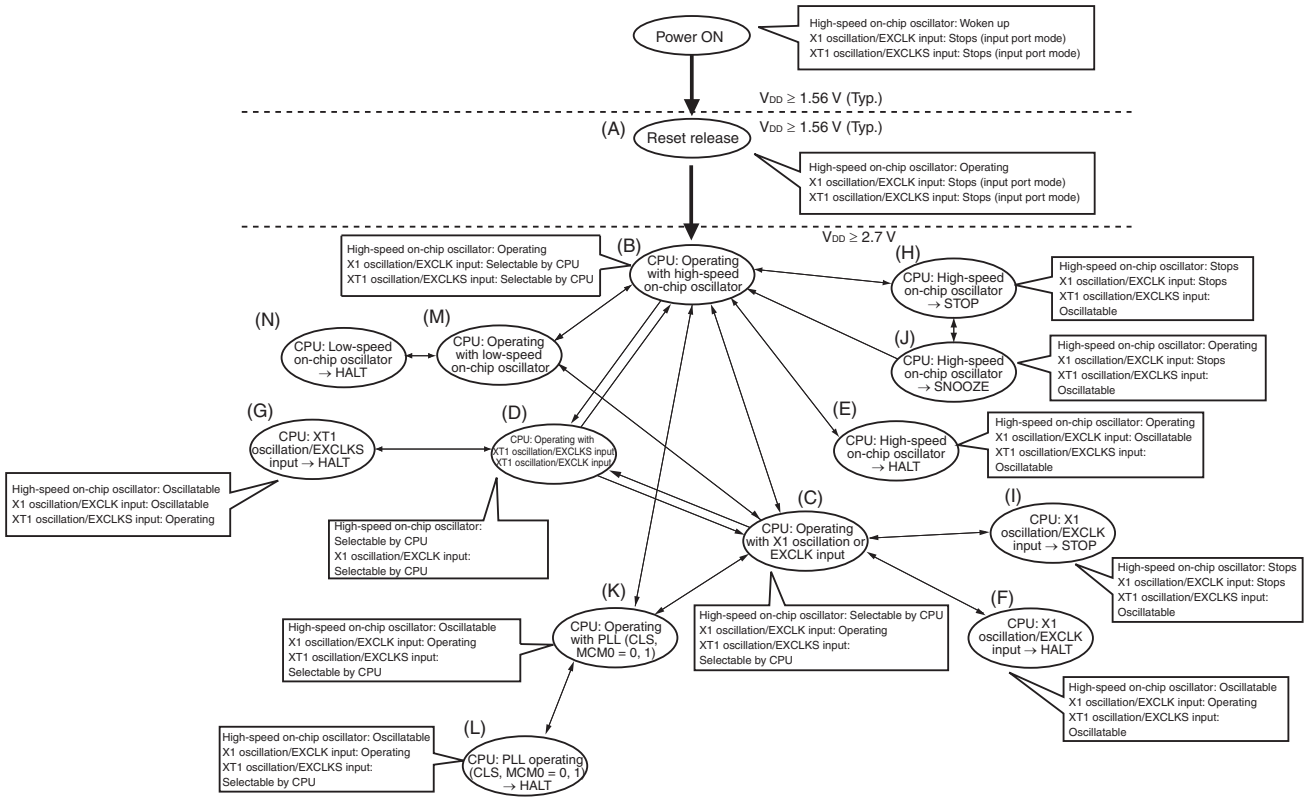
No specific setting is required for input pins because the output of their alternate functions is disabled (the buffer output is Hi-Z).

Disabling the unused functions, including blocks that are only used for input or do not have I/O, is recommended for lower power consumption.

5.6.6 CPU Clock Status Transition Diagram

Figure 5-24 shows the CPU clock status transition diagram of this product.

Figure 5-24. CPU Clock Status Transition Diagram



Caution Transitions in the order of (B) → (D) → (C) or (C) → (D) → (B) are prohibited.

The following shows an example of changing the CPU clock and setting the SFR register.

(1) After reset release (A), change the CPU to operating with the high-speed on-chip oscillator clock (B).

(A)→(B): Setting the SFR register is not required (initial status after reset release).

(2) Change the CPU from operating with the high-speed on-chip oscillator clock (B) to operating with the high-speed system clock (C).

- Set the CMC register (EXCLK = 0, OSCSEL = 1, AMPH = x). **Note 1**
- Set the OSTS register. **Note 2**
- Set the MSTOP bit of the CSC register to 0.
- Check the oscillation stabilization time by using the OSTC register. **Note 2**
- Set the MCM0 bit of the CKC register to 1.
- Set the MCS bit of the CKC register to 1.

Notes 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

2. Set the oscillation stabilization time of the oscillation stabilization time select register (OSTS) as shown below:

OSTS register setting value ≥ Expected oscillation stabilization time counter status register (OSTC)

6.3.16 Noise filter enable registers 1, 2, 3 (NFEN1, NFEN2, NFEN3)

The NFEN1, NFEN2, NFEN3 registers is used to set whether the noise filter can be used for the timer input signal to each channel.

Enable the noise filter by setting the corresponding bits to 1 on the pins in need of noise removal.

When the noise filter is ON, match detection and synchronization of the 2 clocks is performed with the CPU/peripheral hardware clock (f_{MCK}). When the noise filter is OFF, only synchronization is performed with the CPU/peripheral hardware clock (f_{MCK}) **Note**.

Set the NFEN1, NFEN2 and NFEN3 registers by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Note For details, see **6.5.1 (2) When valid edge of input signal via the TImn pin is selected (CCSmn = 1)** and **6.5.2 Start timing of counter**.

Remark NFEN3 register is not incorporated in 100-pin, 80-pin, 64-pin, and 48-pin products.

6.3.17 Port mode registers 0, 1, 3, 4, 5, 6, 7, 11, 12, 14 (PM0, PM1, PM3, PM4, PM5, PM6, PM7, PM11, PM12, PM14)

These registers set input/output of ports 0, 1, 3, 4, 5, 6, 7, 11, 12, 14 in 1-bit units.

The presence or absence of timer I/O pins depends on the product.

When using the ports (such as P17/TO00/TI00 and P16/TO2/TI02) to be shared with the timer output pin for timer output, set the port mode register (PMxx) bit and port register (Pxx) bit corresponding to each port to “0”.

Example: When using P16/TO02/TI02 for timer output

Set the PM16 bit of port mode register 1 to 0.

Set the P16 bit of port register 1 to 0.

When using the ports (such as P17/TO00/TI00 and P16/TO2/TI02) to be shared with the timer output pin for timer input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P16/TO02/TI02 for timer input

Set the PM16 bit of port mode register 1 to 1.

P16 bit of port register may be 0 or 1.

Set the PM0, PM1, PM3, PM4, PM5, PM6, PM7, PM11, PM12 and PM14 registers by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

9.3.7 Real-time clock control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

Set the RTCC1 register by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-8. Format of Real-time Clock Control Register 1 (RTCC1) (1/2)

Address: FFF9EH After reset: 00H R/W Note

Symbol	<7>	<6>	5	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT

WALE	Alarm operation control
0	Match operation is invalid.
1	Match operation is valid.
When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG and RTCIF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of real-time clock control register 1 (RTCC1), the alarm minute register (ALARMWM), the alarm hour register (ALARMWH), and the alarm week register (ALARMWW)), set match operation to be invalid (“0”) for the WALE bit.	

WALIE	Control of alarm interrupt (INTRTC) function operation
0	Does not generate interrupt on matching of alarm.
1	Generates interrupt on matching of alarm.

WAFG	Alarm detection status flag
0	Alarm mismatch
1	Detection of matching of alarm
This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to “1”, one operating clock (f_{RTC}) after matching of the alarm is detected. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

Note Bit 1 is read-only.

Table 9-2 shows the relationship between the setting value of the AMPM bit, the hour count register (HOUR) value, and time.

Table 9-2. Displayed Time Digits

24-Hour Display (AMPM = 1)		12-Hour Display (AMPM = 1)	
Time	HOUR Register	Time	HOUR Register
0	00H	12 a.m.	12H
1	01H	1 a.m.	01H
2	02H	2 a.m.	02H
3	03H	3 a.m.	03H
4	04H	4 a.m.	04H
5	05H	5 a.m.	05H
6	06H	6 a.m.	06H
7	07H	7 a.m.	07H
8	08H	8 a.m.	08H
9	09H	9 a.m.	09H
10	10H	10 a.m.	10H
11	11H	11 a.m.	11H
12	12H	12 p.m.	32H
13	13H	1 p.m.	21H
14	14H	2 p.m.	22H
15	15H	3 p.m.	23H
16	16H	4 p.m.	24H
17	17H	5 p.m.	25H
18	18H	6 p.m.	26H
19	19H	7 p.m.	27H
20	20H	8 p.m.	28H
21	21H	9 p.m.	29H
22	22H	10 p.m.	30H
23	23H	11 p.m.	31H

The HOUR register value is set to 12-hour display when the AMPM bit is “0” and to 24-hour display when the AMPM bit is “1”.

In 12-hour display, the fifth bit of the HOUR register displays 0 for AM and 1 for PM.

9.3.15 Watch error correction register (SUBCUD)

This register is used to correct the watch with high accuracy when it is slow or fast by changing the value that overflows from the internal counter (16 bits) to the second count register (SEC) (reference value: 7FFFH).

Set the SUBCUD register by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-16. Format of Watch Error Correction Register (SUBCUD)

Address: FFF99H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SUBCUD	DEV	F12	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch error when the second digits are at 00, 20, or 40 (every 20 seconds).
1	Corrects watch error only when the second digits are at 00 (every 60 seconds).
Writing to the SUBCUD register at the following timing is prohibited. • When DEV = 0 is set: For a period of SEC = 00H, 20H, 40H • When DEV = 1 is set: For a period of SEC = 00H	

F12	Setting of watch error correction value
0	Increases by {(F5, F4, F3, F2, F1, F0) – 1} × 2.
1	Decreases by {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2.
When (F12, F5, F4, F3, F2, F1, F0) = (*, 0, 0, 0, 0, 0, *), the watch error is not corrected. Range of correction value: (when F12 = 0) 2, 4, 6, 8, … , 120, 122, 124 (when F12 = 1) –2, –4, –6, –8, … , –120, –122, –124	

Cautions 1. / of /Fn (n = 0 to 5) means invert.

2. * means 0 or 1.

The range of value that can be corrected by using the watch error correction register (SUBCUD) is shown below.

	DEV = 0 (correction every 20 seconds)	DEV = 1 (correction every 60 seconds)
Correctable range	–189.2 ppm to 189.2 ppm	–63.1 ppm to 63.1 ppm
Maximum excludes quantization error	± 1.53 ppm	± 0.51 ppm
Minimum resolution	± 3.05 ppm	± 1.02 ppm

Remark If a correctable range is –63.1 ppm or lower and 63.1 ppm or higher, set 0 to DEV.

12.6.8 Hardware trigger no-wait mode (scan mode, one-shot conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.

<3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.

<4> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated.

<5> After A/D conversion of the four channels ends, the ADCS bit remains set to 1, and the system enters the A/D conversion standby status.

<6> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.

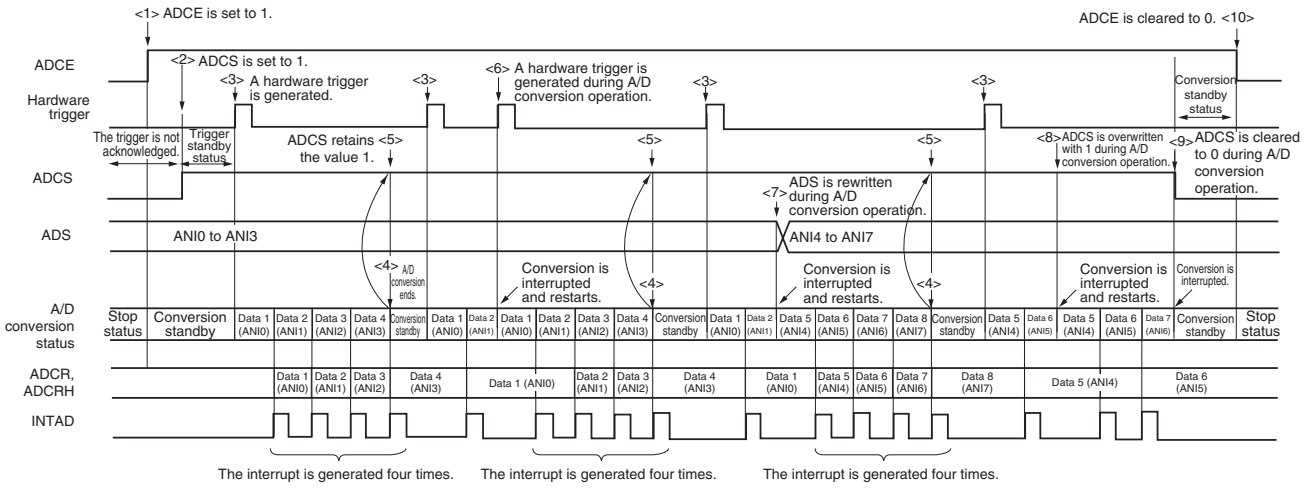
<7> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.

<8> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel. The partially converted data is discarded.

<9> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.

<10> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 12-27. Example of Hardware Trigger No-Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



12.6.12 Hardware trigger wait mode (scan mode, one-shot conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> If a hardware trigger is input while in the hardware trigger standby status, A/D conversion is performed on the four analog input channels specified by scan 0 to scan 3, which are specified by the analog input channel specification register (ADS). The ADCS bit of the ADM0 register is automatically set to 1 according to the hardware trigger input. A/D conversion is performed on the analog input channels in order, starting with that specified by scan 0.

<3> A/D conversion is sequentially performed on the four analog input channels, the conversion results are stored in the A/D conversion result register (ADCR, ADCRH) each time conversion ends, and the A/D conversion end interrupt request signal (INTAD) is generated.

<4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the A/D converter enters the stop status.

<5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts at the first channel. The partially converted data is discarded.

<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the first channel respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, the system enters the hardware trigger standby status, and the A/D converter enters the stop status. When ADCE = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 12-31. Example of Hardware Trigger Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing

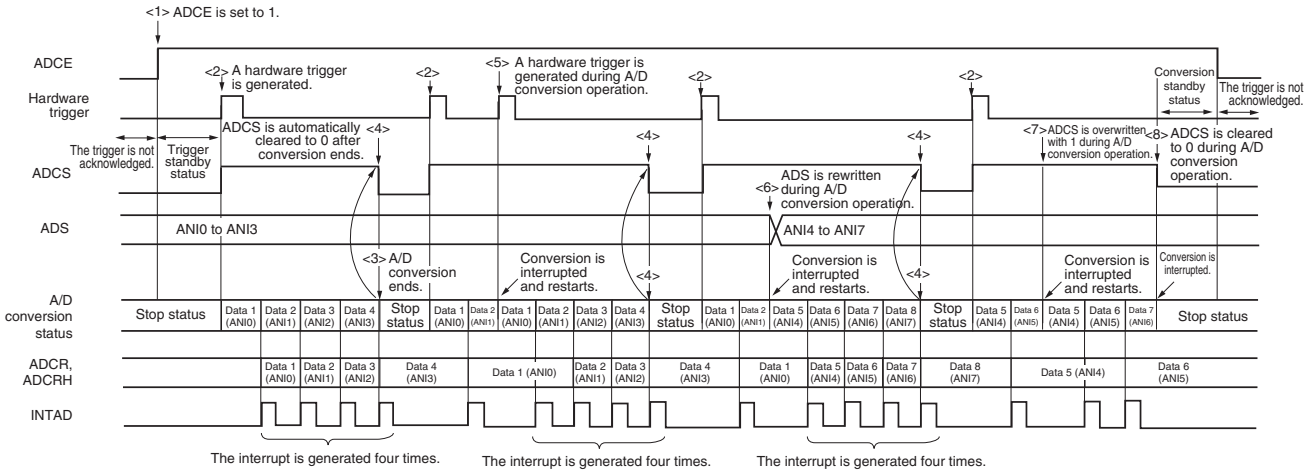
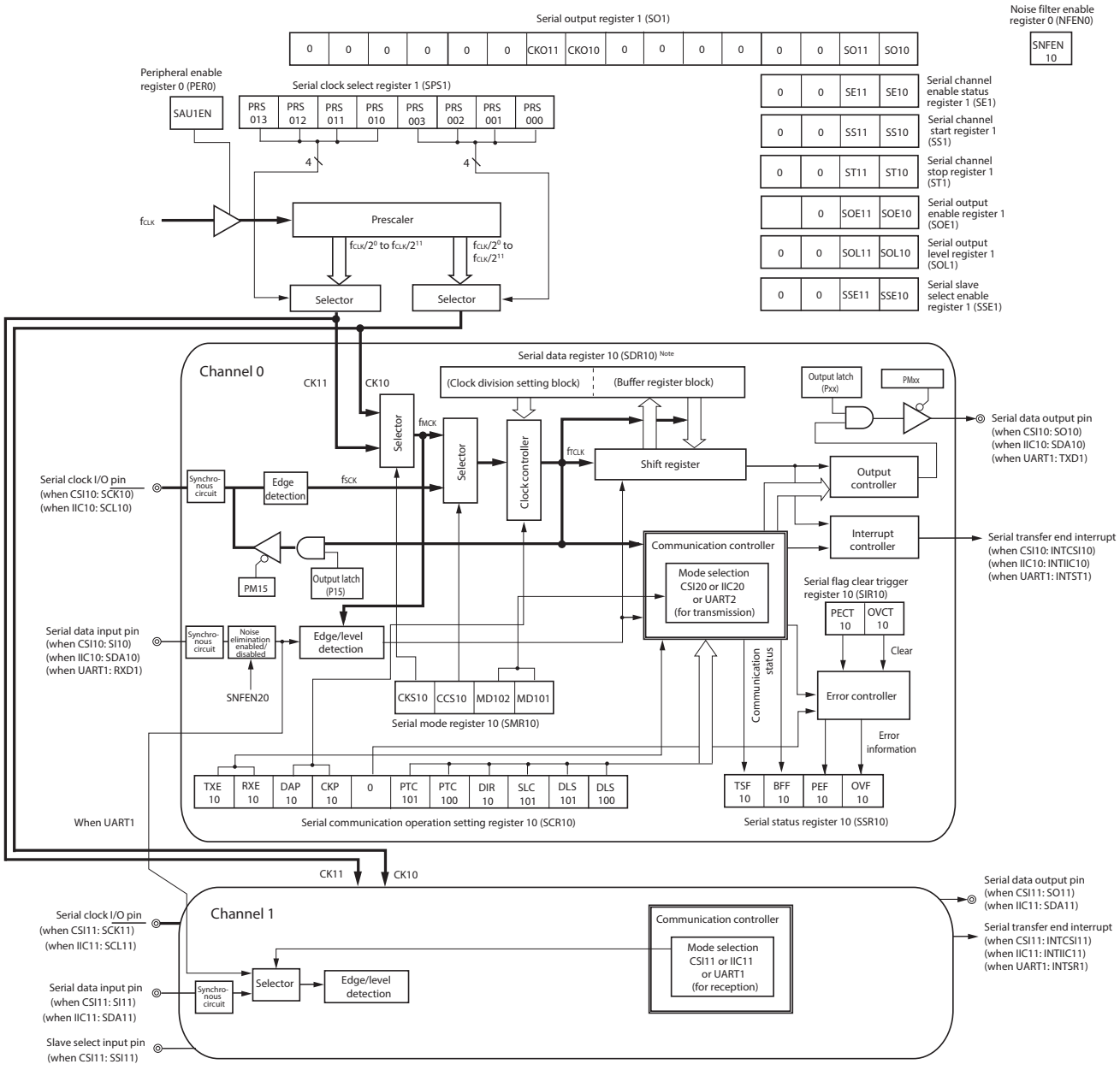


Figure 15-2 shows the block diagram of the serial array unit 1.

Figure 15-2. Block Diagram of Serial Array Unit 1



Caution: If operation is stopped (SEmn = 0), the upper 7 bits set the clock division, and the lower bits have no meaning.

If operation is in progress (SEmn = 1), the serial data register 10 functions as the buffer register.

Figure 15-13. Format of Serial Status Register mn (SSRmn) (2/2)

Address: F0100H, F0101H (SSR00), F0102H, F0103H (SSR01), After reset: 0000H R
F0140H, F0141H (SSR10), F0142H, F0143H (SSR11)
F0140H, F0141H (SSR20), F0142H, F0143H (SSR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSRmn	0	0	0	0	0	0	0	0	0	TSF mn	BFF mn	0	0	FEF mn	PEF mn	OVF mn

FEFmn	Framing error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception).

<Clear condition>
- 1 is written to the FECTmn bit of the SIRmn register.

<Set condition>
- A stop bit is not detected when UART reception ends.

PEF mn	Parity error detection flag of channel n
0	No error occurs.
1	An error occurs (during UART reception) or ACK is not detected (during I^2C transmission).

<Clear condition>
- 1 is written to the PECTmn bit of the SIRmn register.

<Set condition>
- The parity of the transmit data and the parity bit do not match when UART reception ends (parity error).
- No ACK signal is returned from the slave channel at the ACK reception timing during I^2C transmission (ACK is not detected).

OVF mn	Overrun error detection flag of channel n
0	No error occurs.
1	An error occurs.

<Clear condition>
- 1 is written to the OVCTmn bit of the SIRmn register.

<Set condition>
- Even though receive data is stored in the SDRmn register, that data is not read and transmit data or the next receive data is written while the RXEmn bit of the SCRmn register is set to 1 (reception or transmission and reception mode in each communication mode).
- Transmit data is not ready for slave transmission or transmission and reception in CSI mode.

Remark m: Unit number (m = 0-2), n: Channel number (n = 0, 1)

- RFEMP Flag
  This flag is set to 1 when all messages in the receive FIFO buffer have been read. This flag is also set to 1 when the RFE bit in the RFCCm register is 0 or in global reset mode.
  This flag is cleared to 0 when even a single received message has been stored in the receive FIFO buffer.

20.2.6 DTC Base Address Register (DTCBAR)

This is an 8-bit register used to set the following addresses: the vector address where the start address of the DTC control data area is stored and the address of the DTC control data area. The value of the DTCBAR register is handled as the higher 8 bits to generate a 16-bit address.

Cautions 1. Modify the DTCBAR register value with all DTC activation sources set to activation disabled.
2. Do not rewrite the DTCBAR register more than once.
3. Do not access the DTCBAR register using a DTC transfer.
4. For the allocation of the DTC control data area and the DTC vector table area, refer to 20.2.1 Allocation of DTC Control Data Area and DTC Vector Table Area.

Figure 20-6. Format of DTC Base Address Register (DTCBAR)

Address: F02E0H After reset: FDH

Symbol	7	6	5	4	3	2	1	0
DTCBAR	DTCBAR7	DTCBAR6	DTCBAR5	DTCBAR4	DTCBAR3	DTCBAR2	DTCBAR1	DTCBAR0

Table 21-3. Correspondence Between Values Set to ELSELRn (n = 00 to 25) Registers and Operation of Link Destination Peripheral Functions at Reception

Bits ELSELRn3 to ELSELRn0 in ELSELRn Register	Link Destination Peripheral Function	Operation When Receiving Event
0001B	A/D converter	A/D conversion starts
0010B	Timer input of timer array unit 0 channel 0 Notes 1 and 2	Delay counter, input pulse interval measurement, external event counter
0011B	Timer input of timer array unit 0 channel 1 Notes 1 and 2	
0100B	Timer RJ0	Count source
0101B	Timer RD0	TRDIOD0 input capture, pulse output cutoff
0110B	Timer RD1	TRDIOD1 input capture, pulse output cutoff
0111B	DA0 Note 3	Real-time output
1000B	Timer input of timer array unit 0 channel 2 Notes 1 and 2	Delay counter, input pulse interval measurement, external event counter
1001B	Timer input of timer array unit 0 channel 3 Notes 1 and 2	

Notes 1. To select the timer input of timer array unit 0 channel m as the link destination peripheral function, first set the operating clock for channel m to f_{CLK} using timer clock select register 0 (TPS0), and then set the timer output used for channel m to an event input signal from the ELC using timer input select register 0 (TIS0).

2. Before selecting the timer input of timer array unit 0 channel m as the link destination peripheral function, set the noise filter of the corresponding link destination channel in the timer array unit 0 to OFF (set the TNFEN0m bit to 0) by using the noise filter enable register 1 (NFEN1).

3. When entering the STOP status while the real-time output event mode for D/A conversion is enabled, disable linking of ELC events before entering STOP.

Remark m = 0, 3

Table 22-1. Interrupt Source List (5/5)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	144-pin	100-pin	80-pin	64-pin	48-pin
		Name	Trigger								
Maskable	53	INTTM15 Note 6	End of TAU1 channel 5 count/capture	Internal	006EH		√	√	√	√	√
		INTTM25 Note 6	End of TAU2 channel 5 count/capture				√	–	–	–	–
	54	INTTM16 Note 7	End of TAU1 channel 6 count/capture		0070H		√	√	√	√	√
		INTTM26 Note 7	End of TAU2 channel 6 count/capture				√	–	–	–	–
	55	INTTM17 Note 8	End of TAU1 channel 7 count/capture		0072H		√	√	√	√	√
		INTTM27 Note 8	End of TAU2 channel 7 count/capture				√	–	–	–	–
	56	INTCAN1ERR	CAN1 channel error		0074H		√	√	√	√	√
	57	INTCAN1WUP	CAN1 wakeup	External	0076H	(D)	√	√	√	√	√
	58	INTCAN1CFR	CAN1 transmit/receive FIFO receive	Internal	0078H	(A)	√	√	√	√	√
	59	INTCAN1TRM	CAN1 channel transmit		007AH		√	√	√	√	√
	60	INTP14 Note 5	Pin input edge detection 14	External	007CH	(B)	√	–	–	–	–
		INTLIN2WUP Note 5	LIN2 reception pin input			(E)	√	√	–	–	–
Software	–	BRK	Execution of BRK instruction	–	007EH	(F)	√	√	√	√	√
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–	√	√	√	√	√
		POR	Power-on-reset				√	√	√	√	√
		LVD	Voltage detection Note 3				√	√	√	√	√
		WDT	Overflow of watchdog timer				√	√	√	√	√
		TRAP	Execution of illegal instruction Note 4				√	√	√	√	√
		IAW	Illegal-memory access				√	√	√	√	√
		CLM	Main clock oscillation stop				√	√	√	√	√

(**Notes** are listed on the next page.)

24.2.3 STOP status output control register (STPSTC)

The port latch of P31 or P52 can be inverted in response to a source condition for release from the STOP mode being generated or a transition from SNOOZE mode to normal mode.

Set the STPSTC register by a 1-bit or 8-bit memory manipulation instruction.

Writing to the STPSTC register is disabled when the GCSC bit of the IAWCTL register is set to 1.

Reset signal generation clears this register to 00H.

Cautions When the STOP status output control register is to be used, the target port pin should be placed in the output mode and the port latch should be set to 0 beforehand.

Figure 24-3. Format of STOP Status Output Control Register (STPSTC)

Address: F02CAH After reset: 00H R/W

Symbol	<7>	6	5	<4>	3	2	1	<0>
STPSTC	STPOEN	0	0	STPLV Note 1	0	0	0	STPSEL Note 2

STPOEN	Enabling or disabling of STOPST output
0	Nothing is done when this LSI is released from the STOP mode.
1	The STPLV value is output on the pin selected by STPSEL when this LSI is released from the STOP mode.

STPLV Note 1	Control of STOPST output level
0	Output low
1	Output high

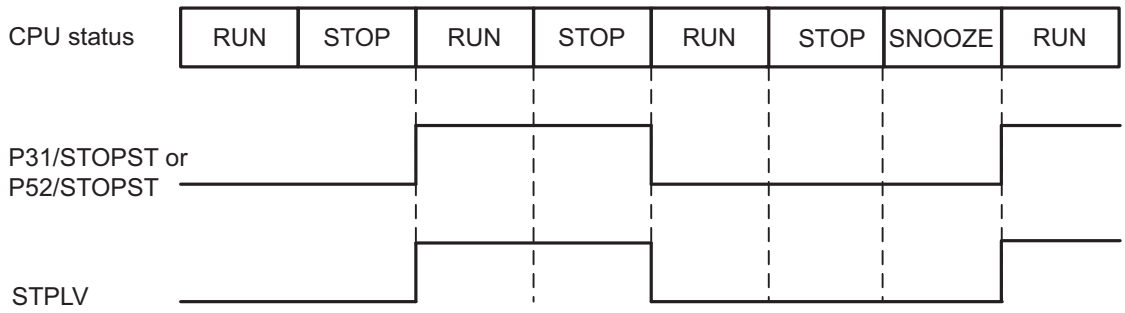
STPSEL Note 2	Control of STOPST pin selection
0	Selects P31
1	Selects P52

Notes 1. The STPLV bit is inverted when this LSI is released from the STOP mode and when this LSI makes a transition from SNOOZE mode to normal mode.

2. Bit 0 is a read-only reserved bit in 48-pin products. When setting the register, write the initial value, 0, to this bit.

Caution Be sure to set bits 1 to 3, 5, and 6 of the STPSTC register to 0.

The following figure shows the timing of the STOPST pin and STPLV bit during CPU operation status.



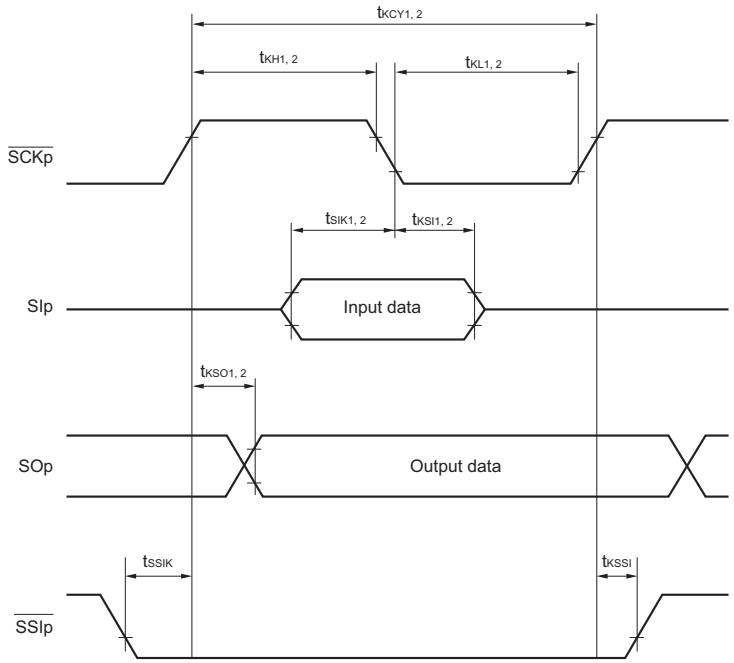
(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/3)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Notes 1, 2]	I_{SNOZ}	SNOOZE mode	A/D converter operation	During mode transition			1.0	1.7	mA
				During conversion	Low-voltage mode AV_{REFP} = V_{DD} = 5.0 V		2.1	3.4	mA
			DTC operation				5.5		mA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, EV_{DD1}, V_{SS}, EV_{SS0}, or EV_{SS1}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

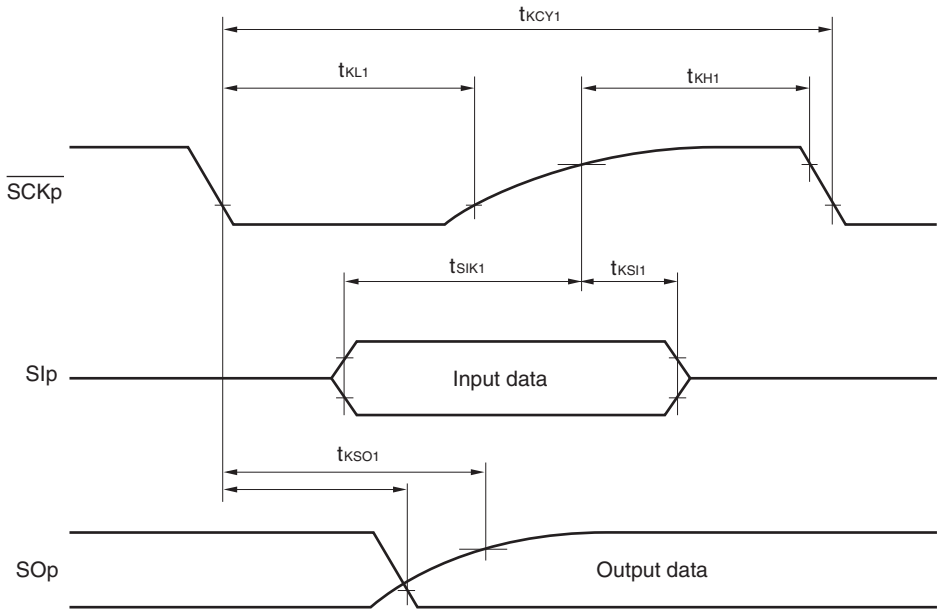
2. The values below the MAX. column include the STOP leakage current.

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)

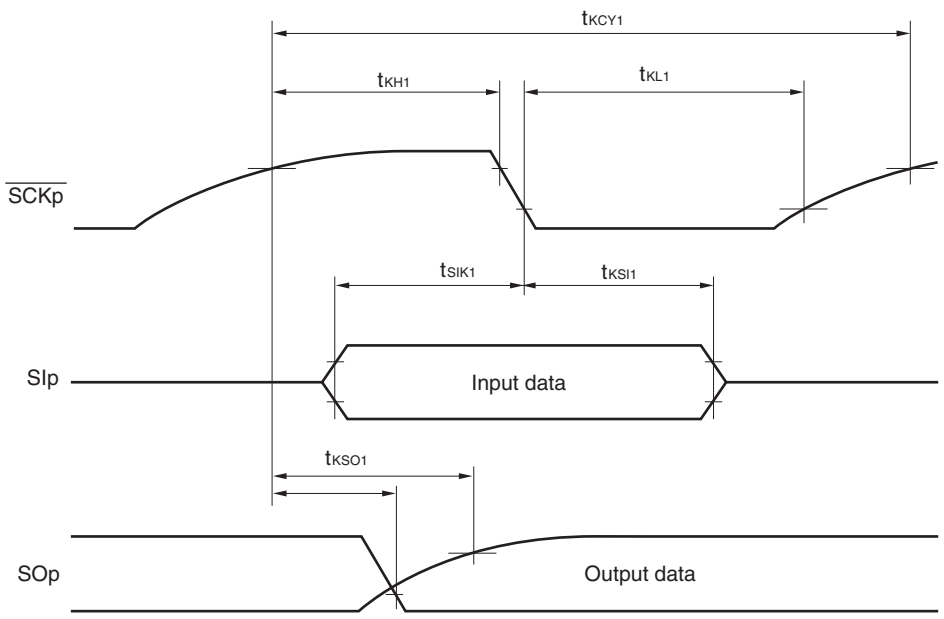


Remark p: CSIp (p = 00, 01, 10, 11, 20, 21), $\overline{\text{SSIp}}$ (p = 00, 01, 10, 11), m: Unit m (m = 0 to 2), n: Channel n (n = 0, 1)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



35.5.3 On-chip Debug (UART)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	-		115.2 k		1 M	bps

35.5.4 LIN/UART Module (RLIN3) UART Mode

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	-	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 to 32 MHz			5333	kbps
		SNOOZE mode	LIN communication clock source (f_{CLK}): 1 to 32 MHz FRQSEL4 = 0 in the user option byte (000C2H/020C2H)			4.8	
			LIN communication clock source (f_{CLK}): 1 to 32 MHz FRQSEL4 = 1 in the user option byte (000C2H/020C2H)			2.4	