# Renesas Electronics America Inc - R5F113TJLFB#X0 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

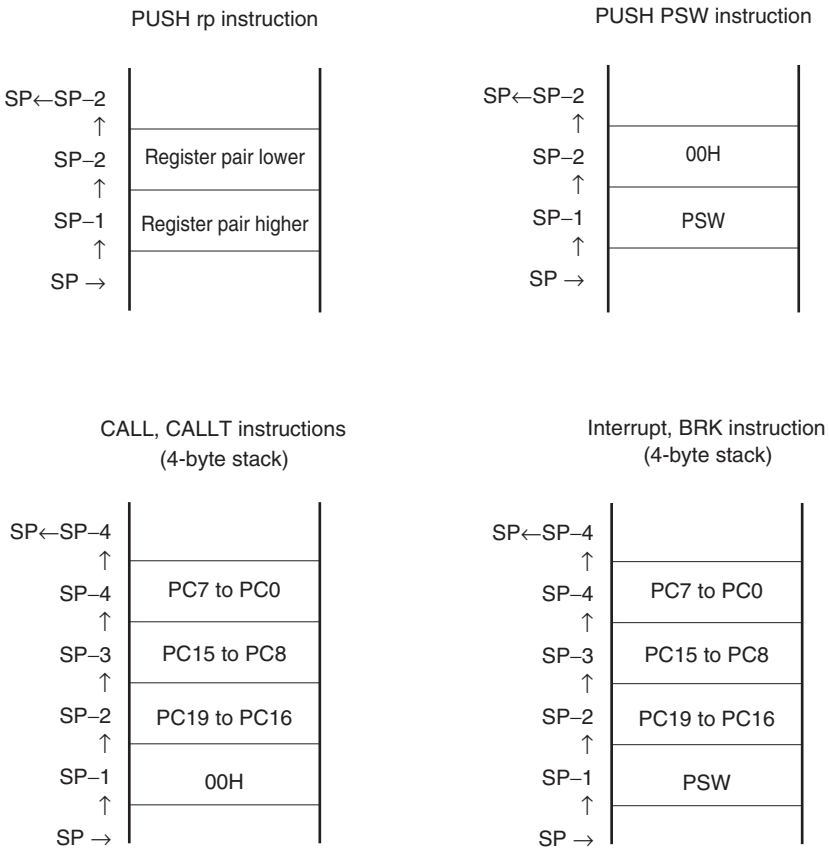
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CANbus, CSI, I²C, LINbus, SPI, UART/USART |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 130 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 31x10b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f113tjlfb-x0 |

Correspondence between the address values and block numbers in the flash memory are shown below.

**Table 3-1. Correspondence between Address Values and Block Numbers in Flash Memory (1/4)**

| Address Value | Block Number | Address Value | Block Number | Address Value | Block Number | Address Value | Block Number |
|---|---|---|---|---|---|---|---|
| 00000H to 003FFH | 000H | 08000H to 083FFH | 020H | 10000H to 103FFH | 040H | 18000H to 183FFH | 060H |
| 00400H to 007FFH | 001H | 08400H to 087FFH | 021H | 10400H to 107FFH | 041H | 18400H to 187FFH | 061H |
| 00800H to 00BFFH | 002H | 08800H to 08BFFH | 022H | 10800H to 10BFFH | 042H | 18800H to 18BFFH | 062H |
| 00C00H to 00FFFH | 003H | 08C00H to 08FFFH | 023H | 10C00H to 10FFFH | 043H | 18C00H to 18FFFH | 063H |
| 01000H to 013FFH | 004H | 09000H to 093FFH | 024H | 11000H to 113FFH | 044H | 19000H to 193FFH | 064H |
| 01400H to 017FFH | 005H | 09400H to 097FFH | 025H | 11400H to 117FFH | 045H | 19400H to 197FFH | 065H |
| 01800H to 01BFFH | 006H | 09800H to 09BFFH | 026H | 11800H to 11BFFH | 046H | 19800H to 19BFFH | 066H |
| 01C00H to 01FFFH | 007H | 09C00H to 09FFFH | 027H | 11C00H to 11FFFH | 047H | 19C00H to 19FFFH | 067H |
| 02000H to 023FFH | 008H | 0A000H to 0A3FFH | 028H | 12000H to 123FFH | 048H | 1A000H to 1A3FFH | 068H |
| 02400H to 027FFH | 009H | 0A400H to 0A7FFH | 029H | 12400H to 127FFH | 049H | 1A400H to 1A7FFH | 069H |
| 02800H to 02BFFH | 00AH | 0A800H to 0ABFFH | 02AH | 12800H to 12BFFH | 04AH | 1A800H to 1ABFFH | 06AH |
| 02C00H to 02FFFH | 00BH | 0AC00H to 0AFFFH | 02BH | 12C00H to 12FFFH | 04BH | 1AC00H to 1AFFFH | 06BH |
| 03000H to 033FFH | 00CH | 0B000H to 0B3FFH | 02CH | 13000H to 133FFH | 04CH | 1B000H to 1B3FFH | 06CH |
| 03400H to 037FFH | 00DH | 0B400H to 0B7FFH | 02DH | 13400H to 137FFH | 04DH | 1B400H to 1B7FFH | 06DH |
| 03800H to 03BFFH | 00EH | 0B800H to 0BBFFH | 02EH | 13800H to 13BFFH | 04EH | 1B800H to 1BBFFH | 06EH |
| 03C00H to 03FFFH | 00FH | 0BC00H to 0BFFFH | 02FH | 13C00H to 13FFFH | 04FH | 1BC00H to 1BFFFH | 06FH |
| 04000H to 043FFH | 010H | 0C000H to 0C3FFH | 030H | 14000H to 143FFH | 050H | 1C000H to 1C3FFH | 070H |
| 04400H to 047FFH | 011H | 0C400H to 0C7FFH | 031H | 14400H to 147FFH | 051H | 1C400H to 1C7FFH | 071H |
| 04800H to 04BFFH | 012H | 0C800H to 0CBFFH | 032H | 14800H to 14BFFH | 052H | 1C800H to 1CBFFH | 072H |
| 04C00H to 04FFFH | 013H | 0CC00H to 0CFFFH | 033H | 14C00H to 14FFFH | 053H | 1CC00H to 1CFFFH | 073H |
| 05000H to 053FFH | 014H | 0D000H to 0D3FFH | 034H | 15000H to 153FFH | 054H | 1D000H to 1D3FFH | 074H |
| 05400H to 057FFH | 015H | 0D400H to 0D7FFH | 035H | 15400H to 157FFH | 055H | 1D400H to 1D7FFH | 075H |
| 05800H to 05BFFH | 016H | 0D800H to 0DBFFH | 036H | 15800H to 15BFFH | 056H | 1D800H to 1DBFFH | 076H |
| 05C00H to 05FFFH | 017H | 0DC00H to 0DFFFH | 037H | 15C00H to 15FFFH | 057H | 1DC00H to 1DFFFH | 077H |
| 06000H to 063FFH | 018H | 0E000H to 0E3FFH | 038H | 16000H to 163FFH | 058H | 1E000H to 1E3FFH | 078H |
| 06400H to 067FFH | 019H | 0E400H to 0E7FFH | 039H | 16400H to 167FFH | 059H | 1E400H to 1E7FFH | 079H |
| 06800H to 06BFFH | 01AH | 0E800H to 0EBFFH | 03AH | 16800H to 16BFFH | 05AH | 1E800H to 1EBFFH | 07AH |
| 06C00H to 06FFFH | 01BH | 0EC00H to 0EFFFH | 03BH | 16C00H to 16FFFH | 05BH | 1EC00H to 1EFFFH | 07BH |
| 07000H to 073FFH | 01CH | 0F000H to 0F3FFH | 03CH | 17000H to 173FFH | 05CH | 1F000H to 1F3FFH | 07CH |
| 07400H to 077FFH | 01DH | 0F400H to 0F7FFH | 03DH | 17400H to 177FFH | 05DH | 1F400H to 1F7FFH | 07DH |
| 07800H to 07BFFH | 01EH | 0F800H to 0FBFFH | 03EH | 17800H to 17BFFH | 05EH | 1F800H to 1FBFFH | 07EH |
| 07C00H to 07FFFH | 01FH | 0FC00H to 0FFFFH | 03FH | 17C00H to 17FFFH | 05FH | 1FC00H to 1FFFFH | 07FH |

**Figure 3-15. Data to Be Saved to Stack Memory**



### 4.2.5 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P47 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 4 (PU4).

For the P43 pin input, the threshold of the input buffer can be specified in 1-bit units using the port input threshold control register 4 (PITHL4).

This port can also be used for external interrupt request input, timer I/O, comparator output, SNOOZE status output, LIN serial data I/O, and data I/O for a flash memory programmer/debugger.

Reset signal generation sets this port to input mode.

**Table 4-9. Settings of Registers When Using Port 4**

| Pin name | | PM4x | PITHL4x | Alternate Function Setting Note 6 | Remark |
|---|---|---|---|---|---|
| Name | I/O | | | | |
| P40 | Input | 1 | – | × | |
| | Output | 0 | – | × | |
| P41 | Input | 1 | – | × | |
| | Output | 0 | – | TRJIO0 output = 0 Note 1<br>TO10 output = 0 Note 2<br>VCOUT0 output = 0 Note 3<br>SNZOUT2 output = 0 Note 4 | |
| P42 | Input | 1 | – | × | |
| | Output | 0 | – | (LTXD0 output = 1) Note 5 | |
| P43 | Input | 1 | 0 | × | CMOS input (Schmitt1 input) |
| | | | 1 | × | CMOS input (Schmitt3 input) |
| | Output | 0 | × | × | |
| P44 | Input | 1 | – | × | |
| | Output | 0 | – | (TO07 output = 0) Note 2 | |
| P45 | Input | 1 | – | × | |
| | Output | 0 | – | (TO10 output = 0) Note 2 | |
| P46 | Input | 1 | – | × | |
| | Output | 0 | – | (TO12 output = 0) Note 2 | |
| P47 | Input | 1 | – | × | |
| | Output | 0 | – | × | |

**Notes 1.** When a pin sharing a timer input/output function of the timer RJ is to be used as a general-purpose port pin, the TMOD2 to TMOD0 bits of the timer RJ mode register 0 (TRJMR0) must have the same setting as their initial value or have a setting other than 001B.

**2.** When a pin sharing a timer output function of the timer array unit is to be used as a general-purpose port pin, the TOmn bit of the timer output register m (TOm) and the TOEmn bit of the timer output enable register m (TOEm) corresponding to the target unit and channel must have the same setting as in the initial state (m = 0, 1, 2, n = 0 to 7).

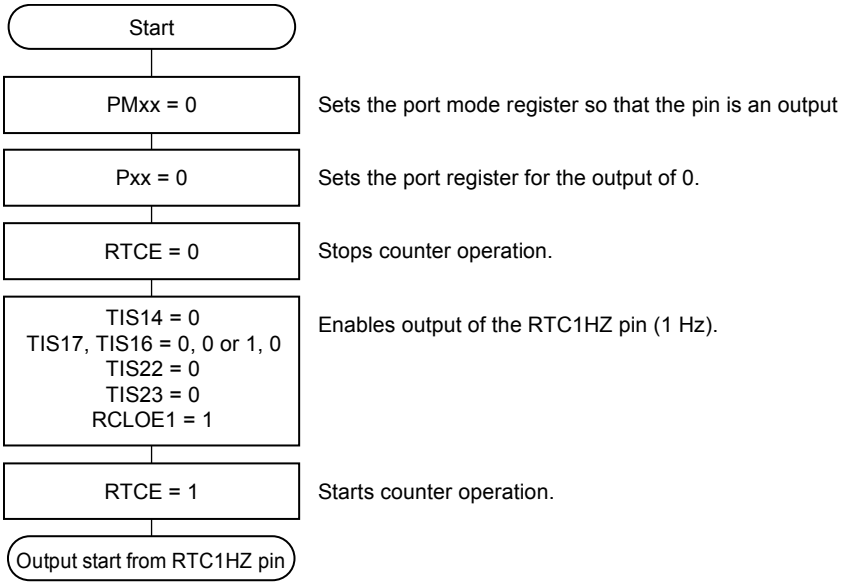
**3.** When a pin sharing the comparator output function is to be used as a general-purpose port pin, the COE bit of the comparator control register (CMPCTL) must have the same setting as its initial value.

**4.** When a pin sharing the SNOOZE status output function is to be used as a general-purpose port pin, the OUTEN0 to OUTEN7 bits of the SNOOZE status output control registers 0, 1, 2, 3 (PSNZCNT0, 1, 2, 3) must have the same setting as its initial value.

**5.** When a pin sharing the serial data output function of the LIN is to be used as a general-purpose port pin, operation of the corresponding LIN must be stopped.

### 9.4.5 1 Hz output of real-time clock

**Figure 9-26. 1 Hz Output Setting Procedure**




**Caution First set the RTCEN bit to 1 while oscillation of the input clock ($f_{RTC}$) is stable.**

### 12.3.13 Port mode registers 3, 7 to 10, and 12 (PM3, PM7 to PM10, PM12)

When using the ANI0/P33 to ANI23/P105 and ANI24/P125 to ANI30/P74 pins for an analog input port, set the PMmn bit to 1. The output latches of PMmn at this time may be 0 or 1.

If the PMmn bits are set to 0, they cannot be used as analog input port pins.

The PMm registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

**Cautions 1. Available pins differ depending on the products. For details, see CHAPTER 2 PIN FUNCTIONS.**

**2. If a pin is set as an analog input port, not the pin level but 0 is always read.**

**Remark** m = 3, 7 to 10, 12; n = 0 to 7

**Figure 12-17. Formats of Port Mode Registers 3, 7 to 10, and 12 (PM3, PM7 to PM10, PM12) (144-pin Products)**

Address: FFF23H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM3 | 1 | 1 | 1 | PM34 | PM33 | 1 | 1 | 1 |

Address: FFF27H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM7 | 1 | 1 | 1 | PM74 | PM73 | PM72 | PM71 | PM70 |

Address: FFF28H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM8 | PM87 | PM86 | PM85 | PM84 | PM83 | PM82 | PM81 | PM80 |

Address: FFF29H After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM9 | PM97 | PM96 | PM95 | PM94 | PM93 | PM92 | PM91 | PM90 |

Address: FFF2AH After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM10 | 1 | 1 | PM105 | PM104 | PM103 | PM102 | PM101 | PM100 |

Address: FFF2CH After reset: FFH R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PM12 | 1 | 1 | PM125 | 1 | 1 | 1 | 1 | PM120 |

| PM bit | I/O mode selection |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

**Caution When using $AV_{REFP}$ and $AV_{REFM}$, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.**

## 15.2 Configuration of Serial Array Unit

The serial array unit includes the following hardware.

**Table 15-1. Configuration of Serial Array Unit**

| Item | Configuration |
|---|---|
| Shift register | 16 bits or 9 bits Note 1 |
| Buffer register | 16 bits or the lower 9 bits of Serial data register mn (SDRmn)Note 1, 2 |
| Serial clock I/O | $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK11}$, $\overline{SCK20}$, $\overline{SCK21}$ pins (for 3-wire serial I/O), SCL00, SCL01, SCL10, SCL11 pins (for simplified $I^2C$) |
| Serial data input | SI00, SI01, SI10, SI11, SI20, SI21 pins (for 3-wire serial I/O), RXD0 pin (for UART supporting LIN-bus), RXD1, RXD2 pin (for UART) |
| Serial data output | SO00, SO01, SO10, SO11, SO20, SO21 pins (for 3-wire serial I/O), TXD0 pin (for UART supporting LIN-bus), TXD1, TXD2 pin (for UART), output controller |
| Serial data I/O | SDA00, SDA01, SDA10, SDA11 pins (for simplified $I^2C$) |
| Slave select input | $\overline{SSI00}$, $\overline{SSI01}$, $\overline{SSI10}$, $\overline{SSI11}$ pin (for 3-wire serial I/O) |
| Control registers | <Registers of unit setting block><br>• Peripheral enable register 0 (PER0)<br>• Peripheral enable register 1 (PER1)<br>• Serial clock select register m (SPSm)<br>• Serial channel enable status register m (SEm)<br>• Serial channel start register m (SSm)<br>• Serial channel stop register m (STm)<br>• Serial output enable register m (SOEm)<br>• Serial output register m (SOm)<br>• Serial output level register m (SOLm)<br>• Serial slave select enable register m (SSEm) Note 3<br>• Serial standby control register m (SSCm) Note 4<br>• Input switch control register (ISC)<br>• Noise filter enable register 0 (NFEN0) |
| | <Registers of each channel><br>• Serial data register mn (SDRmn)<br>• Serial mode register mn (SMRmn)<br>• Serial communication operation setting register mn (SCRmn)<br>• Serial status register mn (SSRmn)<br>• Serial flag clear trigger register mn (SIRmn) |
| | • Port input mode registers 1, 3, 5 to 7, 12 (PIM1, PIM3, PIM5 to PIM7, PIM12)<br>• Port output mode registers 1, 6, 7, 12 (POM1, POM6, POM7, POM12)<br>• Port mode registers 0 to 7, 15 (PM0 to PM7, PM15)<br>• Port registers 0 to 7, 15 (P0 to P7, P15) |

**Notes1.** The number of bits used as the shift register and buffer register differs depending on the unit and channel.

- mn = 00, 01, 10, 11: 16 bits
- mn = 20, 21: lower 9 bits

**2.** When SEmn is 1, the lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … $SDR_pL$ (CSIp data register)
- UARTq reception … $SDR_{mm}L$ (UARTq receive data register)
- UARTq transmission … SDRmnL (UARTq transmit data register)
- IICr communication … SDRrL (IICr data register)

**3.** m = 0, 1 , n = 0,1 only

**4.** m = 2 only

### 16.5.16 Communication operations

The following shows three operation procedures with the flowchart.

#### (1) Master operation in single master system

The flowchart when using the RL78/F15 as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

#### (2) Master operation in multimaster system

In the $I^2C$ bus multimaster system, whether the bus is released or used cannot be judged by the $I^2C$ bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the RL78/F15 takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the RL78/F15 loses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

#### (3) Slave operation

An example of when the RL78/F15 is used as the $I^2C$ bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA0 interrupt occurrence (communication waiting). When an INTIICA0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

The meanings of <3> to <10> in (2) Address ~ data ~ data in Figure 16-32 are explained below.

<3> In the slave device if the address received matches the address (SVA0 value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)[Note].

<5> The master device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL0 = 1), the master device starts transferring data to the slave device.

<7> After data transfer is completed, because of ACKE0 = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA0: end of transfer).

<9> The master device writes the data to transmit to the IICA0 register and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WREL0 = 1). The master device then starts transferring data to the slave device.

**Note** If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

**Remark** <1> to <15> in Figure 16-32 represent the entire procedure for communicating data using the $I^2C$ bus. Figure 16-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 16-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 16-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

### (7) LIN/UART Baud Rate Prescaler Register (LBRPn)

Address: F06C3H, F06C2H

| | LBRPn1 | | | | | | | | LBRPn0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Value after reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Function | Setting Range | R/W |
|---|---|---|---|
| 15 to 0 | Assuming that the value set in this register is L (0 to 65535), the baud rate prescaler divides the frequency of the prescaler clock by L + 1. | 0000H to FFFFH | R/W |

Set the LBRPn register when the OMM0 bit in the LMSTn register is 0 (LIN reset mode).

Assuming that the value set in this register is L, the baud rate prescaler divides the frequency of the clock that is selected by the LPRS bits (prescaler clock select bits) in the LWBRn register by L + 1.
The LBRPn register can be accessed in 8-bit units using the following registers.
- Lower 8 bits: LIN/UART baud rate prescaler 0 register (LBRPn0); address F06C2H
- Upper 8 bits: LIN/UART baud rate prescaler 1 register (LBRPn1); address F06C3H

**Remark** When a sync field reception succeeded in LIN slave mode [auto baud rate], baud rate correction result is set to LBRPn register automatically.

### 18.3.27 CAN Receive Buffer Register nAH (RMIDHn) (n = 0 to 31)

Address RMIDH0: F03A2H, RMIDH1: F03B2H, RMIDH2: F03C2H, RMIDH3: F03D2H
RMIDH4: F03E2H, RMIDH5: F03F2H, RMIDH6: F0402H, RMIDH7: F0412H
RMIDH8: F0422H, RMIDH9: F0432H, RMIDH10: F0442H, RMIDH11: F0452H
RMIDH12: F0462H, RMIDH13: F0472H, RMIDH14: F0482H, RMIDH15: F0492H
RMIDH16: F04A2H, RMIDH17: F04B2H, RMIDH18: F04C2H, RMIDH19: F04D2H
RMIDH20: F04E2H, RMIDH21: F04F2H, RMIDH22: F0502H, RMIDH23: F0512H
RMIDH24: F0522H, RMIDH25: F0532H, RMIDH26: F0542H, RMIDH27: F0552H
RMIDH28: F0562H, RMIDH29: F0572H, RMIDH30: F0582H, RMIDH31: F0592H

The RMIDHn register can be accessed in 16-bit units. In addition, the RMIDHn register can be accessed in 8-bit units as RMIDHnL, RMIDHnH register.

| | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RMIDE | RMRTR | — | RMID[28:16] | | | | | | | | | | | | |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| 15 | RMIDE | Receive Buffer IDE | 0: Standard ID<br>1: Extended ID | R |
| 14 | RMRTR | Receive Buffer RTR | 0: Data frame<br>1: Remote frame | R |
| 13 | — | Reserved | This bit is always read as 0. | R |
| 12 to 0 | RMID[28:16] | Receive Buffer ID Data H | The standard ID or extended ID of received message can be read.<br>For standard ID, these bits are read as 0. | R |

This register can be read when the RPAGE bit in the GRWCR register is 1.

- RMIDE Bit
  This bit indicates the ID format (standard ID or extended ID) of the message stored in the receive buffer.

- RMRTR Bit
  This bit indicates the frame format (data frame or remote frame) of the message stored in the receive buffer.

- RMID[28:16] Bits
  These bits indicate the ID of the message stored in the receive buffer.

### 18.3.28 CAN Receive Buffer Register nBL (RMTSn) (n = 0 to 31)

Address RMTS0L: F03A4H, RMTS1: F03B4H, RMTS2: F03C4H, RMTS3: F03D4H
RMTS4: F03E4H, RMTS5: F03F4H, RMTS6: F0404H, RMTS7: F0414H
RMTS8: F0424H, RMTS9: F0434H, RMTS10: F0444H, RMTS11: F0454H
RMTS12: F0464H, RMTS13: F0474H, RMTS14: F0484H, RMTS15: F0494H
RMTS16: F04A4H, RMTS17: F04B4H, RMTS18: F04C4H, RMTS19: F04D4H
RMTS20: F04E4H, RMTS21: F04F4H, RMTS22: F0504H, RMTS23: F0514H
RMTS24: F0524H, RMTS25: F0534H, RMTS26: F0544H, RMTS27: F0554H
RMTS28: F0564H, RMTS29: F0574H, RMTS30: F0584H, RMTS31: F0594H

The RMTSn register can be accessed in 16-bit units. In addition, the RMTSn register can be accessed in 8-bit units as RMTSnL, RMTSnH register.

| | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RMTS[15:0] | | | | | | | | | | | | | | | |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| 15 to 0 | RMTS[15:0] | Receive Buffer Timestamp Data | Timestamp value of the received message can be read. | R |

This register can be read when the RPAGE bit in the GRWCR register is 1.

- RMTS[15:0] Bits
  These bits indicate the timestamp value of the message stored in the receive buffer.

### 18.3.43 CAN Receive FIFO Access Register mDL (RFDF2m) (m = 0 to 3)

Address RFDF20: F05ACH, RFDF21: F05BCH, RFDF22: F05CCH, RFDF23: F05DCH

The RFDF2m register can be accessed in 16-bit units. In addition, the RFDF2m register can be accessed in 8-bit units as RFDF2mL, RFDF2mH register.

| | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RFDB5[7:0] | | | | | | | | RFDB4[7:0] | | | | | | | |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| 15 to 8 | RFDB5[7:0] | Receive FIFO Buffer Data Byte 5 | Data in the message stored in the receive FIFO buffer can be read. | R |
| 7 to 0 | RFDB4[7:0] | Receive FIFO Buffer Data Byte 4 | | R |

When the RFDLC[3:0] value in the RFPTRm register is smaller than B'1000, data bytes for which no data is set are read as H'00.

This register can be read when the RPAGE bit in the GRWCR register is 1.

### 18.3.56 CANi Transmit/Receive FIFO Access Register kDH (CFDF3k) (i = 0, 1, k = 0, 1)

Address CFDF30: F05EEH, CFDF31: F05FEH

The CFDF3k register can be accessed in 16-bit units. In addition, the CFDF3k register can be accessed in 8-bit units as CFDF3kL, CFDF3kH register.

| | b15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CFDB7[7:0] | | | | | | | | CFDB6[7:0] | | | | | | | |
| After Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Symbol | Bit Name | Description | R/W |
|---|---|---|---|---|
| 15 to 8 | CFDB7[7:0] | Transmit/Receive FIFO Buffer Data Byte 7 | When CFM[1:0] value is B'01 (transmit mode): Set the transmit/receive FIFO buffer data. When CFM[1:0] value is B'00 (receive mode): The message data stored in the transmit/receive FIFO buffer can be read. | R/W |
| 7 to 0 | CFDB6[7:0] | Transmit/Receive FIFO Buffer Data Byte 6 | | R/W |

This register is readable when the CFM[1:0] value in the CFCCHk register is B'00 (receive mode). This register should not be read or written when the CFM[1:0] value is B'10 (gatewaymode).

This register can be read/written when the RPAGE bit in the GRWCR register is 1.

## 18.5 Reception Function

There are two reception types.

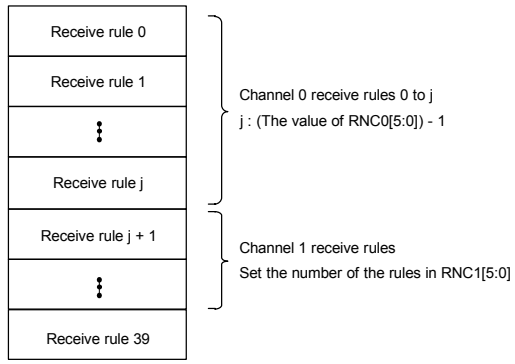
- Reception by receive buffers:
  Zero to 32 receive buffers can be shared by all channels. Since messages stored in receive buffers are overwritten at each reception, the latest receive data can always be read.
- Reception by receive FIFO buffers and transmit/receive FIFO buffers (receive mode):
  Four receive FIFO buffers can be shared by all channels and one dedicated transmit/receive FIFO buffer is provided for each channel. The FIFO buffers can hold the number of received messages set by the RFDC[2:0] bits in the RFCCm register and CFDC[2:0] bits in the CFCCLk register, and massages can be read sequentially from the oldest.

### 18.5.1 Data Processing Using the Receive Rule Table

Data processing using the receive rule table allows selected messages to be stored in the specified buffer. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function processing.

Receive rule is 40 for the entire module, it can be up to 40 registered in one channel. If receive rules are not set, no message can be received. Figure 18-4 illustrates how receive rules are registered.

**Figure 18-4. Entry of Receive Rules**




Remark RNC0[5:0], RNC1[5:0]: Bits in the GAFLCFG register

Each receive rule consists of 12 bytes in the GAFLIDLj, GAFLIDHj, GAFLMLj, GAFLMHj, GAFLPLj, and GAFLPHj registers (j = 0 to 39). The GAFLIDLj and GAFLIDHj registers (j = 0 to 39) are used to set ID, IDE bit, RTR bit, and the mirror function, the GAFLMLj and GAFLMHj registers are used to set mask, the GAFLPLj and GAFLPHj registers are used to set label information to be added, DLC value, and storage receive buffer, and storage FIFO buffer.

#### (1) Acceptance Filter Processing

In the acceptance filter processing, the ID data, IDE bit, and RTR bit in a received message are compared with the ID data, IDE bit, and RTR bit set in the receive rule of the corresponding channel. When all these bits match, the message passes through the acceptance filter processing. The ID data, IDE bit, and RTR bit in a received message which correspond to bits that are set to 0 (bits are not compared) in the GAFLMLj and GAFLMHj registers are not compared and are regarded as matched.

Check begins with the receive rule with the smallest rule number of the corresponding channel. When all the bits to be compared in a received message match the bits set in the receive rule or when all the receive rules are compared without any match, filter processing stops. If there is no matching receive rule, the received message is not stored in the receive buffer or FIFO buffer.

| ECCRV0 | ECC code inversion bit 0 |
|---|---|
| 0 | Bit 0 of ECC code not inverted. |
| 1 | Bit 0 of ECC code inverted. |

| DWRV7 | Write data inversion bit 7 |
|---|---|
| 0 | Bit 7 of write data not inverted. |
| 1 | Bit 7 of write data inverted. |

| DWRV6 | Write data inversion bit 6 |
|---|---|
| 0 | Bit 6 of write data not inverted. |
| 1 | Bit 6 of write data inverted. |

| DWRV5 | Write data inversion bit 5 |
|---|---|
| 0 | Bit 5 of write data not inverted. |
| 1 | Bit 5 of write data inverted. |

| DWRV4 | Write data inversion bit 4 |
|---|---|
| 0 | Bit 4 of write data not inverted. |
| 1 | Bit 4 of write data inverted. |

| DWRV3 | Write data inversion bit 3 |
|---|---|
| 0 | Bit 3 of write data not inverted. |
| 1 | Bit 3 of write data inverted. |

| DWRV2 | Write data inversion bit 2 |
|---|---|
| 0 | Bit 2 of write data not inverted. |
| 1 | Bit 2 of write data inverted. |

| DWRV1 | Write data inversion bit 1 |
|---|---|
| 0 | Bit 1 of write data not inverted. |
| 1 | Bit 1 of write data inverted. |

| DWRV0 | Write data inversion bit 0 |
|---|---|
| 0 | Bit 0 of write data not inverted. |
| 1 | Bit 0 of write data inverted. |

**Cautions 1. Access the ECCDWRVR register in word units.**

**2. Bits 13 to 15 of the ECCDWRVR register are always read as 0. The write value should always be 0.**

**3. All data written to the RAM, including data written to the stack, is inverted. Therefore, all peripheral functions that might rewrite the RAM must be stopped before a write data inversion bit is set. Do not set a write data inversion bit during OCD.**

The dedicated flash memory programmer generates the following signals for the RL78/F15. See the manual of PG-FP5, FL-PR5, or E1 on-chip debugging emulator for details.

**Table 31-2. Pin Connection**

| Dedicated Flash Memory Programmer | | | | RL78/F15 |
|---|---|---|---|---|
| Signal Name | | I/O | Pin Function | Pin Name |
| PG-FP5, FL-PR5 | E1 on-chip debugging emulator | | | |
| $V_{DD}$ | | I/O | $V_{DD}$ voltage generation/power monitoring | $V_{DD}$ |
| GND | | – | Ground | $V_{SS}$, $EV_{SS0}$ Note 1, $EV_{SS0}$ Note 2, REGC Note 3 |
| $EMV_{DD}$ | | – | Driving power for TOOL0 pin | $V_{DD}$, $EV_{DD0}$ Note 1, $EV_{DD1}$ Note 2 |
| /RESET | – | Output | Reset signal | $\overline{RESET}$ |
| – | $\overline{RESET}$ | Output | | |
| – | TOOL0 | I/O | Transmit/receive signal | TOOL0 |
| SI/RXD | – | I/O | Transmit/receive signal | |

**Notes 1.** 64, 80, 100, 144-pin products only.

**2.** 100, 144-pin products only.

**3.** Connect REGC pin to ground via a capacitor (0.47 to 1 $\mu$F).

**Caution The connection destination pins differ depending on the product. For details, see Table 31-1.**

### 34.1.2 Description of operation column

The operation when the instruction is executed is shown in the “Operation” column using the following symbols.

**Table 34-2. Symbols in “Operation” Column**

| Symbol | Function |
|---|---|
| A | A register; 8-bit accumulator |
| X | X register |
| B | B register |
| C | C register |
| D | D register |
| E | E register |
| H | H register |
| L | L register |
| ES | ES register |
| CS | CS register |
| AX | AX register pair; 16-bit accumulator |
| BC | BC register pair |
| DE | DE register pair |
| HL | HL register pair |
| PC | Program counter |
| SP | Stack pointer |
| PSW | Program status word |
| CY | Carry flag |
| AC | Auxiliary carry flag |
| Z | Zero flag |
| RBS | Register bank select flag |
| IE | Interrupt request enable flag |
| () | Memory contents indicated by address or register contents in parentheses |
| $X_H$, $X_L$<br>$X_S$, $X_H$, $X_L$ | 16-bit registers: $X_H$ = higher 8 bits, $X_L$ = lower 8 bits<br>20-bit registers: $X_S$ = (bits 19 to 16), $X_H$ = (bits 15 to 8), $X_L$ = (bits 7 to 0) |
| ∧ | Logical product (AND) |
| ∨ | Logical sum (OR) |
| ∀ | Exclusive logical sum (exclusive OR) |
| ¯ | Inverted data |
| addr5 | 16-bit immediate data (even addresses only in 0080H to 00BFH) |
| addr16 | 16-bit immediate data |
| addr20 | 20-bit immediate data |
| jdisp8 | Signed 8-bit data (displacement value) |
| jdisp16 | Signed 16-bit data (displacement value) |

## 35.3 DC Characteristics

### 35.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **CHAPTER 4 PORT FUNCTIONS**.

**($T_A$ = -40 to +105°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/4)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high[Note 1] | $I_{OH1}$ | Per pin for P00 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P110 to P117, P120, P125 to P127, P130 to P136, P140 to P147, P150 to 157, P160 to P167 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -5.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -3.0 | mA |
| | | Per pin for P10, P12, P14, P30,P120,P140 (special slew rate) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -0.6 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -0.2 | mA |
| | | Total of P01, P02, P40 to P47, P110 to P117, P120, P125 to P127, P131 to P136, P150 to P153, P160 to P167 (for duty factors ≤ 70%[Note 2]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -20.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -10.0 | mA |
| | | Total of P00, P03 to P07, P10 to P17, P20 to P27, P30 to P32, P35 to P37, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140 to P147, P154 to P157 (for duty factors ≤ 70%[Note 2]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -19.0 | mA |
| | | Total of all pins (for duty factors ≤ 70%[Note 2]) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -50.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -29.0 | mA |
| | $I_{OH2}$ | Per pin for P33, P34, P80 to P87, P90 to P97, P100 to P105 | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | -0.1 | mA |
| | | Total of all pins (for duty factors ≤ 70%[Note 2]) | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | -2.0 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from pins $EV_{DD0}$, $EV_{DD1}$, and $V_{DD}$ to an output pin.

**2.** These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins ($I_{OH} \times 0.7$)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 35.4 AC Characteristics

### 35.4.1 Basic Operation

**($T_A$ = -40 to +105°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ = $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | High-speed on-chip oscillator clock operation | | 0.03125 | | 1 | µs |
| | | High-speed system clock operation | | 0.05 | | 1 | µs |
| | | PLL clock operation | | 0.03125 | | 1 | µs |
| | | Subsystem clock operation | | 28.5 | 30.5 | 34.5 | µs |
| | | Low-speed on-chip oscillator clock operation | | | 66.6 | | µs |
| | | In self programming mode | | 0.03125 | | 1 | µs |
| CPU/peripheral hardware clock frequency | $f_{CLK}$ | | | 0.03125 | | 66.6 | µs |
| External system clock frequency | $f_{EX}$ | | | 1.0 | | 20.0 | MHz |
| | $f_{EXS}$ | | | 29 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | | | 24 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | 13.7 | | | µs |
| TI00 to TI07, TI10 to TI17, TI20 to TI27 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | 1/$f_{MCK}$+10 | | | ns |
| TO00 to TO07, TO10 to TO17, TO20 to TO27 output frequency | $f_{TO}$ | All TO pins, Normal slew rate, C = 30 pF | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | TO01, TO06, TO07, TO11, TO13 only, Special slew rate, C = 30 pF | | | | 2 | MHz |
| PCLBUZ0 output frequency | $f_{PCL}$ | Normal slew rate C = 30 pF | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | Special slew rate C = 30 pF | | | | 2 | MHz |
| Timer RJ input cycle | $t_C$ | TRJIO0 | | 100 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{WH}$, $t_{WL}$ | TRJIO0 | | 40 | | | ns |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 to INTP15 Note | | 1 | | | µs |
| KR0 to KR7 key interrupt tinput low-level width | $t_{KR}$ | | | 250 | | | ns |
| $\overline{RESET}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

**Note** Pins $\overline{RESET}$, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

**Caution Excluding the error in oscillation frequency accuracy**.

**Remark** $f_{MCK}$: Timer array unit operation clock frequency

### 36.6.5 POR Circuit Characteristics

**($T_A$ = -40 to +125°C, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage[Note] | $V_{POR}$ | Power supply rise time | 1.48 | 1.56 | 1.62 | V |
| | $V_{PDR}$ | Power supply fall time | 1.47 | 1.55 | 1.61 | V |
| Minimum pulse width | $T_{PW}$ | | 300 | | | μs |
| Detection delay time | $T_{PD}$ | | | | 350 | μs |

**Note** This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).