Renesas Electronics America Inc - R5F113TJLFB#X5 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, CSI, I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	130
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 31x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f113tjlfb-x5

Other Documents

Document Name	Document No.
Renesas MPUs & MCUs RL78 Family	R01CP0003E
Semiconductor Package Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Semiconductor Reliability Handbook	R51ZZ0001E

Note See the “Semiconductor Package Mount Manual” website (http://www.renesas.com/products/package/index.jsp).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

Table 3-6. Extended SFR (2nd SFR) List (16/52)

Address	Special Function Register (2nd SFR) Name	Symbol		R/W	Manipulable Bit Range			After reset
					1-bit	8-bit	16-bit	
F037CH	CAN0 transmit history buffer control register	THLCC0L	THLCC0	R/W	–	√	√	0000H
F037DH		THLCC0H			–	√		
F037EH	CAN1 transmit history buffer control register	THLCC1L	THLCC1	R/W	–	√	√	0000H
F037FH		THLCC1H			–	√		
F0380H	CAN0 transmit history buffer status register	THLSTS0L	THLSTS0	R/W	–	√	√	0001H Note 3
F0381H		THLSTS0H			–	√		
F0382H	CAN1 transmit history buffer status register	THLSTS1L	THLSTS1	R/W	–	√	√	0001H Note 3
F0383H		THLSTS1H			–	√		
F0384H	CAN0 transmit history buffer pointer control register	THLPCTR0L	THLPCTR0	W	–	√	√	0000H
F0385H		THLPCTR0H			–	√		
F0386H	CAN1 transmit history buffer pointer control register	THLPCTR1L	THLPCTR1	W	–	√	√	0000H
F0387H		THLPCTR1H			–	√		
F0388H	CAN global transmit interrupt status register	GTINTSTSL	GTINTSTS	R	–	√	√	0000H
F0389H		GTINTSTSH			–	√		
F038AH	CAN global RAM window control register	GRWCRL	GRWCR	R/W	–	√	√	0000H
F038BH		GRWCRH			–	√		
F038CH	CAN global test configuration register	GTSTCFGL	GTSTCFG	R/W	–	√	√	0000H
F038DH		GTSTCFGH			–	√		
F038EH	CAN global test control register	GTSTCTRL	GTSTCTR	R/W	–	√	–	00H
F0394H	CAN global test protection unlock register	GLOCKK		W	–	–	√	0000H
F0395H					–	–		
F03A0H	CAN receive rule entry register 0AL Note 1	GAFLIDL0L	GAFLIDL0	R/W	–	√	√	0000H
F03A1H		GAFLIDL0H			–	√		
F03A0H	CAN receive buffer register 0AL Note 2	RMIDL0L	RMIDL0	R	–	√	√	0000H
F03A1H		RMIDL0H			–	√		
F03A2H	CAN receive rule entry register 0AH Note 1	GAFLIDH0L	GAFLIDH0	R/W	–	√	√	0000H
F03A3H		GAFLIDH0H			–	√		
F03A2H	CAN receive buffer register 0AH Note 2	RMIDH0L	RMIDH0	R	–	√	√	0000H
F03A3H		RMIDH0H			–	√		
F03A4H	CAN receive rule entry register 0BL Note 1	GAFLML0L	GAFLML0	R/W	–	√	√	0000H
F03A5H		GAFLML0H			–	√		
F03A4H	CAN receive buffer register 0BL Note 2	RMTS0L	RMTS0	R	–	√	√	0000H
F03A5H		RMTS0H			–	√		
F03A6H	CAN receive rule entry register 0BH Note 1	GAFLMH0L	GAFLMH0	R/W	–	√	√	0000H
F03A7H		GAFLMH0H			–	√		
F03A6H	CAN receive buffer register 0BH Note 2	RMPTR0L	RMPTR0	R	–	√	√	0000H
F03A7H		RMPTR0H			–	√		
F03A8H	CAN receive rule entry register 0CL Note 1	GAFLPL0L	GAFLPL0	R/W	–	√	√	0000H
F03A9H		GAFLPL0H			–	√		

Notes 1. These registers are allocated to the RAM window 0 for the CAN module (receive rule and CAN RAM test register). When setting these registers, set the RPAGE bit in the GRWCR register to 0.

2. These registers are allocated to the RAM window 1 for the CAN module (receive buffer, receive FIFO buffer, transmit/receive FIFO buffer, transmit buffer, and transmit history data). When setting these registers, set the RPAGE bit in the GRWCR register to 1.

3. When the CAN0EN bit in the PER2 register is 0, the read value is undefined.
When the CAN0EN bit in the PER2 register is 1, the read value is the initial value listed above.

Table 3-6. Extended SFR (2nd SFR) List (48/52)

Address	Special Function Register (2nd SFR) Name	Symbol		R/W	Manipulable Bit Range			After reset
					1-bit	8-bit	16-bit	
F0656H	CAN1 transmit buffer register 5BH Note 2	TMPTR5L	TMPTR5	R/W	–	√	√	0000H
F0657H		TMPTR5H			–	√		
F0658H	CAN RAM test register 108 Note 1	RPGACC108L	RPGACC108	R/W	–	√	√	0000H
F0659H		RPGACC108H			–	√		
F0658H	CAN1 transmit buffer register 5CL Note 2	TMDF05L	TMDF05	R/W	–	√	√	0000H
F0659H		TMDF05H			–	√		
F065AH	CAN RAM test register 109 Note 1	RPGACC109L	RPGACC109	R/W	–	√	√	0000H
F065BH		RPGACC109H			–	√		
F065AH	CAN1 transmit buffer register 5CH Note 2	TMDF15L	TMDF15	R/W	–	√	√	0000H
F065BH		TMDF15H			–	√		
F065CH	CAN RAM test register 110 Note 1	RPGACC110L	RPGACC110	R/W	–	√	√	0000H
F065DH		RPGACC110H			–	√		
F065CH	CAN1 transmit buffer register 5DL Note 2	TMDF25L	TMDF25	R/W	–	√	√	0000H
F065DH		TMDF25H			–	√		
F065EH	CAN RAM test register 111 Note 1	RPGACC111L	RPGACC111	R/W	–	√	√	0000H
F065FH		RPGACC111H			–	√		
F065EH	CAN1 transmit buffer register 5DH Note 2	TMDF35L	TMDF35	R/W	–	√	√	0000H
F065FH		TMDF35H			–	√		
F0660H	CAN RAM test register 112 Note 1	RPGACC112L	RPGACC112	R/W	–	√	√	0000H
F0661H		RPGACC112H			–	√		
F0660H	CAN1 transmit buffer register 6AL Note 2	TMIDL6L	TMIDL6	R/W	–	√	√	0000H
F0661H		TMIDL6H			–	√		
F0662H	CAN RAM test register 113 Note 1	RPGACC113L	RPGACC113	R/W	–	√	√	0000H
F0663H		RPGACC113H			–	√		
F0662H	CAN1 transmit buffer register 6AH Note 2	TMIDH6L	TMIDH6	R/W	–	√	√	0000H
F0663H		TMIDH6H			–	√		
F0664H	CAN RAM test register 114 Note 1	RPGACC114L	RPGACC114	R/W	–	√	√	0000H
F0665H		RPGACC114H			–	√		
F0666H	CAN RAM test register 115 Note 1	RPGACC115L	RPGACC115	R/W	–	√	√	0000H
F0667H		RPGACC115H			–	√		
F0666H	CAN1 transmit buffer register 6BH Note 2	TMPTR6L	TMPTR6	R/W	–	√	√	0000H
F0667H		TMPTR6H			–	√		
F0668H	CAN RAM test register 116 Note 1	RPGACC116L	RPGACC116	R/W	–	√	√	0000H
F0669H		RPGACC116H			–	√		
F0668H	CAN1 transmit buffer register 6CL Note 2	TMDF06L	TMDF06	R/W	–	√	√	0000H
F0669H		TMDF06H			–	√		
F066AH	CAN RAM test register 117 Note 1	RPGACC117L	RPGACC117	R/W	–	√	√	0000H
F066BH		RPGACC117H			–	√		
F066AH	CAN1 transmit buffer register 6CH Note 2	TMDF16L	TMDF16	R/W	–	√	√	0000H
F066BH		TMDF16H			–	√		
F066CH	CAN RAM test register 118 Note 1	RPGACC118L	RPGACC118	R/W	–	√	√	0000H
F066DH		RPGACC118H			–	√		
F066CH	CAN1 transmit buffer register 6DL Note 2	TMDF26L	TMDF26	R/W	–	√	√	0000H
F066DH		TMDF26H			–	√		

Notes 1. These registers are allocated to the RAM window 0 for the CAN module (receive rule and CAN RAM test register). When setting these registers, set the RPAGE bit in the GRWCR register to 0.

2. These registers are allocated to the RAM window 1 for the CAN module (receive buffer, receive FIFO buffer, transmit/receive FIFO buffer, transmit buffer, and transmit history data). When setting these registers, set the RPAGE bit in the GRWCR register to 1.

4.2.14 Port 13

P131 to P136 are I/O ports with an output latch. Port 13 can be set to the input mode or output mode in 1-bit units using port mode register 13 (PM13). When the P131 to P136 pins are used as an input port, use of an onchip pull-up resistor can be specified by pull-up resistor option register 13 (PU13).

P130 is a 1-bit output-only port with an output latch.

P137 is a 1-bit input-only port.

P130 is fixed to output mode, and P137 is fixed to input mode.

This port can also be used for external interrupt request input and reset output.

The RESOUT output can be set by an option byte.

Table 4-25. Settings of Registers When Using Port 13

Pin Name		PM13X	Alternate Function Setting	Remark
Name	I/O			
P130	Output	–	RESOUT	
P131 to P136	Input	1	×	
	Output	0	×	
P137	Input	–	×	

Figure 8-26. Format of Timer RD Status Register i (TRDSRi) (i = 0 or 1)
[Functions Other Than Input Capture Function]

Address: F0273H (TRDSR0), F0283H (TRDSR1) After Reset: 00H Note 1

Symbol	7	6	5	4	3	2	1	0
TRDSRi	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA

Bits 7 to 6	Nothing is assigned	R/W
—	The write value must be 0. The read value is 0.	R

UDF	Underflow flag Note 2	R/W
In complementary PWM mode [Source for setting to 0] Write 0 after reading. Note 3 [Sources for setting to 1] When TRDi underflows. Enabled only in complementary PWM mode.		R/W

OVF	Overflow flag Note 4	R/W
[Source for setting to 0] Write 0 after reading. Note 3 [Source for setting to 1] When the TRDi register overflows		R/W

IMFD	Input capture/compare match flag D Note 6	R/W
[Source for setting to 0] Write 0 after reading. Note 3 [Source for setting to 1] When the values of TRDi and TRDGRDi match. Note 5		R/W

IMFC	Input capture/compare match flag C Note 6	R/W
[Source for setting to 0] Write 0 after reading. Note 3 [Source for setting to 1] When the values of TRDi and TRDGRCi match. Note 5		R/W

IMFB	Input capture/compare match flag B Note 6	R/W
[Source for setting to 0] Write 0 after reading. Note 3 [Source for setting to 1] When the values of TRDi and TRDGRBi match.		R/W

IMFA	Input capture/compare match flag A Note 6	R/W
[Source for setting to 0] Write 0 after reading. Note 3 [Source for setting to 1] When the values of TRDi and TRDGRAi match.		R/W

(Notes are listed on the next page.)

12.6.2 Software trigger mode (select mode, one-shot conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to perform the A/D conversion of the analog input specified by the analog input channel specification register (ADS).

<3> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated.

<4> After A/D conversion ends, the ADCS bit is automatically cleared to 0, and the system enters the A/D conversion standby status.

<5> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status.

<8> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCE = 0, specifying 1 for ADCS is ignored and A/D conversion does not start. In addition, A/D conversion does not start even if a hardware trigger is input while in the A/D conversion standby status.

Figure 12-21. Example of Software Trigger Mode (Select Mode, One-Shot Conversion Mode) Operation Timing

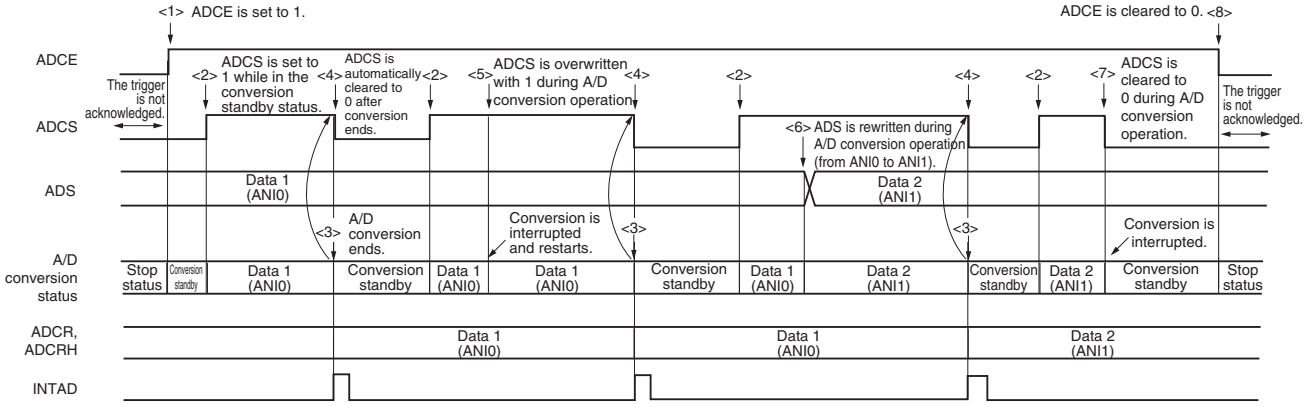
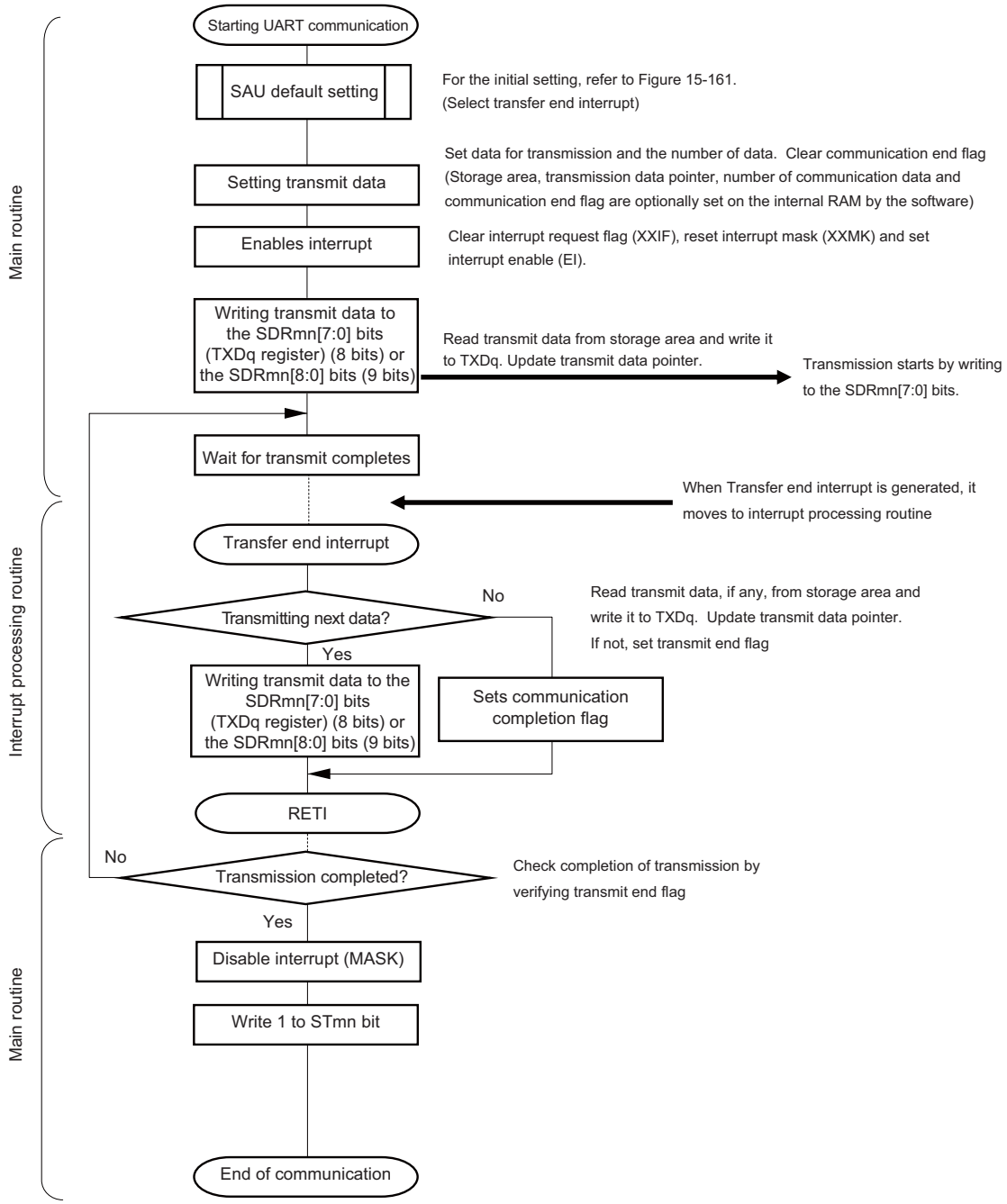


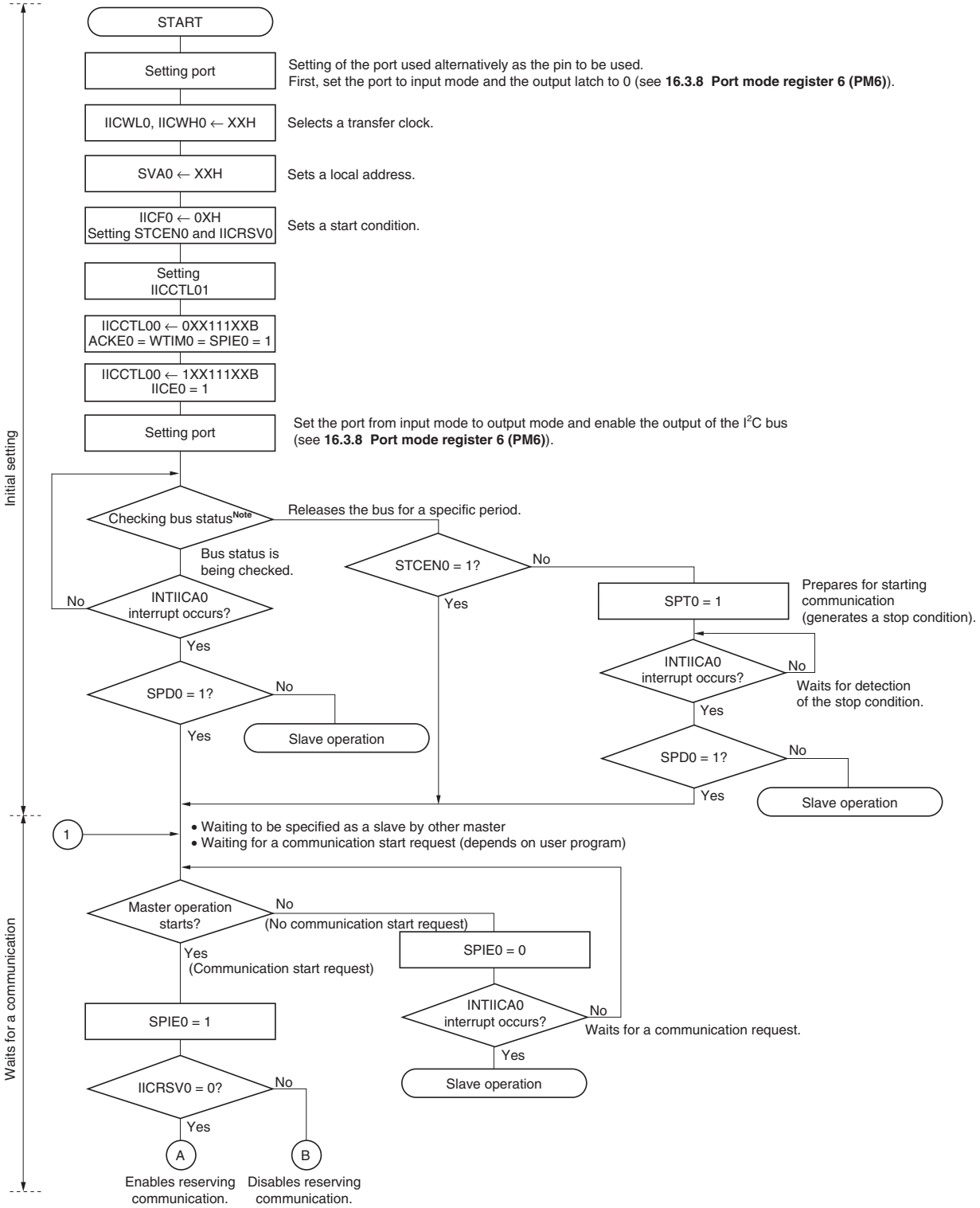
Figure 15-166. Flowchart of UART Transmission (in Single-Transmission Mode) (UART2)



Remark m: Unit number (m = 2), n: Channel number (n = 0), mn = 20, q: UART number (q = 2)

(2) Master operation in multi-master system

Figure 16-30. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDAA0 pin is constantly at low level, decide whether to release the I^2C bus (SCLA0 and SDAA0 pins = high level) in conformance with the specifications of the product that is communicating.

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in Figure 16-32 are explained below.

<1> The start condition trigger is set by the master device (STT0 = 1) and a start condition (i.e. SCLA0 = 1 changes SDAA0 from 1 to 0) is generated once the bus data line goes low (SDAA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS0 = 1). The master device is ready to communicate once the bus clock line goes low (SCLA0 = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register 0 (IICA0) and transmits the slave address.

<3> In the slave device if the address received matches the address (SVA0 value) of a slave device**Note**, that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)**Note**.

<5> The master device writes the data to transmit to the IICA0 register and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL0 = 1), the master device starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 16-32 represent the entire procedure for communicating data using the I^2C bus. Figure 16-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 16-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 16-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

The meanings of <3> to <12> in (2) Address ~ data ~ data in Figure 16-33 are explained below.

<3> In the slave device if the address received matches the address (SVA0 value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD0 = 1) at the rising edge of the 9th clock.

<4> The master device issues an interrupt (INTIICA0: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCLA0 = 0) and issues an interrupt (INTIICA0: address match)[Note].

<5> The master device changes the timing of the wait status to the 8th clock (WTIM0 = 0).

<6> The slave device writes the data to transmit to the IICA shift register 0 (IICA0) and releases the wait status that it set by the slave device.

<7> The master device releases the wait status (WREL0 = 1) and starts transferring data from the slave device to the master device.

<8> The master device sets a wait status (SCLA0 = 0) at the falling edge of the 8th clock, and issues an interrupt (INTIICA0: end of transfer). Because of ACKE0 = 1 in the master device, the master device then sends an ACK by hardware to the slave device.

<9> The master device reads the received data and releases the wait status (WREL0 = 1).

<10> The ACK is detected by the slave device (ACKD0 = 1) at the rising edge of the 9th clock.

<11> The slave device set a wait status (SCLA0 = 0) at the falling edge of the 9th clock, and the slave device issue an interrupt (INTIICA0: end of transfer).

<12> By the slave device writing the data to transmit to the IICA0 register, the wait status set by the slave device is released. The slave device then starts transferring data to the master device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDAA0 = 1). The slave device also does not issue the INTIICA0 interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA0 interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <19> in Figure 16-33 represent the entire procedure for communicating data using the I^2C bus. Figure 16-33 (1) Start condition ~ address ~ data shows the processing from <1> to <7>, Figure 16-33 (2) Address ~ data ~ data shows the processing from <3> to <12>, and Figure 16-33 (3) Data ~ data ~ stop condition shows the processing from <8> to <19>.

(23) UART Option Register 1 (LUORn1)

Address: F06E1H

	7	6	5	4	3	2	1	0
	—	—	—	UECD	UTIGTS	UEBDCE	UEBDL	UEBE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
0	UEBE	Expansion Bit Enable	0: Disables expansion bit operation. 1: Enables expansion bit operation.	R/W
1	UEBDL	Expansion Bit Detection Level Select	0: Selects expansion bit value 0 as the expansion bit detection level. 1: Selects expansion bit value 1 as the expansion bit detection level.	R/W
2	UEBDCE	Expansion Bit/Data Comparison Enable	0: Disables data comparison after detection of the expansion bit. 1: Enables data comparison after detection of the expansion bit.	R/W
3	UTIGTS	Transmission Interrupt Generation Timing Select	0: Transmission interrupt is generated at the start of transmission. 1: Transmission interrupt is generated at the completion of transmission.	R/W
4	UECD	Expansion Bit Comparison Disable	0: Enables comparison between the received expansion bit and the UEBDL bit value. 1: Disables comparison between the received expansion bit and the UEBDL bit value.	R/W
7 to 5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

UEBE bit (expansion bit enable bit)

The UEBE bit enables or disables expansion bit operation.
With 0 set, expansion bit operation is disabled.
With 1 set, expansion bit operation is enabled.
Set this bit when the OMM0 bit in the LMSTn register is 0 (LIN reset mode).
Do not set this bit to 1 when the UART buffer is in use.

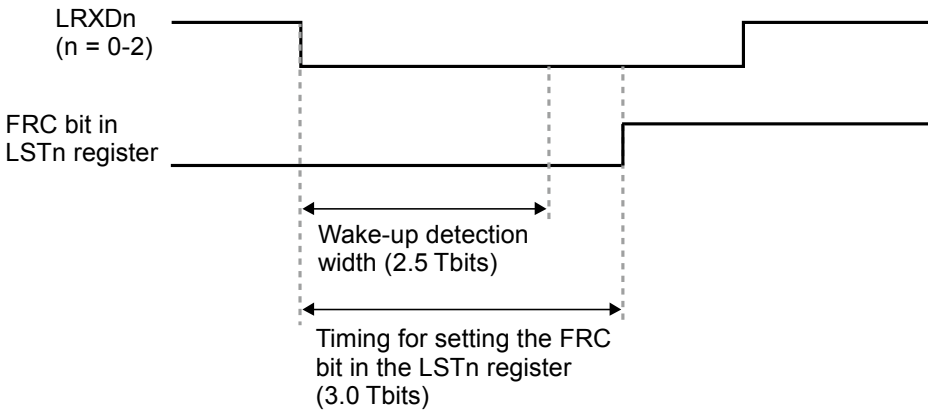
UEBDL bit (expansion bit detection level select bit)

The UEBDL bit sets the level to be detected as the expansion bit when the UEBE bit is 1 (expansion bit operation is enabled) and the UECD bit is 0 (comparison of the expansion bit is enabled).
With 0 set, expansion bit value 0 is the level to be detected as the expansion bit.
With 1 set, expansion bit value 1 is the level to be detected as the expansion bit.
Set this bit when the OMM0 bit in the LMSTn register is 0 (LIN reset mode).
Do not set this bit to 1 when the UART buffer is in use.

(2) Wake-up Reception

The detection of a wake-up signal involves the use of an input signal low width count function.
The input signal low width count function measures the low width of the input signal to the LRXDn pin, using the same sampling point as data reception. The function can measure the input signal low width of 2.5 Tbits of fLIN or greater.
In LIN master mode, appropriately setting the LWBR0 bit in the LWBRn register allows switching between LIN operation mode and LIN wake-up mode without changing any baud rate generator setting.
Set the LWBR0 bit in the LWBRn register to 0 when LIN Specification Package Revision 1.3 is used, and set it to 1 when LIN Specification Package Revision 2.x is used. When the LWBR0 bit is set to 1, fa is always selected as the LIN system clock (f_{LIN}) regardless of the setting of LCKS bits in the LMDn register (setting of LCKS bits not affected).
Setting the baud rate to 19200 bps with fa selected allows 130 μs or longer low level width of the input signal to be detected regardless of the setting of LCKS bits in the LMDn register.
When using this function, in LIN wake-up mode, set the RFT bit in the LDFCn register to 0 (LIN master mode: reception), or RCDS bit to 0 (LIN slave mode: reception), and the FTS bit in the LTRCn register to 1 (LIN master mode: frame transmission or wake-up transmission/reception started; LIN slave mode: header reception or wake-up transmission/reception started).
When the low width to be measured is reached, the FRC flag in the LSTn register turns 1 (successful response/wake-up reception). If the FRCIE bit in the LIEn register is 1 (successful response or wake-up reception interrupt enabled), an interrupt request is generated.

Figure 17-19. Input Signal Low Count Function



- BORF Flag
  This flag is set to 1 when 11 consecutive recessive bits have been detected 128 times and the CAN module returns from the bus off state. However, this flag is not set to 1 if the CAN module returns from the bus off state in either of the following ways before 11 consecutive recessive bits are detected 128 times.
  - The CHMDC[1:0] bits in the CiCTRL register are set to B'01 (channel reset mode).
  - The RTBO bit in the CiCTRL register is set to 1 (forcible return from the bus off state is made).
  - The BOM[1:0] bits in the CiCTRH register are set to B'01 (transition to channel halt mode at bus off entry).
  - The CHMDC[1:0] bits in the CiCTRL register are set to B'10 (channel halt mode) before 11 consecutive recessive bits are detected 128 times with the BOM[1:0] bits set to B'11 (transition to channel halt mode upon a request from the program during bus off).

- BOEF Flag
  This flag is set to 1 when the state becomes bus off state (TEC[7:0] value > 255). This flag is also set to 1 when the state becomes bus off state with the BOM[1:0] bits in the CiCTRH register set to B'01 (transition to channel halt mode at bus off entry).

- EPF Flag
  This flag becomes 1 when the CAN module becomes error passive state (REC[7:0] or TEC[7:0] value > 127). This flag becomes 1 only when the REC[7:0] or TEC[7:0] value exceeds 127 for the first time. Therefore, if the program writes 0 to this flag with the REC[7:0] or TEC[7:0] value remaining over 127, this bit is not set to 1 until both REC [7:0] and TEC[7:0] values become 127 or less and then the REC[7:0] or TEC[7:0] value exceeds 127 again.

- EWF Flag
  This flag is set to 1 only when the REC[7:0] or TEC[7:0] value exceeds 95 for the first time. Therefore, if the program writes 0 to this flag with the REC[7:0] or TEC[7:0] value remaining over 95, this bit is not set to 1 until both REC [7:0] and TEC[7:0] values become 95 or less and then the REC[7:0] or TEC[7:0] value exceeds 95 again.

- BEF Flag
  This flag is set to 1 when any one of the ADERR, B0ERR, B1ERR, CERR, AERR, FERR, and SERR flags in the CiERFLL register is set to 1.

18.3.37 CAN Receive FIFO Access Register mAL (RFIDLm) (m = 0 to 3)

Address RFIDL0: F05A0H, RFIDL1: F05B0H, RFIDL2: F05C0H, RFIDL3: F05D0H

The RFIDLm register can be accessed in 16-bit units. In addition, the RFIDLm register can be accessed in 8-bit units as RFIDLmL, RFIDLmH register.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFID[15:0]															
After Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
15 to 0	RFID[15:0]	Receive FIFO Buffer ID Data L	The standard ID or extended ID of received message can be read. Read bits 10 to 0 for standard ID. Bits 15 to 11 are read as 0.	R

This register can be read when the RPAGE bit in the GRWCR register is 1.

- RFID[15:0] Bits
  These bits indicate the ID of the message stored in the receive FIFO buffer.

18.3.42 CAN Receive FIFO Access Register mCH (RFDF1m) (m = 0 to 3)

Address RFDF10: F05AAH, RFDF11: F05BAH, RFDF12: F05CAH, RFDF13: F05DAH

The RFDF1m register can be accessed in 16-bit units. In addition, the RFDF1m register can be accessed in 8-bit units as RFDF1mL, RFDF1mH register.

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB3[7:0]								RFDB2[7:0]							
After Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
15 to 8	RFDB3[7:0]	Receive FIFO Buffer Data Byte 3	Data in the message stored in the receive FIFO buffer can be read.	R
7 to 0	RFDB2[7:0]	Receive FIFO Buffer Data Byte 2		R

When the RFDLC[3:0] value in the RFPTRm register is smaller than B'1000, data bytes for which no data is set are read as H'00.

This register can be read when the RPAGE bit in the GRWCR register is 1.

18.3.61 CANi Transmit Buffer Control Register p (TMCp) (i = 0, 1, p = 0 to 7)

Address CAN0 Transmit Buffer Control Register p (p = 0 to 3)
TMC0: F0364H, TMC1: F0365H, TMC2: F0366H, TMC3: F0367H
CAN1 Transmit Buffer Control Register p (p = 4 to 7)
TMC4: F0368H, TMC5: F0369H, TMC6: F036AH, TMC7: F036BH

The TMCp register can be accessed in 8-bit units.

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TMOM	TMTAR	TMTR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
7 to 3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R
2	TMOM	One-Shot Transmission Enable	0: One-shot transmission is disabled. 1: One-shot transmission is enabled.	R/W
1	TMTAR	Transmit Abort Request	0: Transmit abort is not requested. 1: Transmit abort is requested.	R/(W)Note
0	TMTR	Transmit Request	0: Transmission is not requested. 1: Transmission is requested.	R/(W)Note

Note The only effective value for writing to this bit is 1, which sets the bit. Otherwise writing to the bit results in retention of its state.

When the TMCp register meets any of the following conditions, set it to H'00.

- The TMCp register corresponds to the transmit buffer number selected by the CFTML[1:0] bits in the CFCCHk register.

Bits in the TMCp register are cleared to all 0 in channel reset mode. Modify the TMCp register only in channel communication mode or channel halt mode.

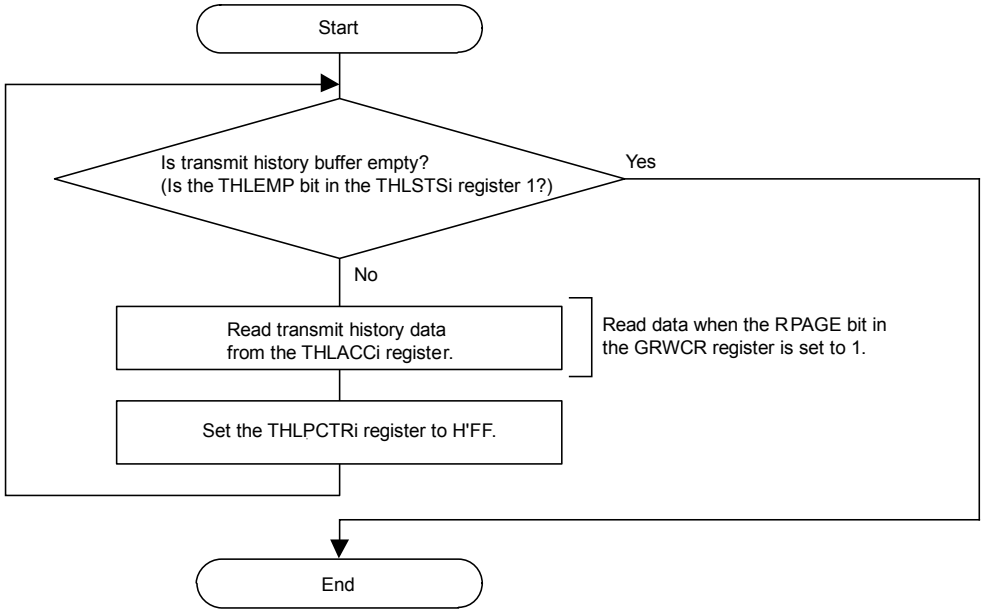
- TMOM Bit
  Setting this bit to 1 enables one-shot transmission. When transmission fails, retransmission defined in the CAN protocol is not performed.
  Modify the TMOM bit when the TMTRM flag in the TMSTSp register is set to 0. To set the TMOM bit to 1, also set the TMTR bit together.

- TMTAR Bit
  Setting this bit to 1 generates a transmit abort request for the message stored in the transmit buffer. However, a message that is being transmitted or to be transmitted next cannot be aborted.
  When the TMTR bit is set to 1, the TMTAR bit can be set to 1.
  The TMTAR bit is cleared to 0 when any of the following conditions is met, but is not cleared by writing 0 by the program.
  • Transmission has been completed.
  • Transmit abort has been completed.
  • An error or arbitration lost has been detected.
  If this bit becomes 0 at the timing when the program writes 1 to this bit, this bit becomes 0.

18.13.3 Transmit History Buffer Reading Procedure

Transmit history data can be read from the THLACCi register. The next data can be accessed by writing H'FF to the corresponding THLPCTRi register after reading a set of data. Figure 18-33 shows the transmit history buffer reading procedure.

Figure 18-33. Transmit History Buffer Reading Procedure



Remark i = 0, 1

28.3.11 Digital output signal level detection function for I/O ports

By using the digital output signal level detection function for I/O ports, the digital output level of the pin can be read when the port is set to output mode (the PMmn bit in the port mode register (PMm) is 0).

This function allows the output level of the pin to be read even when the PMnm (I/O mode) bit is set to output mode. As a result, the CPU can determine the current output level is a high or low level. For details on the registers to control this function, see **CHAPTER 4 PORT FUNCTIONS**.

<Control register>

(1) Port mode select register (PMS)

This register is used to select the output level from output latch level or pin output level when the port is output mode in which PMm bit of port mode register (PMm) is 0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 28-28. Format of Port Mode Select Register (PMS)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMS	0	0	0	0	0	0	0	PMS0

PMS0	Method for selecting output level to be read when port is output mode (PMmn = 0)
0	Pmn register value is read.
1	Output level of the pin is read.

Remark m = 0 to 16
n = 0 to 7

CHAPTER 31 FLASH MEMORY

The RL78/F15 incorporate the flash memory to which a program can be written, erased, and overwritten. The flash memory includes the “code flash memory”, in which programs can be executed, and the “data flash memory”, an area for storing data.

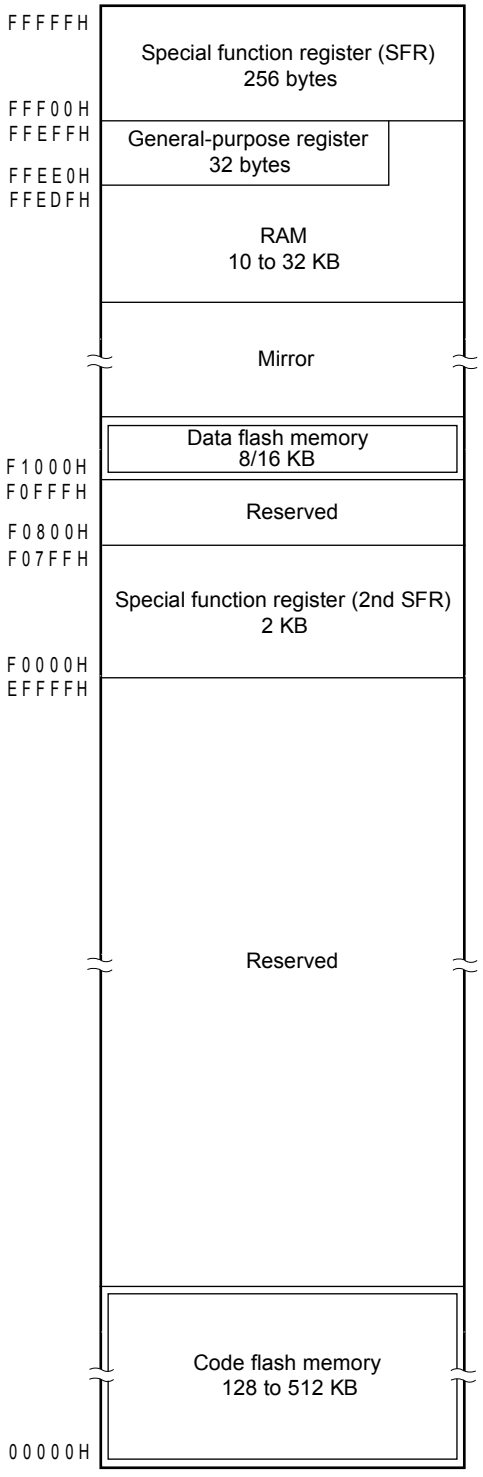


Table 34-5. Operation List (8/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	SUBC	A, #byte	2	1	–	A, CY ← A – byte – CY	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) – byte – CY	×	×	×
		A, r Note 3	2	1	–	A, CY ← A – r – CY	×	×	×
		r, A	2	1	–	r, CY ← r – A – CY	×	×	×
		A, !addr16	3	1	4	A, CY ← A – (addr16) – CY	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A – (ES, addr16) – CY	×	×	×
		A, saddr	2	1	–	A, CY ← A – (saddr) – CY	×	×	×
		A, [HL]	1	1	4	A, CY ← A – (HL) – CY	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A – (ES, HL) – CY	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A – (HL+byte) – CY	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A – ((ES, HL)+byte) – CY	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A – (HL+B) – CY	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A – ((ES, HL)+B) – CY	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A – (HL+C) – CY	×	×	×
		A, ES:[HL+C]	3	2	5	A, CY ← A – ((ES:HL)+C) – CY	×	×	×
	AND	A, #byte	2	1	–	A ← A ∧ byte	×		
		saddr, #byte	3	2	–	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	1	–	A ← A ∧ r	×		
		r, A	2	1	–	R ← r ∧ A	×		
		A, !addr16	3	1	4	A ← A ∧ (addr16)	×		
		A, ES:!addr16	4	2	5	A ← A ∧ (ES:addr16)	×		
		A, saddr	2	1	–	A ← A ∧ (saddr)	×		
		A, [HL]	1	1	4	A ← A ∧ (HL)	×		
		A, ES:[HL]	2	2	5	A ← A ∧ (ES:HL)	×		
		A, [HL+byte]	2	1	4	A ← A ∧ (HL+byte)	×		
		A, ES:[HL+byte]	3	2	5	A ← A ∧ ((ES:HL)+byte)	×		
		A, [HL+B]	2	1	4	A ← A ∧ (HL+B)	×		
		A, ES:[HL+B]	3	2	5	A ← A ∧ ((ES:HL)+B)	×		
		A, [HL+C]	2	1	4	A ← A ∧ (HL+C)	×		
		A, ES:[HL+C]	3	2	5	A ← A ∧ ((ES:HL)+C)	×		

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the program memory area is accessed.

3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.