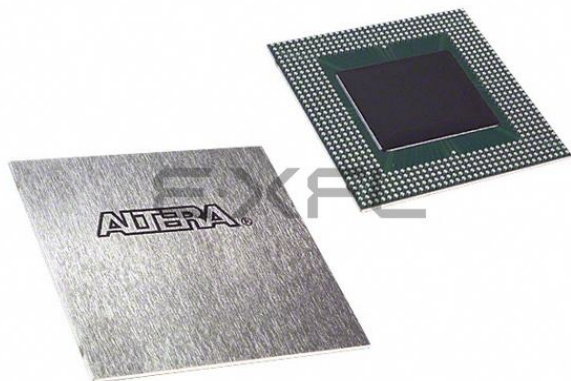




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	327680
Number of I/O	488
Number of Gates	1772000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1000ebc652-3

Table 2. Additional APEX 20K Device Features *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

Note to Tables 1 and 2:

- (1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

Additional Features

- Designed for low-power operation
 - 1.8-V and 2.5-V supply voltage (see Table 3)
 - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
 - ESB offering programmable power-saving mode

Table 3. APEX 20K Supply Voltages

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

Note to Table 3:

- (1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
 - Built-in low-skew clock tree
 - Up to eight global clock signals
 - ClockLock[®] feature reducing clock delay and skew
 - ClockBoost[®] feature providing clock multiplication and division
 - ClockShift[™] programmable clock phase and delay shifting
- Powerful I/O features
 - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
 - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
 - Bidirectional I/O performance ($t_{CO} + t_{SU}$) up to 250 MHz
 - LVDS performance up to 840 Mbits per channel
 - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
 - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
 - Programmable clamp to V_{CCIO}
 - Individual tri-state output enable control for each pin
 - Programmable output slew-rate control to reduce switching noise
 - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
 - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
 - Four-level hierarchical FastTrack[®] Interconnect structure providing fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
 - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
 - FineLine BGA[®] packages maximize board space efficiency
- Advanced software support
 - Software design support and automatic place-and-route provided by the Altera[®] Quartus[®] II development system for

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS)

Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

Functional Description

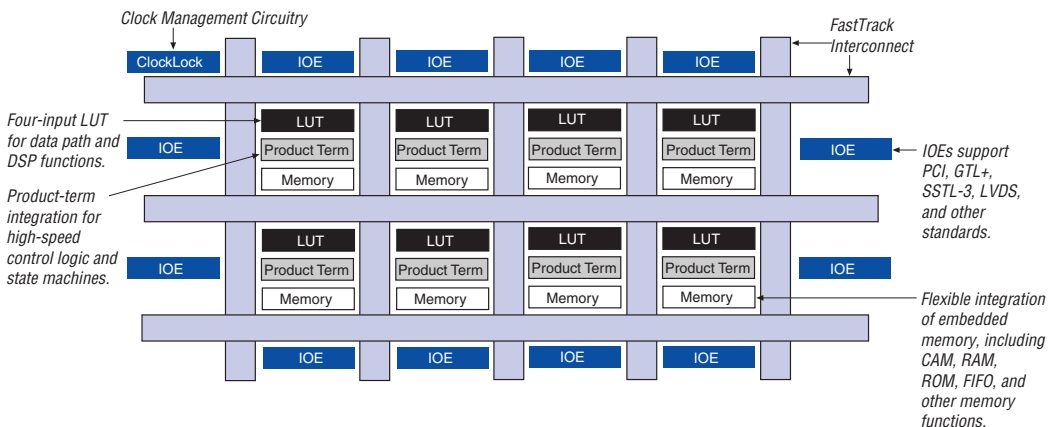
APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack[®] Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram



LE Operating Modes

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

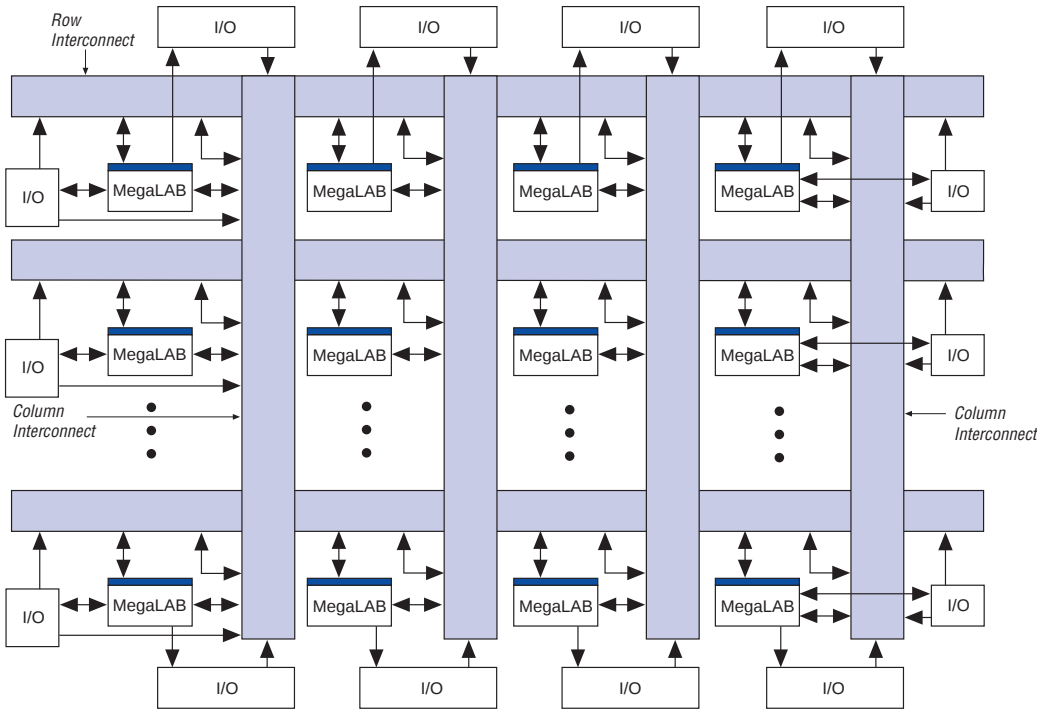
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 9. APEX 20K Interconnect Structure

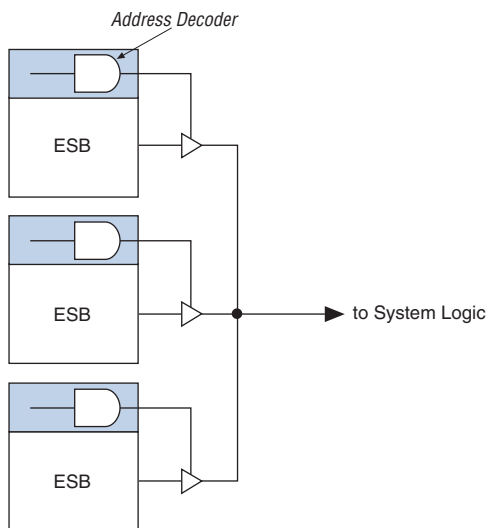


A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

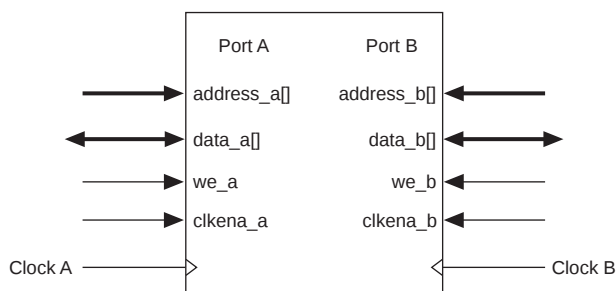
Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 18. Deep Memory Block Implemented with Multiple ESBs



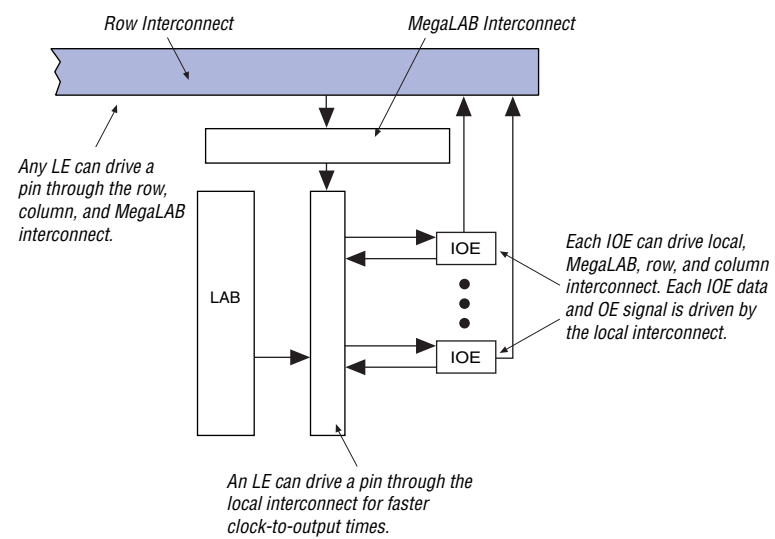
The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in [Figure 19](#).

Figure 19. APEX 20K ESB Implementing Dual-Port RAM



Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. **Figure 27** shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect



Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. [Figure 30](#) shows the incoming and generated clock specifications.



For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. [Tables 20 and 21](#) show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 (1)

Note to [Table 20](#):

- (1) This device does not support JTAG boundary scan testing.

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) Notes (2), (7), (8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 12 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (11)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (11)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (11)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11)			0.2	V
		$I_{OL} = 1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11)			0.4	V
		$I_{OL} = 2 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11)			0.7	V
I_I	Input pin leakage current	$V_I = 5.75 \text{ to } -0.5 \text{ V}$	-10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.75 \text{ to } -0.5 \text{ V}$	-10		10	μA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	$V_I = \text{ground}$, no load, no toggling inputs, -1 speed grade (12)		10		mA
		$V_I = \text{ground}$, no load, no toggling inputs, -2, -3 speed grades (12)		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0 \text{ V}$ (13)	20		50	W
		$V_{CCIO} = 2.375 \text{ V}$ (13)	30		80	W

Figure 37. APEX 20KE t_{MAX} Timing Model

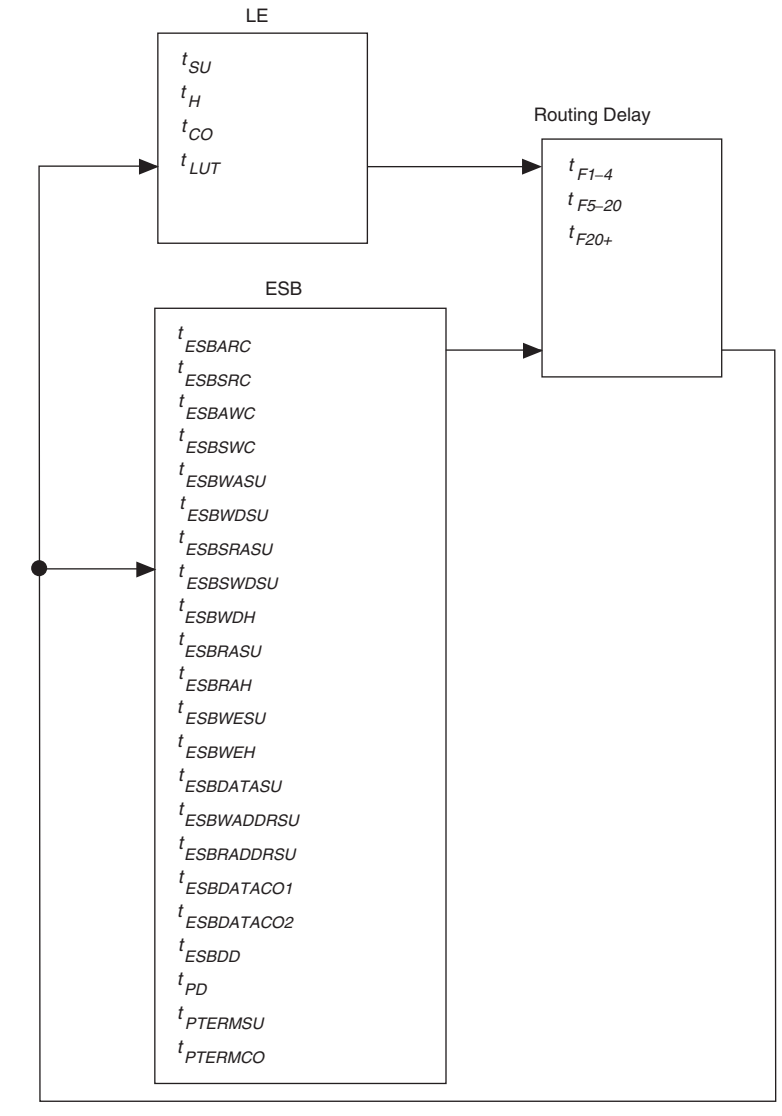


Table 50. EP20K30E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.03		2.86		4.24	ns
t_{ESBSRC}		2.58		3.49		5.02	ns
t_{ESBAWC}		3.88		5.45		8.08	ns
t_{ESBSWC}		4.08		5.35		7.48	ns
$t_{ESBWASU}$	1.77		2.49		3.68		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.95		2.74		4.05		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.96		2.75		4.07		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.80		2.73		4.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.48		1.17		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.30		0.80		1.64		ns
$t_{ESBRADDRSU}$	0.37		0.90		1.78		ns
$t_{ESBDATAO1}$		1.11		1.32		1.67	ns
$t_{ESBDATAO2}$		2.65		3.73		5.53	ns
t_{ESBDD}		3.88		5.45		8.08	ns
t_{PD}		1.91		2.69		3.98	ns
$t_{PTERMSU}$	1.04		1.71		2.82		ns
$t_{PTERMCO}$		1.13		1.34		1.69	ns

Table 51. EP20K30E t_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.31	ns
t_{F5-20}		1.03		1.14		1.30	ns
t_{F20+}		1.42		1.54		1.77	ns

Tables 85 through 90 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

Table 85. EP20K400E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.23		0.23		ns
t_H	0.23		0.23		0.23		ns
t_{CO}		0.25		0.29		0.32	ns
t_{LUT}		0.70		0.83		1.01	ns

Table 86. EP20K400E t_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		1.91		1.99	ns
t_{ESBSRC}		2.30		2.66		2.93	ns
t_{ESBAWC}		3.09		3.58		3.99	ns
t_{ESBSWC}		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
t_{ESBWAH}	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
t_{ESBWDH}	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
t_{ESBDD}		2.73		3.17		3.58	ns
t_{PD}		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

Table 87. EP20K400E t_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.25		0.26	ns
t_{F5-20}		1.01		1.12		1.25	ns
t_{F20+}		3.71		3.92		4.17	ns

Table 88. EP20K400E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.22		2.35		ns
t_{CL}	1.36		2.26		2.35		ns
t_{CLRP}	0.18		0.18		0.19		ns
t_{PREP}	0.18		0.18		0.19		ns
t_{ESBCH}	1.36		2.26		2.35		ns
t_{ESBCL}	1.36		2.26		2.35		ns
t_{ESBWP}	1.17		1.38		1.56		ns
t_{ESBRP}	0.94		1.09		1.25		ns

Table 89. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.51		2.64		2.77		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

Table 99. EP20K1000E t_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.27		0.27		0.27	ns
t_{F5-20}		1.45		1.63		1.75	ns
t_{F20+}		4.15		4.33		4.97	ns

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 101. EP20K1000E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.70		2.84		2.97		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{INSUPLL}$	1.64		2.09		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.25		1.43		1.67		ns
t _{CL}	1.25		1.43		1.67		ns
t _{CLRP}	0.20		0.20		0.20		ns
t _{PREP}	0.20		0.20		0.20		ns
t _{ESBCH}	1.25		1.43		1.67		ns
t _{ESBCL}	1.25		1.43		1.67		ns
t _{ESBWP}	1.28		1.51		1.65		ns
t _{ESBRP}	1.11		1.29		1.41		ns

Table 107. EP20K1500E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	3.09		3.30		3.58		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	6.18	2.00	6.81	2.00	7.36	ns
t _{INSUPLL}	1.94		2.08		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.67	0.50	2.99	-	-	ns

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).