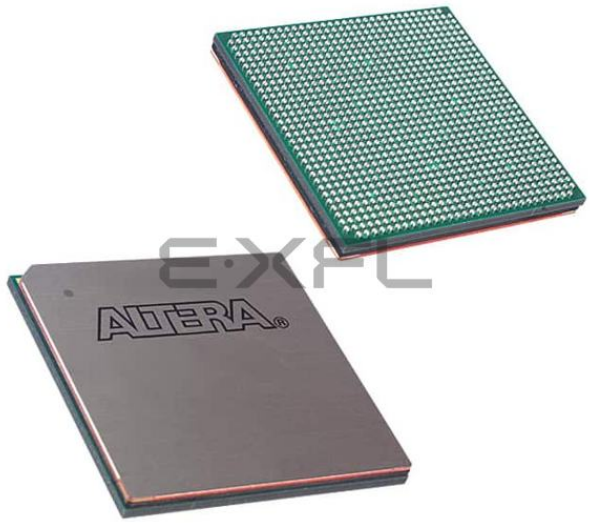

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	327680
Number of I/O	708
Number of Gates	1772000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1000efc33-2

Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure

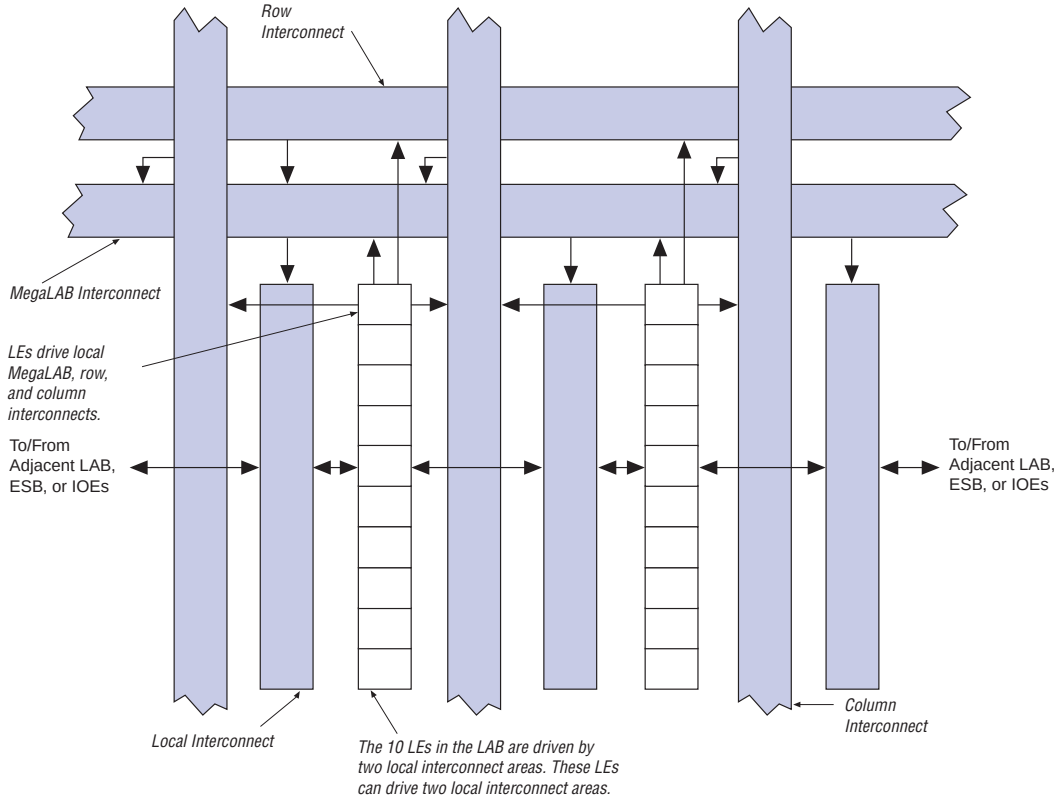


Figure 6. APEX 20K Carry Chain

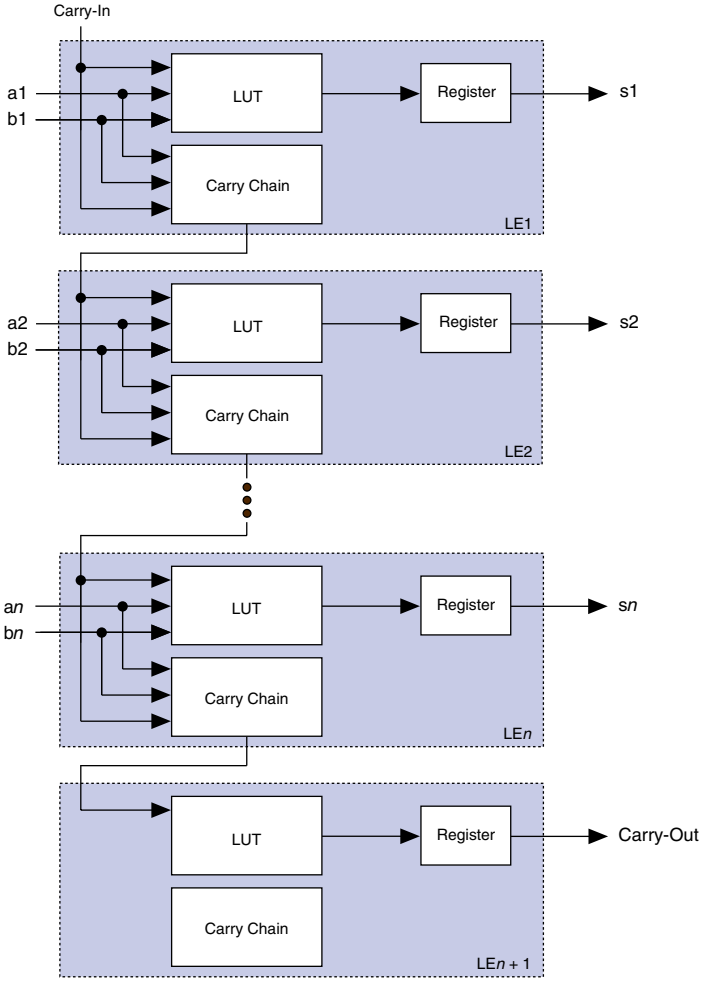
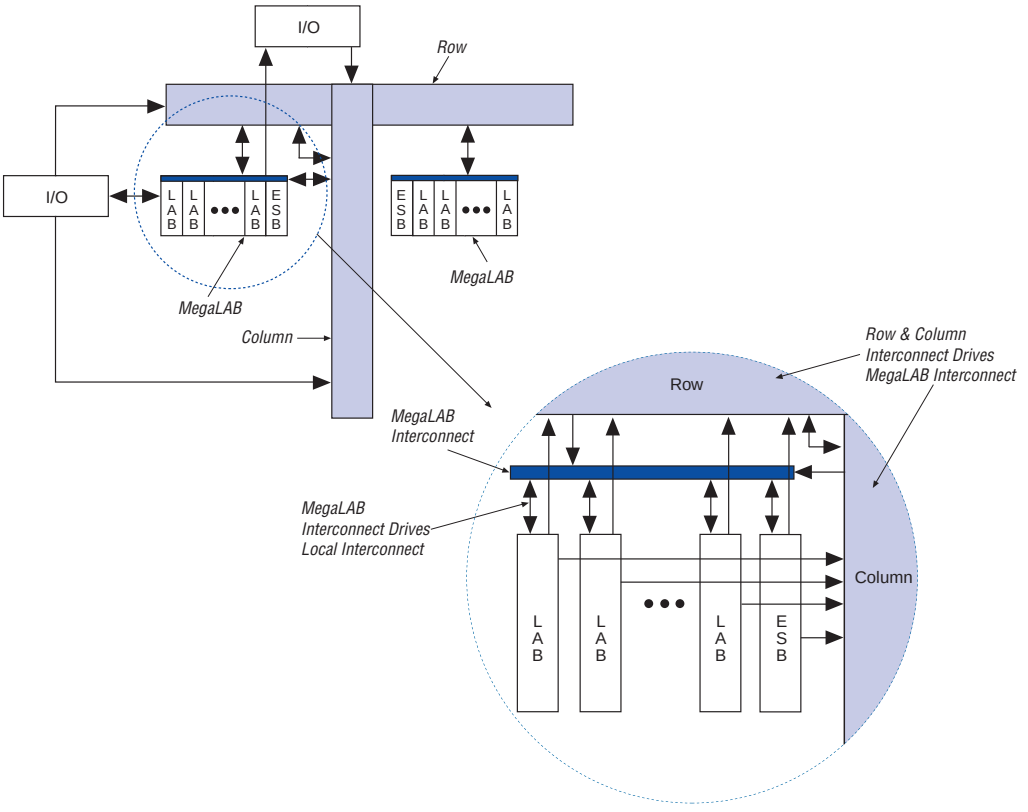


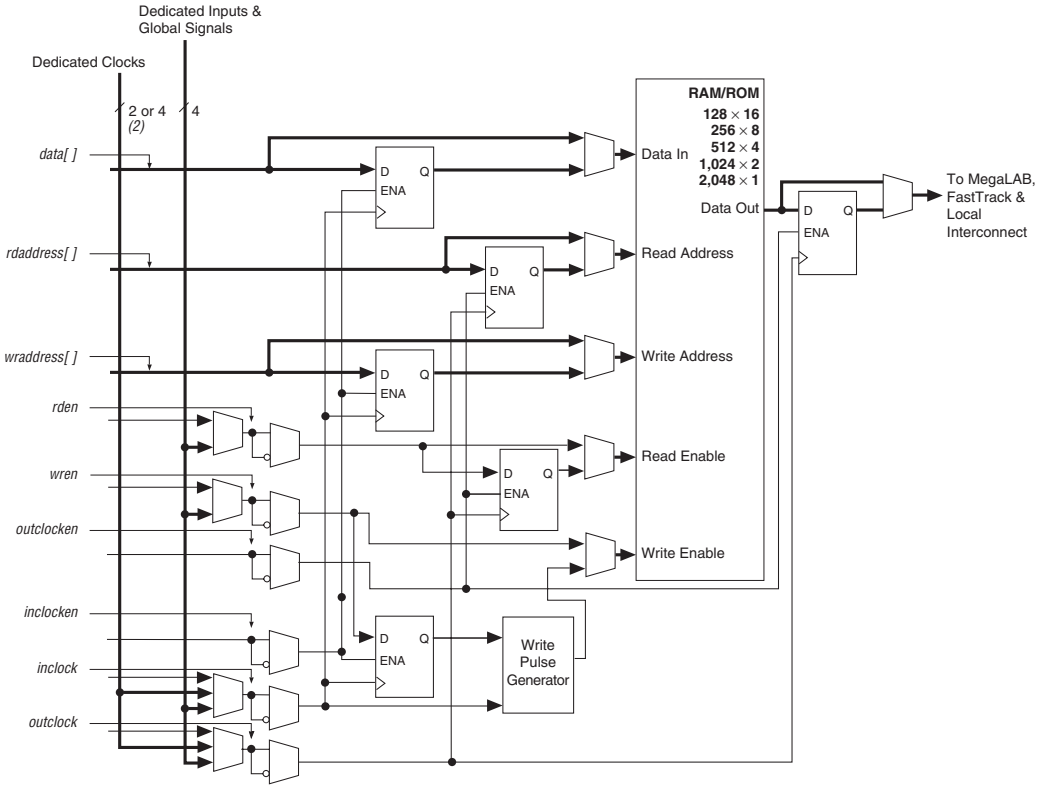
Figure 10. FastTrack Connection to Local Interconnect



Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

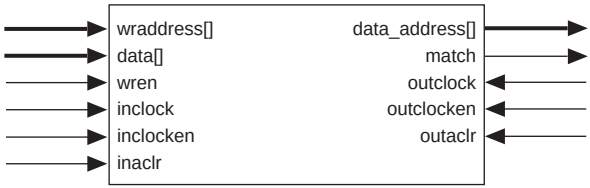
Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Notes to Figure 20:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Figure 23. APEX 20KE CAM Block Diagram



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't-care" bit can be used as a mask for CAM comparisons; any bit set to "don't-care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address `12`, the ESB output is `12`. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address `12`, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't-care" bits are used, a third clock cycle is required.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

Table 10. APEX 20K Programmable Delay Chains

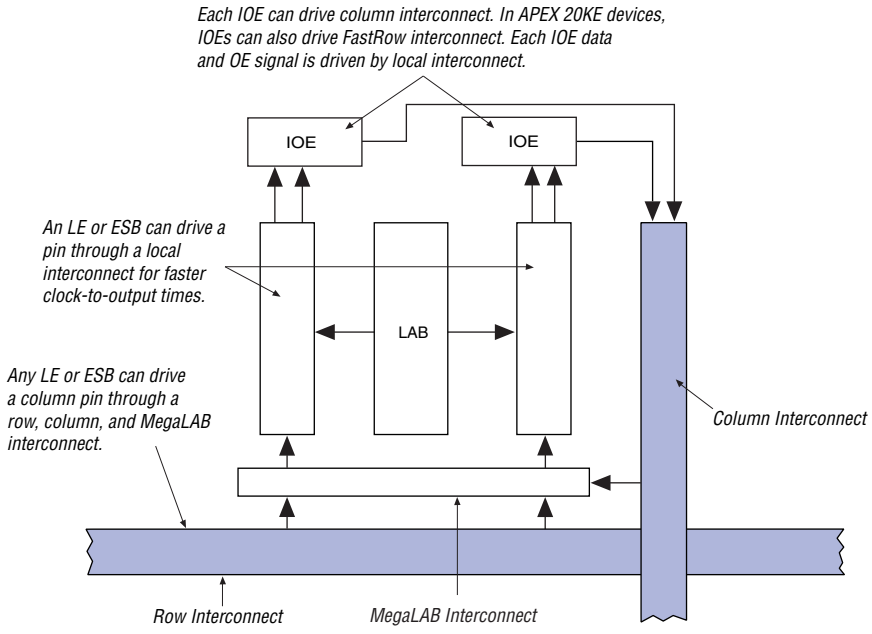
Programmable Delays	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 28 shows how a column IOE connects to the interconnect.

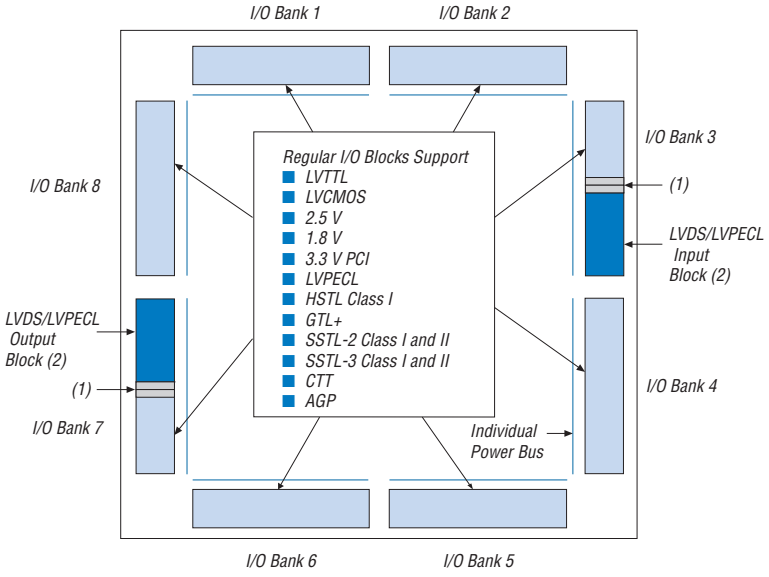
Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Figure 29. APEX 20KE I/O Banks



Notes to Figure 29:

(1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices*).

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

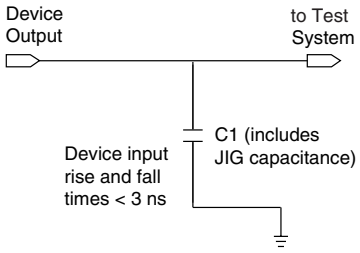
Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Figure 32. APEX 20K AC Test Conditions *Note (1)*



Note to Figure 32:

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 26. APEX 20K 5.0-V Tolerant Device Capacitance *Notes (2), (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 23 through 26:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
(10) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
(11) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 27. APEX 20KE Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 28. APEX 20KE Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	*(5)*, *(6)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the f_{MAX} timing model for APEX 20K devices.

Figure 36. APEX 20K f_{MAX} Timing Model

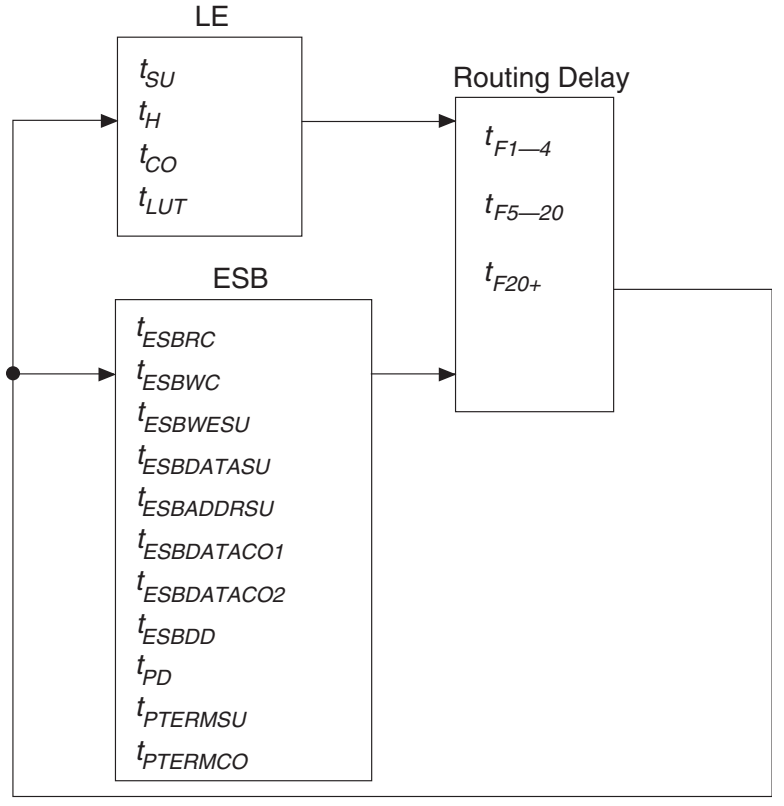
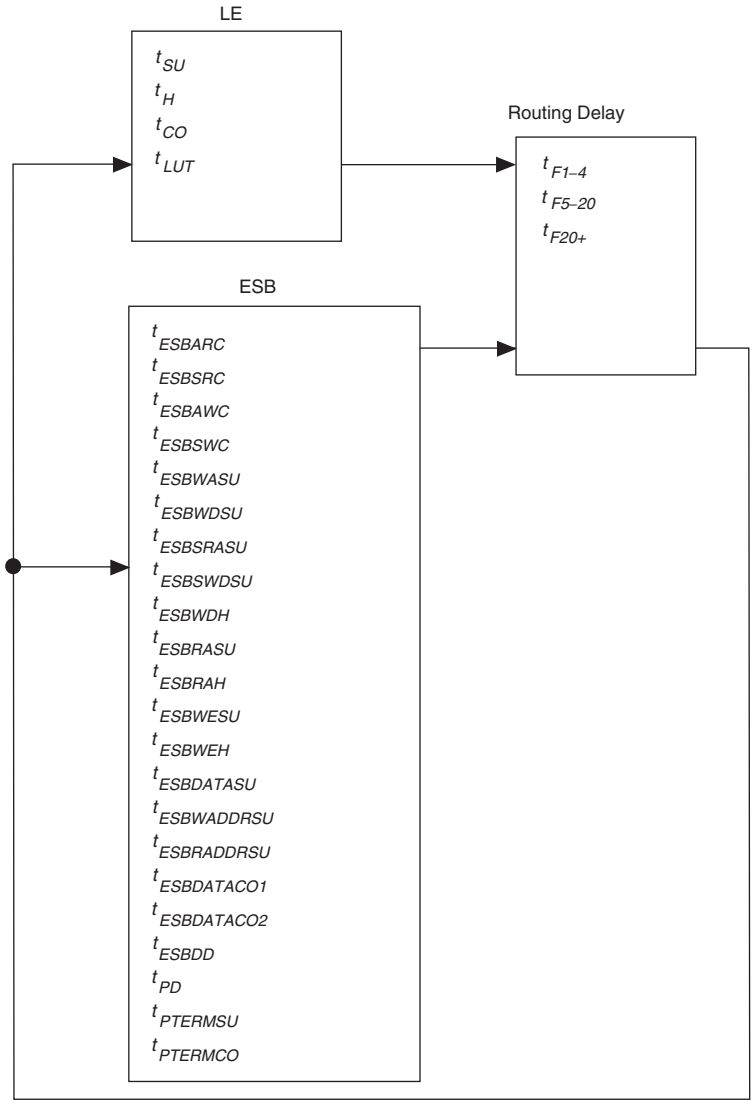


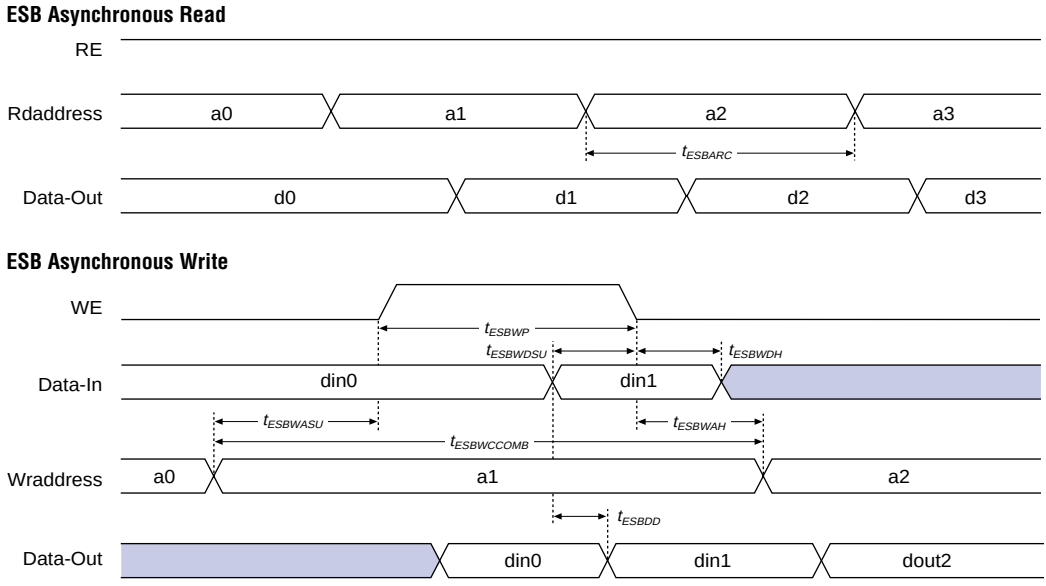
Figure 37 shows the f_{MAX} timing model for APEX 20KE devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Figure 37. APEX 20KE f_{MAX} Timing Model



Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms



Note to Tables 32 and 33:
(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the f_{MAX} timing model.

Table 34. APEX 20KE LE Timing Microparameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 35. APEX 20KE ESB Timing Microparameters

Symbol	Parameter
t_{ESBARC}	ESB Asynchronous read cycle time
t_{ESBSRC}	ESB Synchronous read cycle time
t_{ESBAWC}	ESB Asynchronous write cycle time
t_{ESBSWC}	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
t_{ESBWEH}	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

Table 50. EP20K30E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.03		2.86		4.24	ns
t_{ESBSRC}		2.58		3.49		5.02	ns
t_{ESBAWC}		3.88		5.45		8.08	ns
t_{ESBSWC}		4.08		5.35		7.48	ns
$t_{ESBWASU}$	1.77		2.49		3.68		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.95		2.74		4.05		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.96		2.75		4.07		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.80		2.73		4.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.48		1.17		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.30		0.80		1.64		ns
$t_{ESBRADDRSU}$	0.37		0.90		1.78		ns
$t_{ESBDATACO1}$		1.11		1.32		1.67	ns
$t_{ESBDATACO2}$		2.65		3.73		5.53	ns
t_{ESBDD}		3.88		5.45		8.08	ns
t_{PD}		1.91		2.69		3.98	ns
$t_{PTERMSU}$	1.04		1.71		2.82		ns
$t_{PTERMCO}$		1.13		1.34		1.69	ns

Table 51. EP20K30E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.31	ns
t_{F5-20}		1.03		1.14		1.30	ns
t_{F20+}		1.42		1.54		1.77	ns

Table 72. EP20K160E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.86		3.24		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{XZBIDIR}$		7.43		8.23		8.58	ns
$t_{ZXBIDIR}$		7.43		8.23		8.58	ns
$t_{INSUBIDIRPLL}$	4.93		5.48		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{XZBIDIRPLL}$		5.36		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.36		5.99		-	ns

Tables 73 through 78 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

Table 73. EP20K200E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.24		0.26		ns
t_{H}	0.23		0.24		0.26		ns
t_{CO}		0.26		0.31		0.36	ns
t_{LUT}		0.70		0.90		1.14	ns

Table 86. EP20K400E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		1.91		1.99	ns
t_{ESBSRC}		2.30		2.66		2.93	ns
t_{ESBAWC}		3.09		3.58		3.99	ns
t_{ESBSWC}		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
t_{ESBWAH}	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
t_{ESBWDH}	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
t_{ESBDD}		2.73		3.17		3.58	ns
t_{PD}		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

Table 90. EP20K400E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.93		3.23		3.44		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{XZBIDIR}$		5.95		6.77		7.12	ns
$t_{ZXBIDIR}$		5.95		6.77		7.12	ns
$t_{INSUBIDIRPLL}$	4.31		4.76		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.25	0.50	2.45	-	-	ns
$t_{XZBIDIRPLL}$		2.94		3.43		-	ns
$t_{ZXBIDIRPLL}$		2.94		3.43		-	ns

Tables 91 through 96 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K600E APEX 20KE devices.

Table 91. EP20K600E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.16		0.17		ns
t_{H}	0.29		0.33		0.37		ns
t_{CO}		0.65		0.38		0.49	ns
t_{LUT}		0.70		1.00		1.30	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.47		3.68		3.99		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{XZBIDIR}$		6.91		7.62		8.38	ns
$t_{ZXBIDIR}$		6.91		7.62		8.38	ns
$t_{INSUBIDIRPLL}$	3.05		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.67	0.50	2.99			ns
$t_{XZBIDIRPLL}$		3.41		3.80			ns
$t_{ZXBIDIRPLL}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		–0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		–0.24		–0.23		–0.19	ns
SSTL-3 Class I		–0.32		–0.21		–0.47	ns
SSTL-3 Class II		–0.08		0.03		–0.23	ns
SSTL-2 Class I		–0.17		–0.06		–0.32	ns
SSTL-2 Class II		–0.16		–0.05		–0.31	ns
LVDS		–0.12		–0.12		–0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns