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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	252
Number of Gates	263000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k100bc356-1

Table 2. Additional APEX 20K Device Features *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

Note to Tables 1 and 2:

(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

Additional Features

- Designed for low-power operation
 - 1.8-V and 2.5-V supply voltage (see [Table 3](#))
 - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
 - ESB offering programmable power-saving mode

Table 3. APEX 20K Supply Voltages

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

Note to Table 3:

(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

Table 5. APEX 20K FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

Notes to Tables 4 and 5:

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm ²)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 7. APEX 20K FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

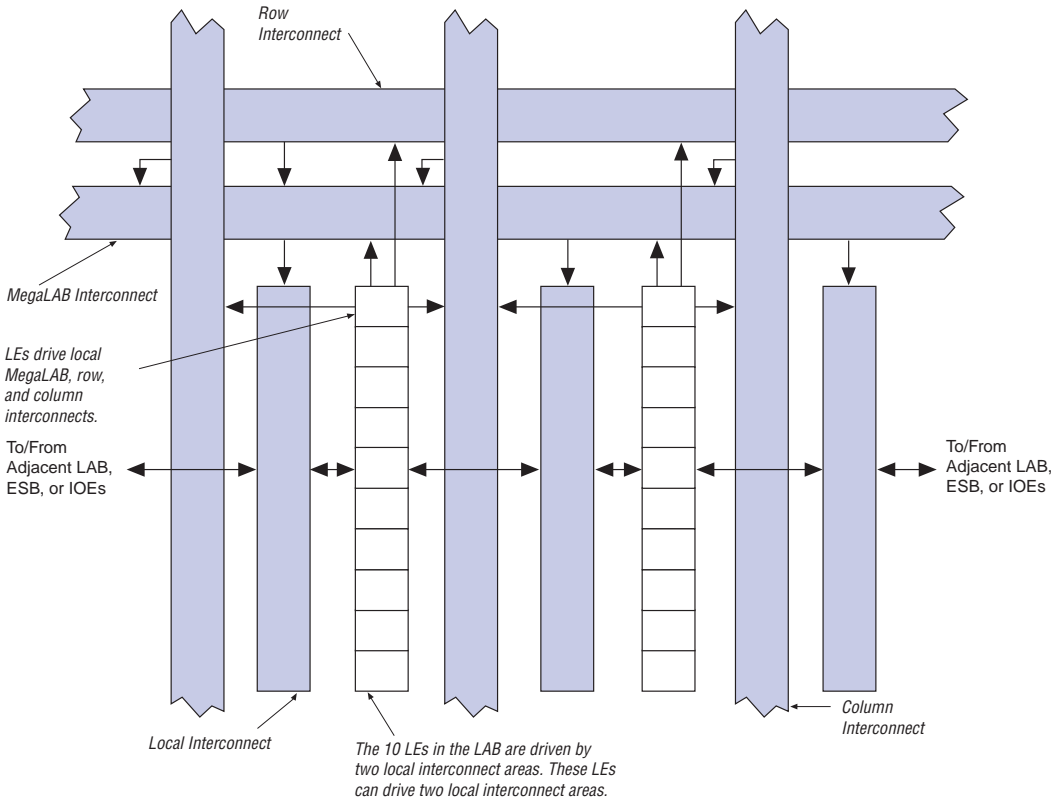
The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

Figure 3. LAB Structure



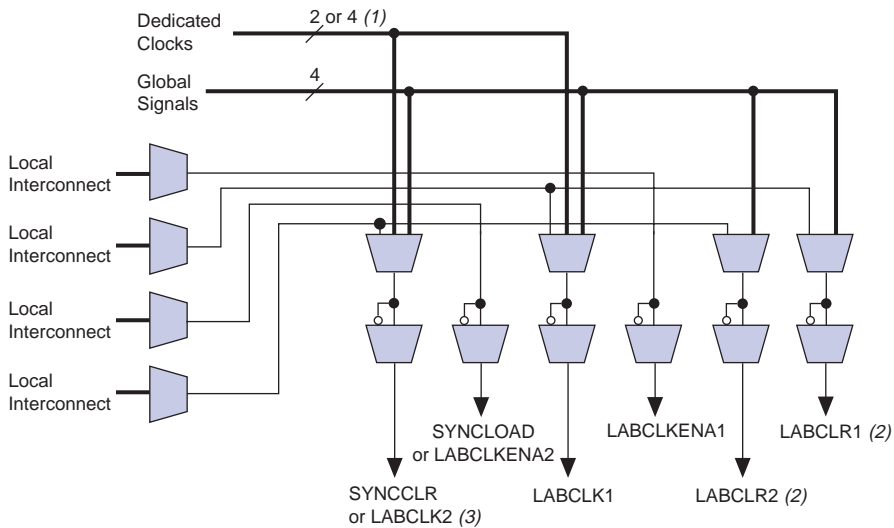
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. **Figure 4** shows the LAB control signal generation circuit.

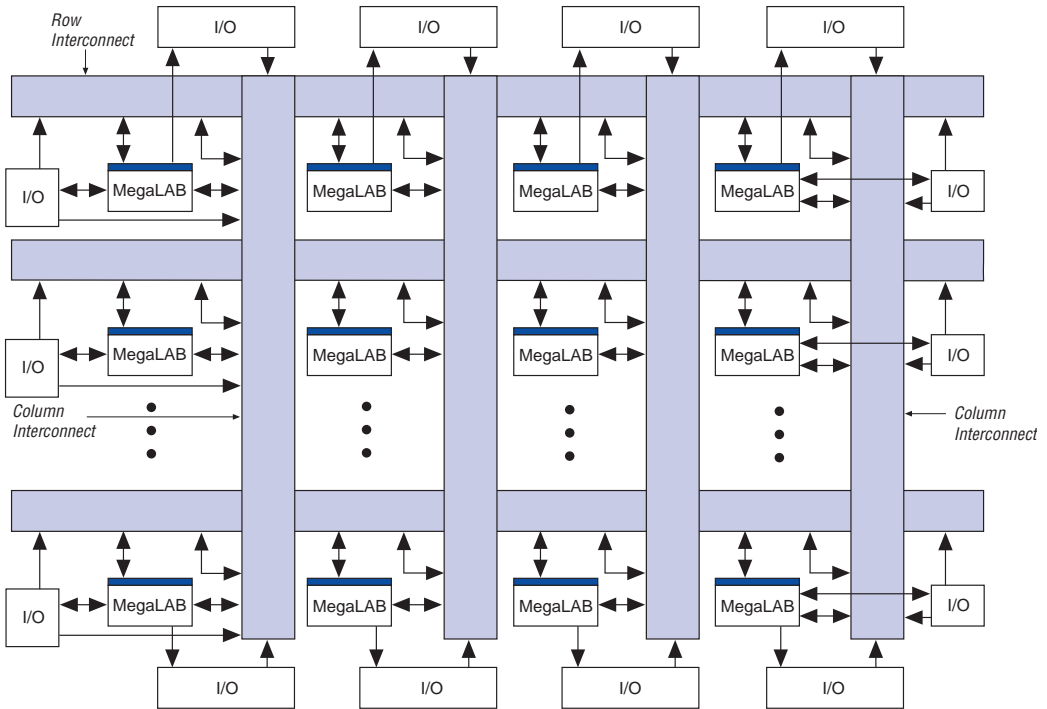
Figure 4. LAB Control Signal Generation



Notes to Figure 4:

- (1) APEX 20KE devices have four dedicated clocks.
- (2) The LABCLER1 and LABCLER2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
- (3) The SYNCCLR signal can be generated by the local interconnect or global signals.

Figure 9. APEX 20K Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

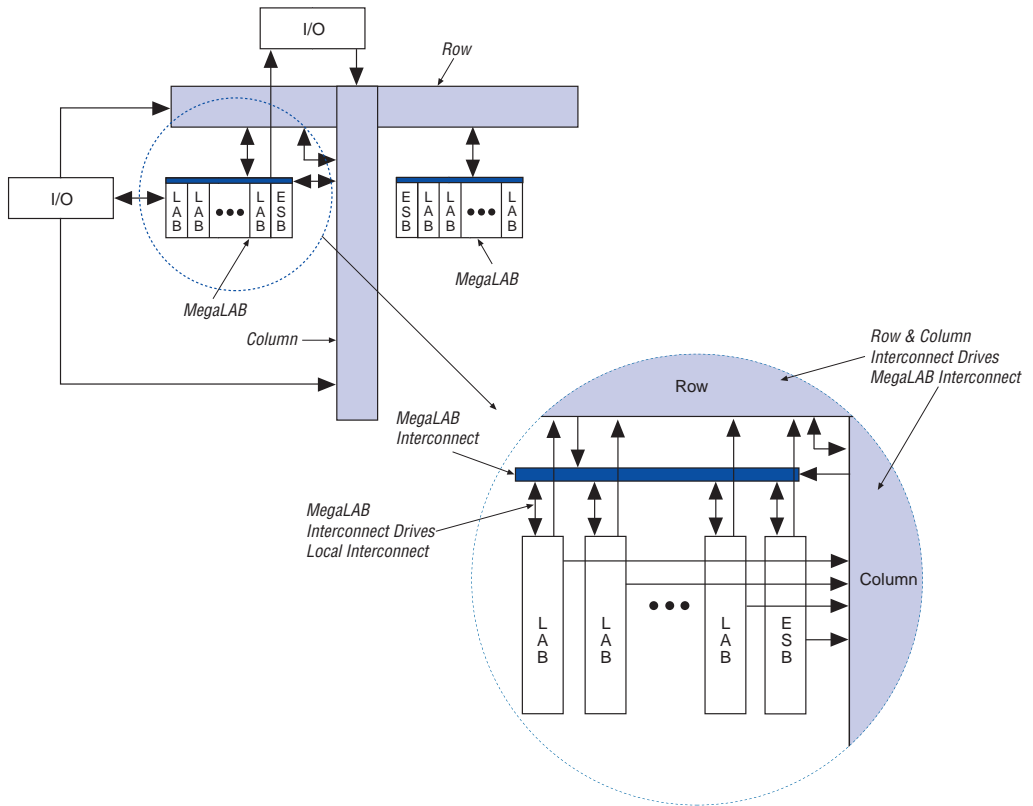
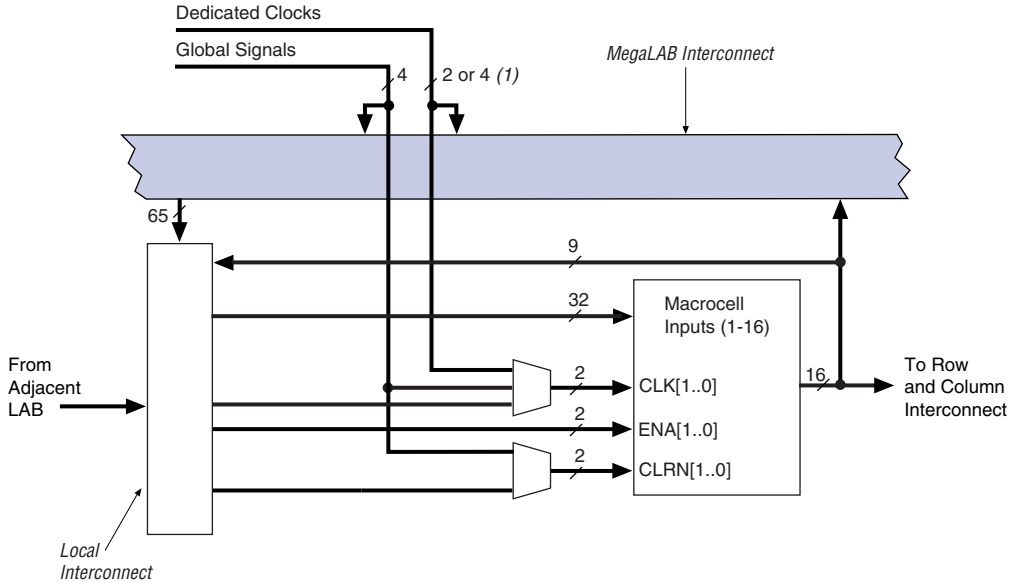


Figure 13. Product-Term Logic in ESB



Note to Figure 13:

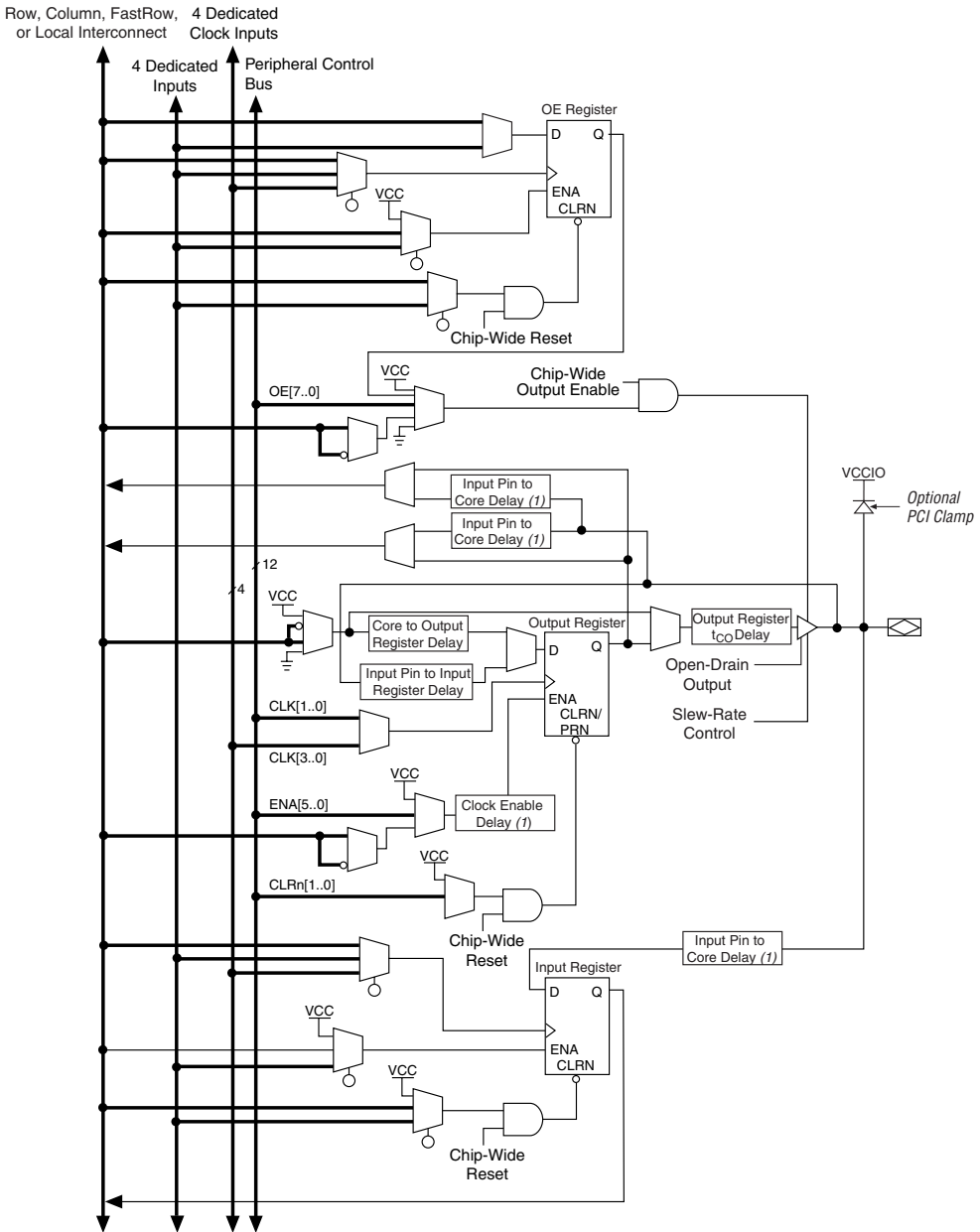
(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan’s inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

Figure 26. APEX 20KE Bidirectional I/O Registers Notes (1), (2)

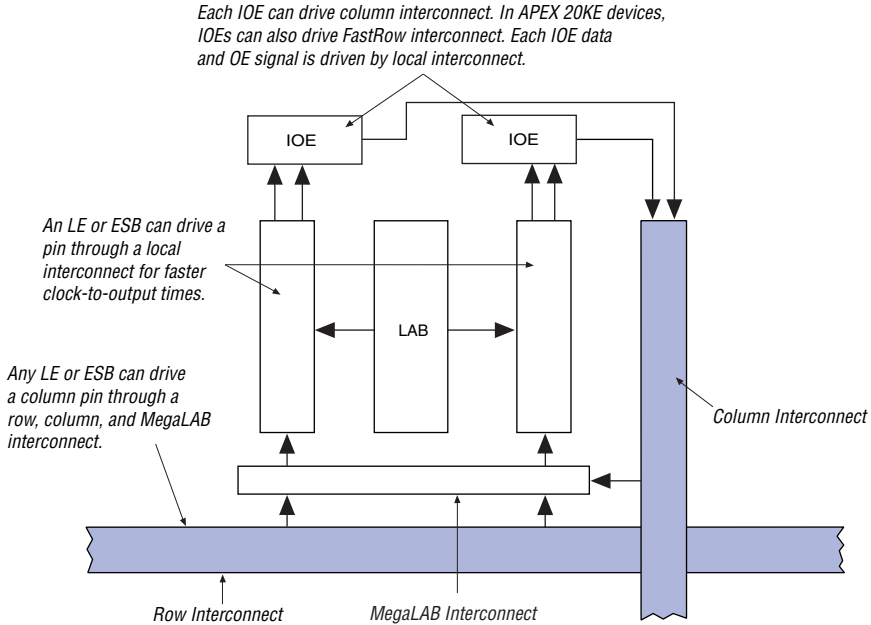


Notes to Figure 26:

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V VCCINT level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

Table 13. APEX 20KE MultiVolt I/O Support <i>Note (1)</i>								
V _{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓	(2)			✓(3)	

Notes to Table 13:

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.
- (2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.
- (3) When V_{CCIO} = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device’s high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length	
Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 (1)

Note to Table 20:

(1) This device does not support JTAG boundary scan testing.

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms

ESB Asynchronous Read



ESB Asynchronous Write



Figure 39. ESB Synchronous Timing Waveforms



Figure 40 shows the timing model for bidirectional I/O pin timing.

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.86		3.24		3.54		ns
t_{INHBDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
t_{XZBIDIR}		7.43		8.23		8.58	ns
t_{ZXBIDIR}		7.43		8.23		8.58	ns
$t_{\text{INSUBIDIRPLL}}$	4.93		5.48		-		ns
$t_{\text{INHBDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.36		5.99		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.36		5.99		-	ns

Tables 73 through 78 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.24		0.26		ns
t_{H}	0.23		0.24		0.26		ns
t_{CO}		0.26		0.31		0.36	ns
t_{LUT}		0.70		0.90		1.14	ns

Table 76. EP20K200E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.36		2.44		2.65		ns
t _{CL}	1.36		2.44		2.65		ns
t _{CLRP}	0.18		0.19		0.21		ns
t _{PREP}	0.18		0.19		0.21		ns
t _{ESBCH}	1.36		2.44		2.65		ns
t _{ESBCL}	1.36		2.44		2.65		ns
t _{ESBWP}	1.18		1.48		1.76		ns
t _{ESBRP}	0.95		1.17		1.41		ns

Table 77. EP20K200E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.24		2.35		2.47		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.12	2.00	5.62	2.00	6.11	ns
t _{INSUPLL}	2.13		2.07		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	3.01	0.50	3.36	-	-	ns

Table 92. EP20K600E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		2.39		3.11	ns
t_{ESBSRC}		2.27		3.07		3.86	ns
t_{ESBAWC}		3.19		4.56		5.93	ns
t_{ESBSWC}		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATACO1}$		1.01		1.19		1.37	ns
$t_{ESBDATACO2}$		2.18		3.12		4.05	ns
t_{ESBDD}		3.19		4.56		5.93	ns
t_{PD}		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

Table 93. EP20K600E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.25		0.26	ns
t_{F5-20}		1.26		1.39		1.52	ns
t_{F20+}		3.51		3.88		4.26	ns

Table 94. EP20K600E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	2.00		2.50		2.75		ns
t _{CL}	2.00		2.50		2.75		ns
t _{CLRP}	0.18		0.26		0.34		ns
t _{PREP}	0.18		0.26		0.34		ns
t _{ESBCH}	2.00		2.50		2.75		ns
t _{ESBCL}	2.00		2.50		2.75		ns
t _{ESBWP}	1.17		1.68		2.18		ns
t _{ESBRP}	0.95		1.35		1.76		ns

Table 95. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.74		2.74		2.87		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.51	2.00	6.06	2.00	6.61	ns
t _{INSUPLL}	1.86		1.96		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.62	0.50	2.91	-	-	ns

Table 96. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	0.64		0.98		1.08		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	5.51	2.00	6.06	2.00	6.61	ns
t _{XZBIDIR}		6.10		6.74		7.10	ns
t _{ZXBIDIR}		6.10		6.74		7.10	ns
t _{INSUBIDIRPLL}	2.26		2.68		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.62	0.50	2.91	-	-	ns
t _{XZBIDIRPLL}		3.21		3.59		-	ns
t _{ZXBIDIRPLL}		3.21		3.59		-	ns

Table 102. EP20K1000E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.22		3.33		3.51		ns
$t_{\text{INHIBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
t_{XZBIDIR}		6.31		7.09		7.76	ns
t_{ZXBIDIR}		6.31		7.09		7.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.25		3.26				ns
$t_{\text{INHIBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.25	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		2.81		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		2.81		3.80			ns

Tables 103 through 108 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

Table 103. EP20K1500E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.32		0.33	ns
t_{LUT}		0.80		0.95		1.13	ns

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).