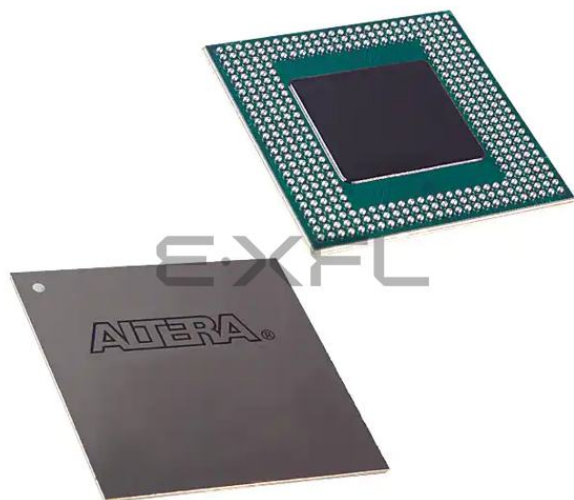




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	252
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100bc356-2

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

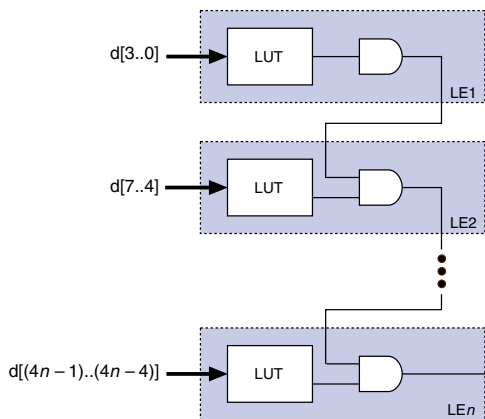
Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain

AND Cascade Chain



OR Cascade Chain

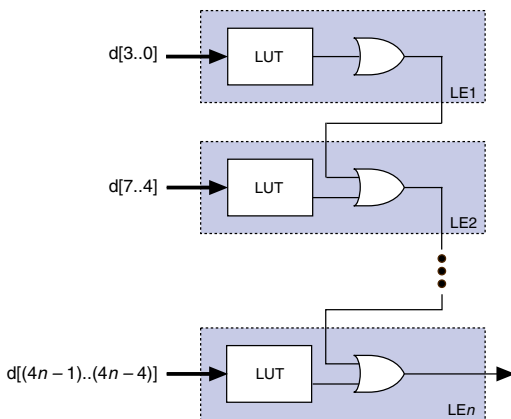
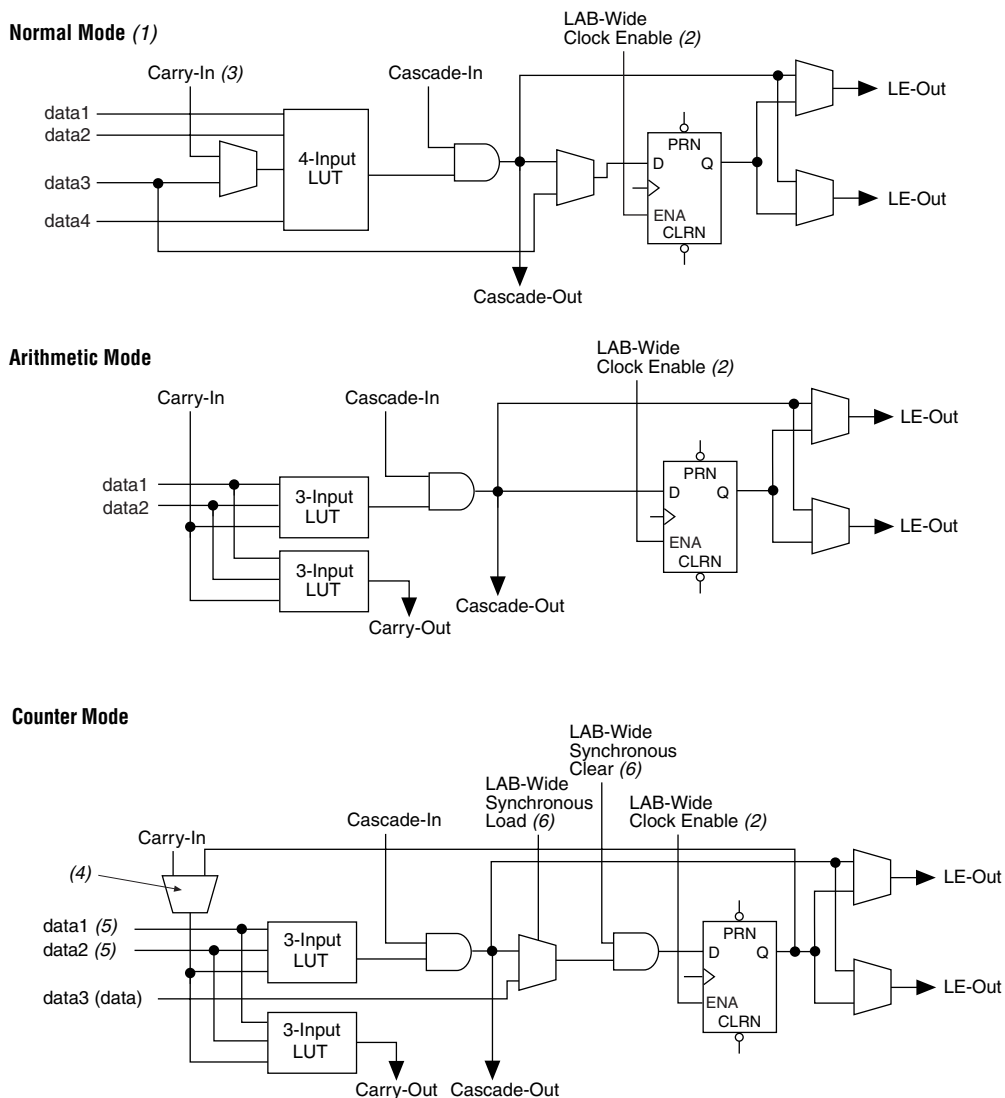


Figure 8. APEX 20K LE Operating Modes



Notes to Figure 8:

- (1) LEs in normal mode support register packing.
- (2) There are two LAB-wide clock enables per LAB.
- (3) When using the carry-in in normal mode, the packed register feature is unavailable.
- (4) A register feedback multiplexer is available on LE1 of each LAB.
- (5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
- (6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

Figure 12. APEX 20KE FastRow Interconnect

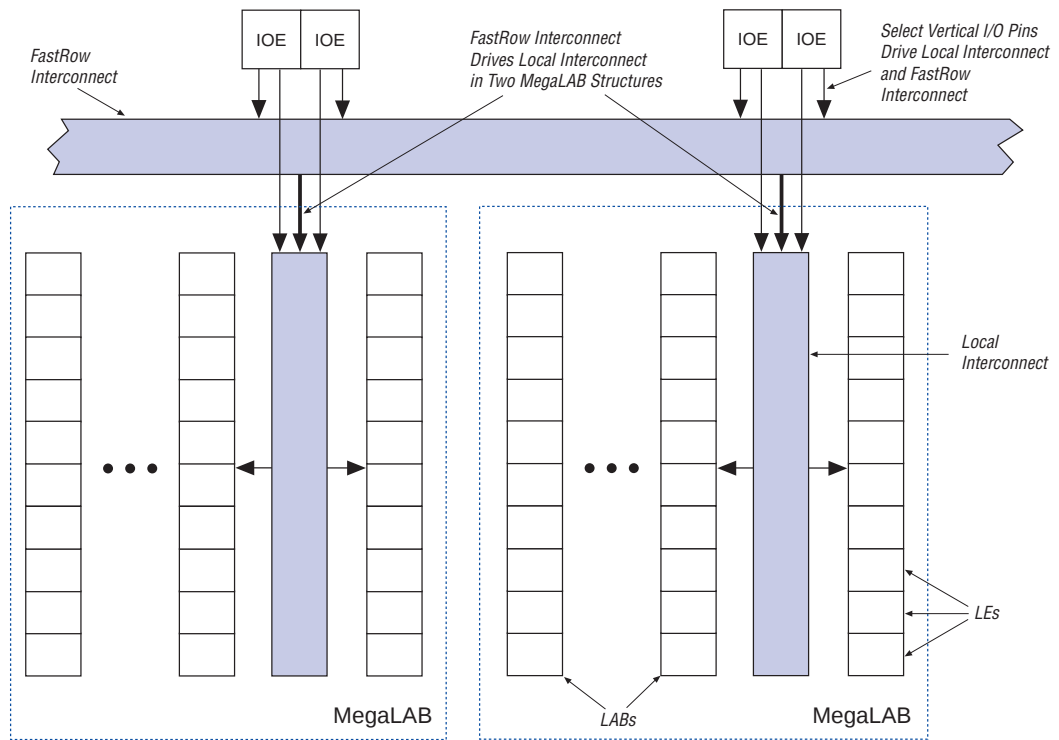
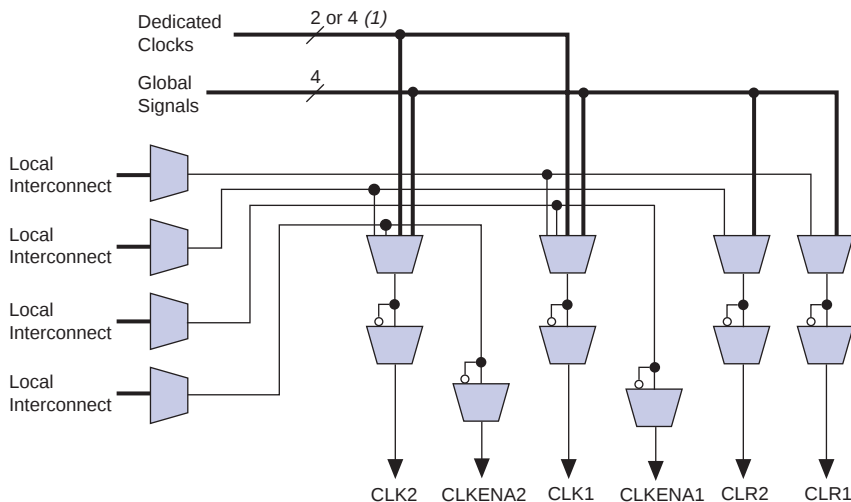


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Note to Figure 15:

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

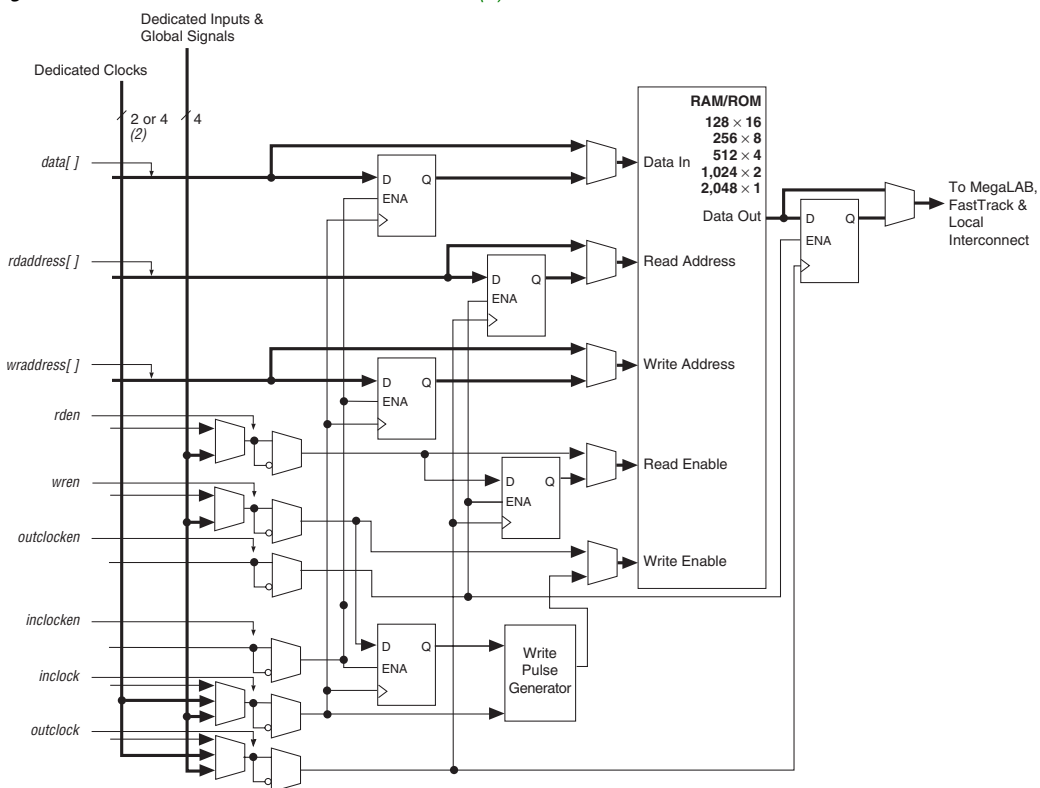
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Notes to Figure 20:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

Table 10. APEX 20K Programmable Delay Chains	
Programmable Delays	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock (5)		200	ps
t_{INCLKSTB}	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:

- (1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
- (2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
- (4) The jitter specification is measured under long-term observation.
- (5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
t_{OUTDUTY}	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) (1)		25,000 (2)	PPM
t_{R}	Input rise time		5	ns
t_{F}	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock (3)		10	μs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock (4)		200	ps
t_{INCLKSTB}	Input clock stability (measured between adjacent clocks)		50	ps

Table 18. APEX 20KE Clock Input & Output Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f_{IN}	Input clock frequency	3.3-V LVTTL	1.5	290	1.5	257	MHz
		2.5-V LVTTL	1.5	281	1.5	250	MHz
		1.8-V LVTTL	1.5	272	1.5	243	MHz
		GTL+	1.5	303	1.5	261	MHz
		SSTL-2 Class I	1.5	291	1.5	253	MHz
		SSTL-2 Class II	1.5	291	1.5	253	MHz
		SSTL-3 Class I	1.5	300	1.5	260	MHz
		SSTL-3 Class II	1.5	300	1.5	260	MHz
		LVDS	1.5	420	1.5	350	MHz

Notes to Tables 17 and 18:

- (1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
- (2) The maximum lock time is 40 μ s or 2000 input clock cycles, whichever occurs first.
- (3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the CLKLK_ENA pin goes high in user mode.
- (4) The PLL VCO operating range is 200 MHz δ f_{VCO} δ 840 MHz for LVDS mode.

SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) ⁽¹⁾			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) ⁽²⁾
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 21:

- (1) The most significant bit (MSB) is on the left.
 (2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

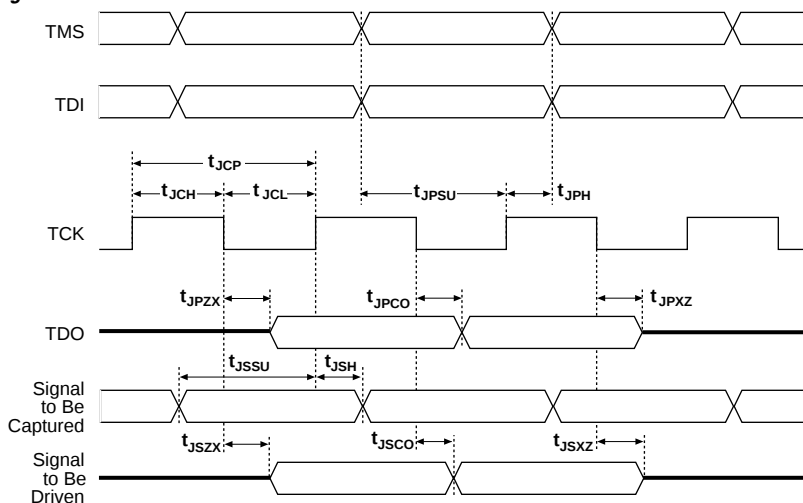
Figure 31. APEX 20K JTAG Waveforms

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

Table 22. APEX 20K JTAG Timing Parameters & Values				
Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	(3), (6)	-0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (9)		5.75	V
V_{IL}	Low-level input voltage		-0.5		$0.8, 0.3 \times V_{CCIO}$ (9)	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (10)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (10)	1.7			V

Figure 39. ESB Synchronous Timing Waveforms

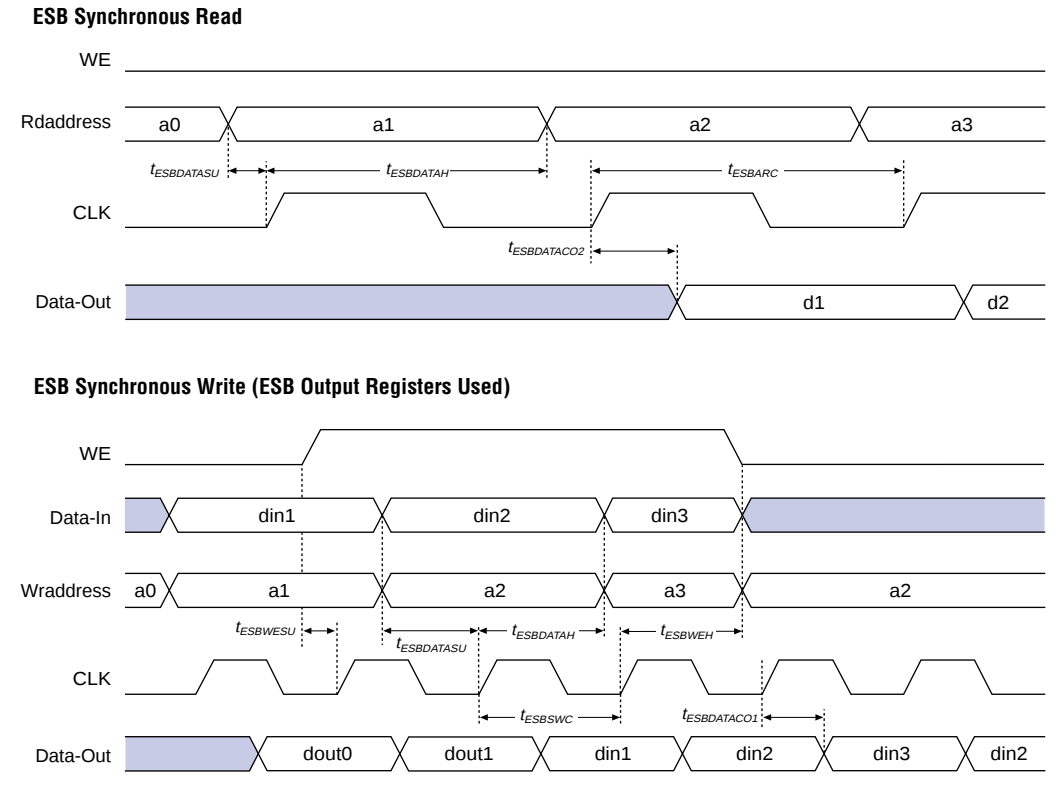


Figure 40 shows the timing model for bidirectional I/O pin timing.

Table 36. APEX 20KE Routing Timing Microparameters *Note (1)*

Symbol	Parameter
t_{F1-4}	Fanout delay using Local Interconnect
t_{F5-20}	Fanout delay estimate using MegaLab Interconnect
t_{F20+}	Fanout delay estimate using FastTrack Interconnect

Note to Table 36:

- (1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 37. APEX 20KE Functional Timing Microparameters

Symbol	Parameter
TCH	Minimum clock high time from clock pin
TCL	Minimum clock low time from clock pin
TCLRP	LE clear Pulse Width
TPREP	LE preset pulse width
TESBCH	Clock high time for ESB
TESBCL	Clock low time for ESB
TESBWP	Write pulse width
TESBRP	Read pulse width

Tables 38 and 39 describe the APEX 20KE external timing parameters.

Table 38. APEX 20KE External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF

Table 39. APEX 20KE External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
t_{INHBDIR}	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{\text{OUTCOBDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
t_{XZBDIR}	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
t_{ZXBIDIR}	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{\text{INSUBIDIRPLL}}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{\text{INHBDIRPLL}}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{\text{OUTCOBDIRPLL}}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{\text{XZBDIRPLL}}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{\text{ZXBIDIRPLL}}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

Note to Tables 38 and 39:

(1) These timing parameters are sample-tested only.

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
t_{ESBWESU}	3.3		3.9		4.6		ns
$t_{\text{ESBDATASU}}$	2.2		2.7		3.1		ns
t_{ESBDATAH}	0.6		0.8		0.9		ns
$t_{\text{ESBADDRSU}}$	2.4		2.9		3.3		ns
$t_{\text{ESBDATACO1}}$		1.3		1.6		1.8	ns
$t_{\text{ESBDATACO2}}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
t_{PTERMSU}	2.3		2.6		3.2		ns
t_{PTERMCO}		1.5		1.8		2.1	ns
$t_{\text{F1-4}}$		0.5		0.6		0.7	ns
$t_{\text{F5-20}}$		1.6		1.7		1.8	ns
$t_{\text{F20+}}$		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU} (1)	2.3		2.8		3.2		ns
t _{INH} (1)	0.0		0.0		0.0		ns
t _{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t _{INSU} (2)	1.1		1.2		—		ns
t _{INH} (2)	0.0		0.0		—		ns
t _{OUTCO} (2)	0.5	2.7	0.5	3.1	—	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR} (1)	2.3		2.8		3.2		ns
t _{INHBIDIR} (1)	0.0		0.0		0.0		ns
t _{OUTCOBIDIR} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t _{XZBIDIR} (1)		5.0		5.9		6.9	ns
t _{ZXBIDIR} (1)		5.0		5.9		6.9	ns
t _{INSUBIDIR} (2)	1.0		1.2		—		ns
t _{INHBIDIR} (2)	0.0		0.0		—		ns
t _{OUTCOBIDIR} (2)	0.5	2.7	0.5	3.1	—	—	ns
t _{XZBIDIR} (2)		4.3		5.0		—	ns
t _{ZXBIDIR} (2)		4.3		5.0		—	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU} (1)	1.9		2.3		2.6		ns
t _{INH} (1)	0.0		0.0		0.0		ns
t _{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t _{INSU} (2)	1.1		1.2		—		ns
t _{INH} (2)	0.0		0.0		—		ns
t _{OUTCO} (2)	0.5	2.7	0.5	3.1	—	—	ns

Table 94. EP20K600E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	2.00		2.50		2.75		ns
t _{CL}	2.00		2.50		2.75		ns
t _{CLRP}	0.18		0.26		0.34		ns
t _{PREP}	0.18		0.26		0.34		ns
t _{ESBCH}	2.00		2.50		2.75		ns
t _{ESBCL}	2.00		2.50		2.75		ns
t _{ESBWP}	1.17		1.68		2.18		ns
t _{ESBRP}	0.95		1.35		1.76		ns

Table 95. EP20K600E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.74		2.74		2.87		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.51	2.00	6.06	2.00	6.61	ns
t _{INSUPLL}	1.86		1.96		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.62	0.50	2.91	-	-	ns

Table 96. EP20K600E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	0.64		0.98		1.08		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	5.51	2.00	6.06	2.00	6.61	ns
t _{XZBIDIR}		6.10		6.74		7.10	ns
t _{ZXBIDIR}		6.10		6.74		7.10	ns
t _{INSUBIDIRPLL}	2.26		2.68		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.62	0.50	2.91	-	-	ns
t _{XZBIDIRPLL}		3.21		3.59		-	ns
t _{ZXBIDIRPLL}		3.21		3.59		-	ns

Tables 97 through 102 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

Table 97. EP20K1000E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_H	0.25		0.25		0.25		ns
t_{CO}		0.28		0.32		0.33	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.25		1.43		1.67		ns
t _{CL}	1.25		1.43		1.67		ns
t _{CLRP}	0.20		0.20		0.20		ns
t _{PREP}	0.20		0.20		0.20		ns
t _{ESBCH}	1.25		1.43		1.67		ns
t _{ESBCL}	1.25		1.43		1.67		ns
t _{ESBWP}	1.28		1.51		1.65		ns
t _{ESBRP}	1.11		1.29		1.41		ns

Table 107. EP20K1500E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	3.09		3.30		3.58		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	6.18	2.00	6.81	2.00	7.36	ns
t _{INSUPLL}	1.94		2.08		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.67	0.50	2.99	-	-	ns