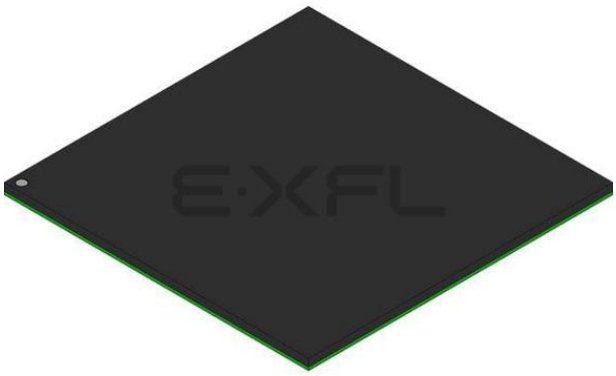
# Altera - EP20K100EBC356-2 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

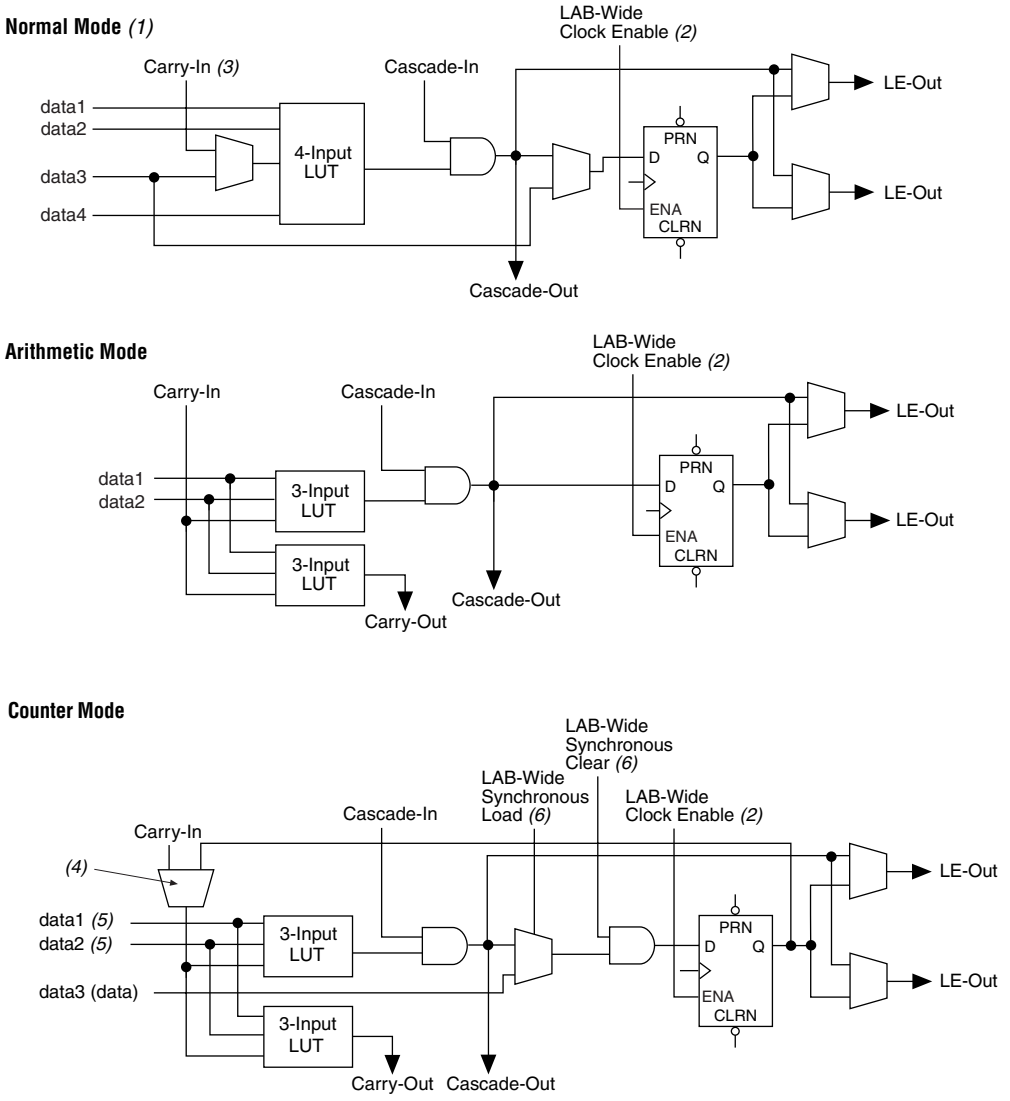
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 416 |
| Number of Logic Elements/Cells | 4160 |
| Total RAM Bits | 53248 |
| Number of I/O | 246 |
| Number of Gates | 263000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 356-LBGA |
| Supplier Device Package | 356-BGA (35x35) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k100ebc356-2 |

*Figure 8. APEX 20K LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

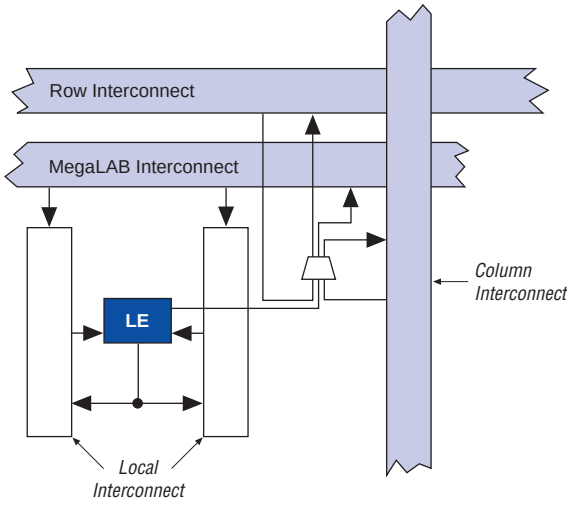
The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

*Figure 11. Driving the FastTrack Interconnect*




APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABS in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

*Table 10. APEX 20K Programmable Delay Chains*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input pin to core delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input register |
| Core to output register delay | Decrease input delay to output register |
| Output register $t_{CO}$ delay | Increase delay to output pin |

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

## MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V $V_{CCINT}$ level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

*Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support*

| $V_{CCIO}$ (V) | Input Signals (V) | | | Output Signals (V) | | |
|---|---|---|---|---|---|---|
| | 2.5 | 3.3 | 5.0 | 2.5 | 3.3 | 5.0 |
| 2.5 | ✓ | ✓(1) | ✓(1) | ✓ | | |
| 3.3 | ✓ | ✓ | ✓(1) | ✓(2) | ✓ | ✓ |

*Notes to Table 12:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$.

(2) When $V_{CCIO}$ = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

*Table 18. APEX 20KE Clock Input & Output Parameters (Part 2 of 2)* Note (1)

| Symbol | Parameter | I/O Standard | -1X Speed Grade | | -2X Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{IN}$ | Input clock frequency | 3.3-V LVTTL | 1.5 | 290 | 1.5 | 257 | MHz |
| | | 2.5-V LVTTL | 1.5 | 281 | 1.5 | 250 | MHz |
| | | 1.8-V LVTTL | 1.5 | 272 | 1.5 | 243 | MHz |
| | | GTL+ | 1.5 | 303 | 1.5 | 261 | MHz |
| | | SSTL-2 Class I | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-2 Class II | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-3 Class I | 1.5 | 300 | 1.5 | 260 | MHz |
| | | SSTL-3 Class II | 1.5 | 300 | 1.5 | 260 | MHz |
| | | LVDS | 1.5 | 420 | 1.5 | 350 | MHz |

*Notes to Tables 17 and 18:*

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ð $f_{VCO}$ ð 840 MHz for LVDS mode.

## SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

*Table 20. APEX 20K Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K30E | 420 |
| EP20K60E | 624 |
| EP20K100 | 786 |
| EP20K100E | 774 |
| EP20K160E | 984 |
| EP20K200 | 1,176 |
| EP20K200E | 1,164 |
| EP20K300E | 1,266 |
| EP20K400 | 1,536 |
| EP20K400E | 1,506 |
| EP20K600E | 1,806 |
| EP20K1000E | 2,190 |
| EP20K1500E | 1 *(1)* |

***Note to Table 20:***
(1) This device does not support JTAG boundary scan testing.

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

*Table 22. APEX 20K JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

*Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions* *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4), (5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3), (6)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(9)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 1.7 | | | V |

| Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 2 of 2) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB macrocell register clock-to-output delay |
| $t_{F1-4}$ | Fanout delay using local interconnect |
| $t_{F5-20}$ | Fanout delay using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay using FastTrack Interconnect |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 32 and 33 describe APEX 20K external timing parameters.

| Table 32. APEX 20K External Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Clock Parameter** |
| $t_{INSU}$ | Setup time with global clock at IOE register |
| $t_{INH}$ | Hold time with global clock at IOE register |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register |

| Table 33. APEX 20K External Bidirectional Timing Parameters *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | C1 = 10 pF |

*Table 41. EP20K200 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.7 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

*Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

*Table 51. EP20K30E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

*Table 64. EP20K100E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{CL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.29 | | 1.53 | | 1.66 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 65. EP20K100E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.23 | | 2.32 | | 2.43 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| $t_{INSUPLL}$ | 1.58 | | 1.66 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |

*Table 66. EP20K100E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.74 | | 2.96 | | 3.19 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| $t_{XZBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| $t_{ZXBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| $t_{INSUBIDIRPLL}$ | 4.64 | | 5.03 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |

*Table 72. EP20K160E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.86 | | 3.24 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{XZBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{ZXBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{INSUBIDIRPLL}$ | 4.93 | | 5.48 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |

Tables 73 through 78 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

*Table 73. EP20K200E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.26 | | 0.31 | | 0.36 | ns |
| $t_{LUT}$ | | 0.70 | | 0.90 | | 1.14 | ns |

*Table 74. EP20K200E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.68 | | 2.06 | | 2.24 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 2.77 | | 3.18 | ns |
| $t_{ESBAWC}$ | | 3.10 | | 3.86 | | 4.50 | ns |
| $t_{ESBSWC}$ | | 2.90 | | 3.67 | | 4.21 | ns |
| $t_{ESBWASU}$ | 0.55 | | 0.67 | | 0.74 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.83 | | 0.95 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.90 | | 2.09 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.42 | | 1.71 | | 2.01 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.06 | | -0.07 | | 0.05 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.13 | | 0.31 | | ns |
| $t_{ESBRADDRSU}$ | 0.18 | | 0.23 | | 0.39 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.35 | | 1.51 | ns |
| $t_{ESBDATACO2}$ | | 2.19 | | 2.75 | | 3.22 | ns |
| $t_{ESBDD}$ | | 2.75 | | 3.41 | | 4.03 | ns |
| $t_{PD}$ | | 1.58 | | 1.97 | | 2.33 | ns |
| $t_{PTERMSU}$ | 1.00 | | 1.22 | | 1.51 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.37 | | 1.09 | ns |

*Table 75. EP20K200E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.02 | | 1.20 | | 1.41 | ns |
| $t_{F20+}$ | | 1.99 | | 2.23 | | 2.53 | ns |

*Table 98. EP20K1000E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.78 | | 2.02 | | 1.95 | ns |
| $t_{ESBSRC}$ | | 2.52 | | 2.91 | | 3.14 | ns |
| $t_{ESBAWC}$ | | 3.52 | | 4.11 | | 4.40 | ns |
| $t_{ESBSWC}$ | | 3.23 | | 3.84 | | 4.16 | ns |
| $t_{ESBWASU}$ | 0.62 | | 0.67 | | 0.61 | | ns |
| $t_{ESBWAH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.77 | | 0.79 | | 0.81 | | ns |
| $t_{ESBWDH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.74 | | 1.92 | | 1.85 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.01 | | 0.23 | | ns |
| $t_{ESBWESU}$ | 2.07 | | 2.28 | | 2.41 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.25 | | 0.27 | | 0.29 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.04 | | 0.11 | | ns |
| $t_{ESBRADDRSU}$ | 0.14 | | 0.11 | | 0.16 | | ns |
| $t_{ESBDATACO1}$ | | 1.29 | | 1.50 | | 1.63 | ns |
| $t_{ESBDATACO2}$ | | 2.55 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.12 | | 3.57 | | 3.85 | ns |
| $t_{PD}$ | | 1.84 | | 2.13 | | 2.32 | ns |
| $t_{PTERMSU}$ | 1.08 | | 1.19 | | 1.32 | | ns |
| $t_{PTERMCO}$ | | 1.31 | | 1.53 | | 1.66 | ns |

*Table 102. EP20K1000E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 3.22 | | 3.33 | | 3.51 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{XZBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{ZXBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{INSUBIDIRPLL}$ | 3.25 | | 3.26 | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | | | ns |
| $t_{XZBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |
| $t_{ZXBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |

Tables 103 through 108 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

*Table 103. EP20K1500E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

*Table 110. Selectable I/O Standard Output Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.09 | | 0.10 | ns |
| 1.8 V | | 2.49 | | 2.98 | | 3.03 | ns |
| PCI | | –0.03 | | 0.17 | | 0.16 | ns |
| GTL+ | | 0.75 | | 0.75 | | 0.76 | ns |
| SSTL-3 Class I | | 1.39 | | 1.51 | | 1.50 | ns |
| SSTL-3 Class II | | 1.11 | | 1.23 | | 1.23 | ns |
| SSTL-2 Class I | | 1.35 | | 1.48 | | 1.47 | ns |
| SSTL-2 Class II | | 1.00 | | 1.12 | | 1.12 | ns |
| LVDS | | –0.48 | | –0.48 | | –0.48 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

# Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

# Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

## Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to $V_{CCIO}$ by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 111. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, EPC16 configuration devices |
| Passive serial (PS) | MasterBlaster or ByteBlasterMV download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File |

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

## Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$ added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.