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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	246
Number of Gates	263000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k100ebc356-3">https://www.e-xfl.com/product-detail/intel/ep20k100ebc356-3</a>

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock<sup>®</sup> feature reducing clock delay and skew
  - ClockBoost<sup>®</sup> feature providing clock multiplication and division
  - ClockShift<sup>™</sup> programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ( $t_{CO} + t_{SU}$ ) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - Programmable clamp to  $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack<sup>®</sup> Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
  - FineLine BGA<sup>®</sup> packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera<sup>®</sup> Quartus<sup>®</sup> II development system for

**Table 5. APEX 20K FineLine BGA Package Options & I/O Count** *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

**Notes to Tables 4 and 5:**

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

**Table 6. APEX 20K QFP, BGA & PGA Package Sizes**

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	—
Area (mm <sup>2</sup> )	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

**Table 7. APEX 20K FineLine BGA Package Sizes**

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm <sup>2</sup> )	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

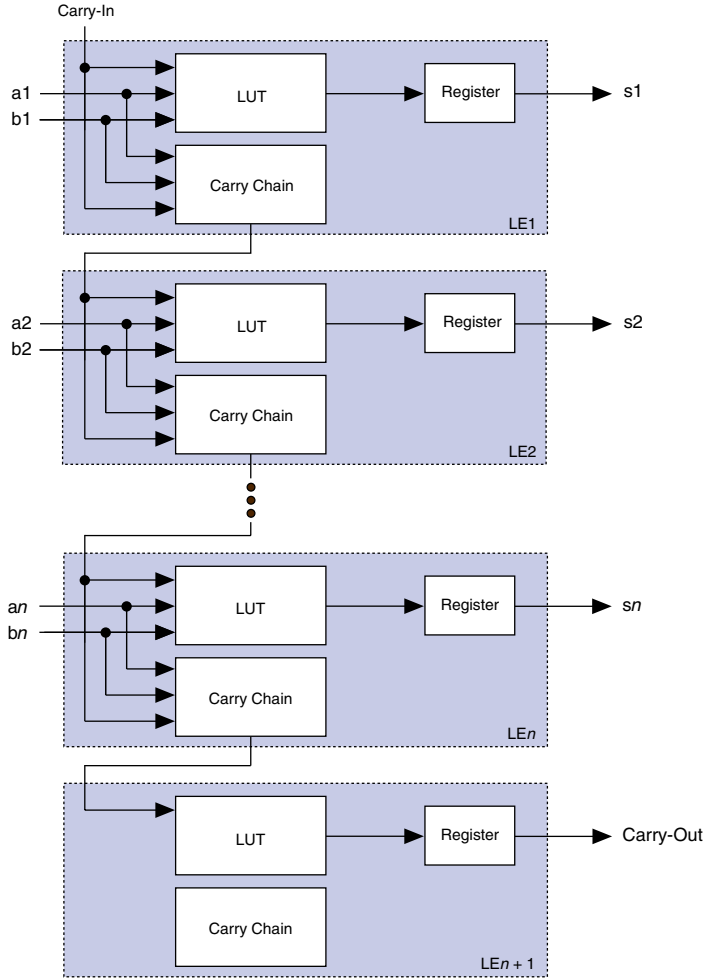
APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

Figure 6. APEX 20K Carry Chain



The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV\_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## **FastTrack Interconnect**

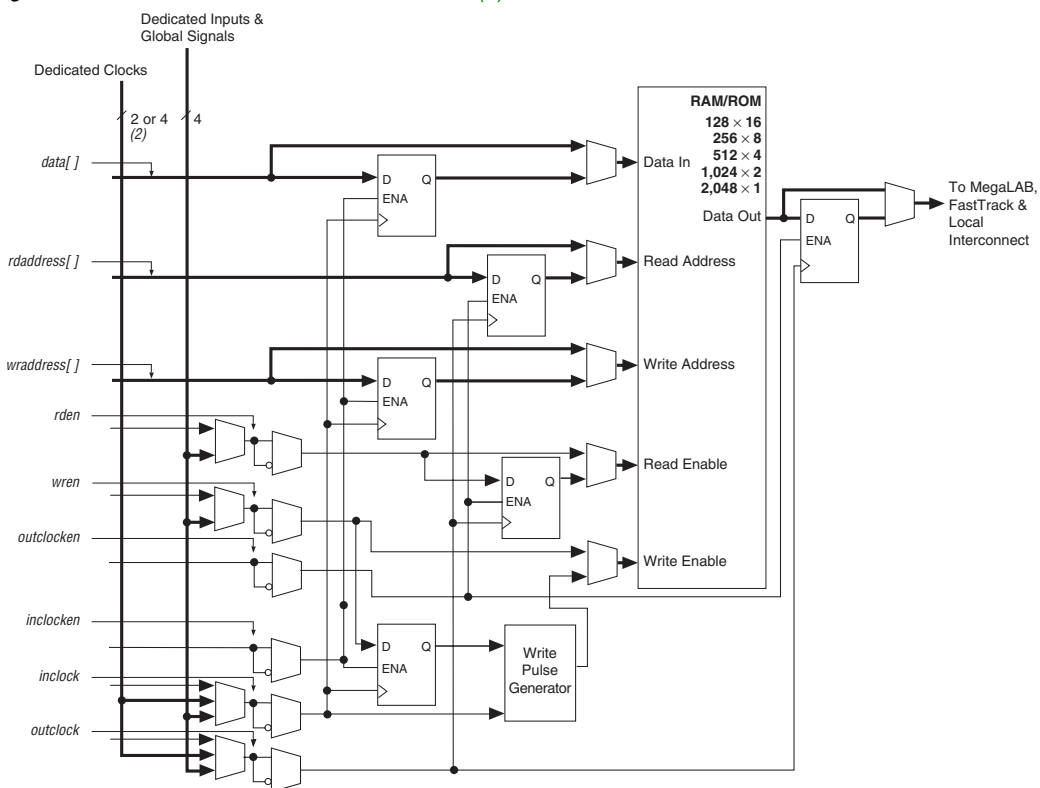
In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).

## Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

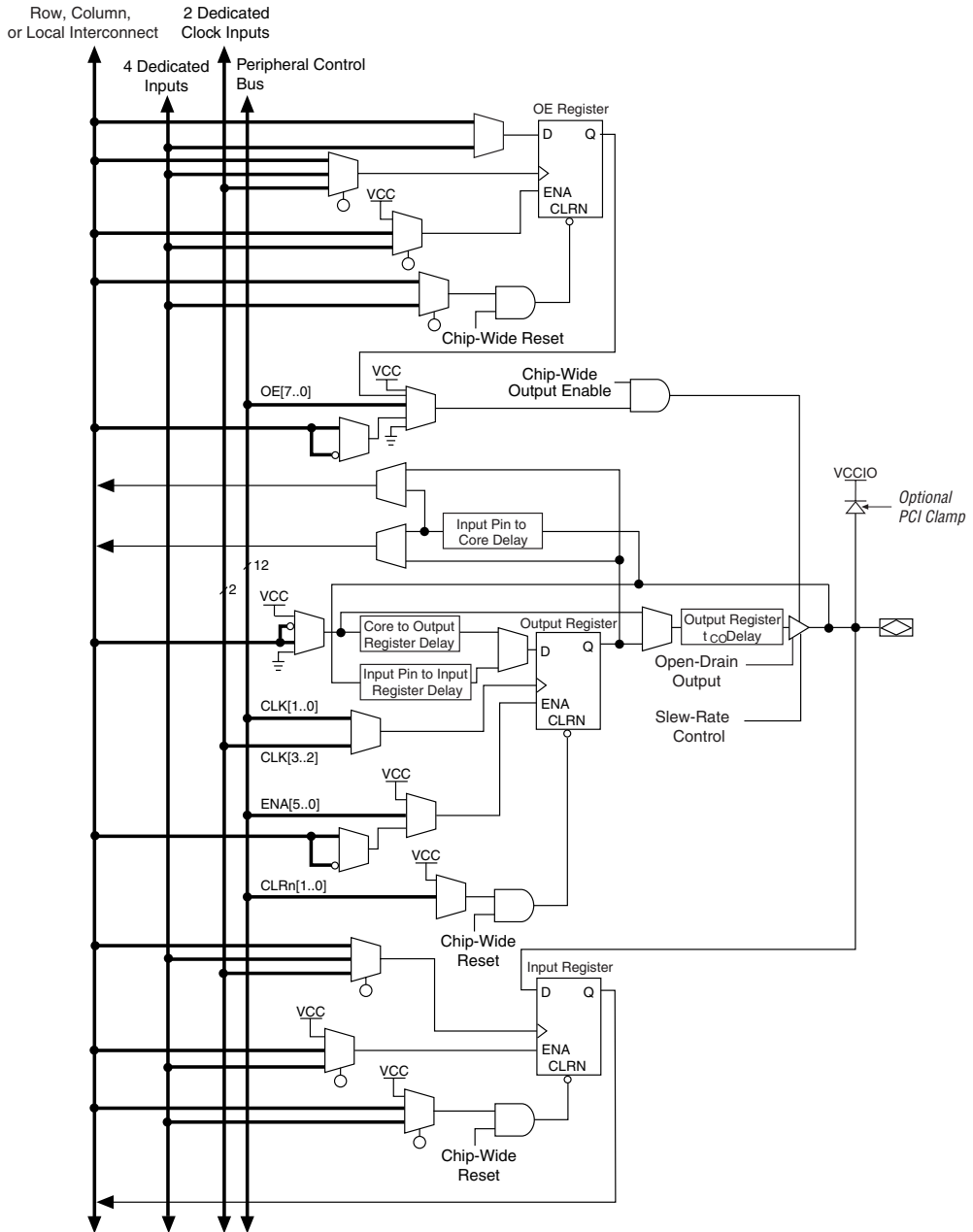
**Figure 20. ESB in Read/Write Clock Mode** *Note (1)*



### Notes to Figure 20:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

**Figure 25. APEX 20K Bidirectional I/O Registers** *Note (1)*



**Note to Figure 25:**

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.



## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.



For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate  $V_{REF}$  level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. [Figure 29](#) shows the arrangement of the APEX 20KE I/O banks.

**Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}$ (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
$f_{CLOCK0}$	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
$f_{CLOCK1}$	clock1 PLL output frequency for internal use		20	335	20	200	MHz
$f_{CLOCK0\_EXT}$	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
$f_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. [Tables 20 and 21](#) show the boundary-scan register length and device IDCODE information for APEX 20K devices.

**Table 20. APEX 20K Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 <a href="#">(1)</a>

**Note to [Table 20](#):**

- (1) This device does not support JTAG boundary scan testing.



For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

**Table 30. APEX 20KE Device Capacitance** Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 27 through 30:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than  $100\text{ mA}$ . The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to  $100\%$  duty cycle.

$V_{IN}$	Max. Duty Cycle
$4.0\text{ V}$	$100\%$ (DC)
$4.1$	$90\%$
$4.2$	$50\%$
$4.3$	$30\%$
$4.4$	$17\%$
$4.5$	$10\%$
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 1.8\text{ V}$ , and  $V_{CCIO} = 1.8\text{ V}$ ,  $2.5\text{ V}$  or  $3.3\text{ V}$ .
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ , and  $I_I$  parameters when  $V_{CCIO} = 1.8\text{ V}$ .
- (10) The APEX 20KE input buffers are compatible with  $1.8\text{-V}$ ,  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVCMOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for  $3.3\text{-V}$  PCI compliance on APEX 20K devices.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the  $f_{MAX}$  timing model for APEX 20K devices.

**Figure 36. APEX 20K  $t_{MAX}$  Timing Model**

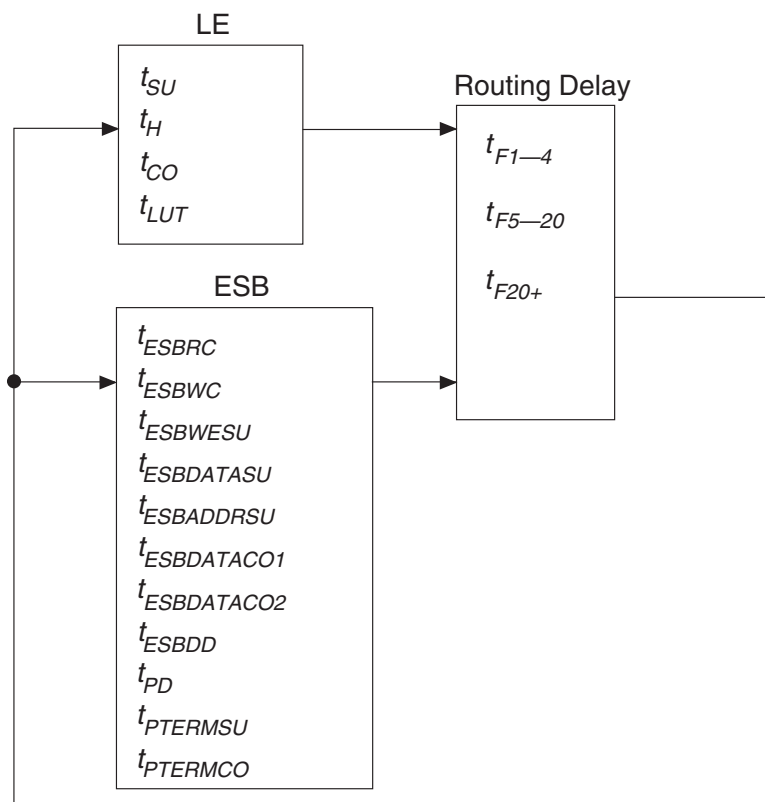


Figure 37 shows the  $f_{MAX}$  timing model for APEX 20KE devices. These parameters can be used to estimate  $f_{MAX}$  for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Tables 40 through 42 show the  $f_{\text{MAX}}$  timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 40. EP20K100  $f_{\text{MAX}}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.5		0.6		0.8		ns
$t_{\text{H}}$	0.7		0.8		1.0		ns
$t_{\text{CO}}$		0.3		0.4		0.5	ns
$t_{\text{LUT}}$		0.8		1.0		1.3	ns
$t_{\text{ESBRC}}$		1.7		2.1		2.4	ns
$t_{\text{ESBWC}}$		5.7		6.9		8.1	ns
$t_{\text{ESBWESU}}$	3.3		3.9		4.6		ns
$t_{\text{ESBDATASU}}$	2.2		2.7		3.1		ns
$t_{\text{ESBDATAH}}$	0.6		0.8		0.9		ns
$t_{\text{ESBADDRSU}}$	2.4		2.9		3.3		ns
$t_{\text{ESBDATACO1}}$		1.3		1.6		1.8	ns
$t_{\text{ESBDATACO2}}$		2.6		3.1		3.6	ns
$t_{\text{ESBDD}}$		2.5		3.3		3.6	ns
$t_{\text{PD}}$		2.5		3.0		3.6	ns
$t_{\text{PTERMSU}}$	2.3		2.6		3.2		ns
$t_{\text{PTERMCO}}$		1.5		1.8		2.1	ns
$t_{\text{F1-4}}$		0.5		0.6		0.7	ns
$t_{\text{F5-20}}$		1.6		1.7		1.8	ns
$t_{\text{F20+}}$		2.2		2.2		2.3	ns
$t_{\text{CH}}$	2.0		2.5		3.0		ns
$t_{\text{CL}}$	2.0		2.5		3.0		ns
$t_{\text{CLRP}}$	0.3		0.4		0.4		ns
$t_{\text{PREP}}$	0.5		0.5		0.5		ns
$t_{\text{ESBCH}}$	2.0		2.5		3.0		ns
$t_{\text{ESBCL}}$	2.0		2.5		3.0		ns
$t_{\text{ESBWP}}$	1.6		1.9		2.2		ns
$t_{\text{ESBRP}}$	1.0		1.3		1.4		ns

**Table 50. EP20K30E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		2.03		2.86		4.24	ns
$t_{ESBSRC}$		2.58		3.49		5.02	ns
$t_{ESBAWC}$		3.88		5.45		8.08	ns
$t_{ESBSWC}$		4.08		5.35		7.48	ns
$t_{ESBWASU}$	1.77		2.49		3.68		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.95		2.74		4.05		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.96		2.75		4.07		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.80		2.73		4.28		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.48		1.17		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.30		0.80		1.64		ns
$t_{ESBRADDRSU}$	0.37		0.90		1.78		ns
$t_{ESBDATACO1}$		1.11		1.32		1.67	ns
$t_{ESBDATACO2}$		2.65		3.73		5.53	ns
$t_{ESBDD}$		3.88		5.45		8.08	ns
$t_{PD}$		1.91		2.69		3.98	ns
$t_{PTERMSU}$	1.04		1.71		2.82		ns
$t_{PTERMCO}$		1.13		1.34		1.69	ns

**Table 51. EP20K30E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.27		0.31	ns
$t_{F5-20}$		1.03		1.14		1.30	ns
$t_{F20+}$		1.42		1.54		1.77	ns

Tables 67 through 72 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

**Table 67. EP20K160E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.22		0.24		0.26		ns
$t_H$	0.22		0.24		0.26		ns
$t_{CO}$		0.25		0.31		0.35	ns
$t_{LUT}$		0.69		0.88		1.12	ns



**Table 69. EP20K160E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.26		0.28	ns
$t_{F5-20}$		1.00		1.18		1.35	ns
$t_{F20+}$		1.95		2.19		2.30	ns

**Table 70. EP20K160E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.34		1.43		1.55		ns
$t_{CL}$	1.34		1.43		1.55		ns
$t_{CLRP}$	0.18		0.19		0.21		ns
$t_{PREP}$	0.18		0.19		0.21		ns
$t_{ESBCH}$	1.34		1.43		1.55		ns
$t_{ESBCL}$	1.34		1.43		1.55		ns
$t_{ESBWP}$	1.15		1.45		1.73		ns
$t_{ESBRP}$	0.93		1.15		1.38		ns

**Table 71. EP20K160E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.23		2.34		2.47		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{INSUPLL}$	2.12		2.07		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.00	0.50	3.35	-	-	ns

**Table 86. EP20K400E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		1.91		1.99	ns
$t_{ESBSRC}$		2.30		2.66		2.93	ns
$t_{ESBAWC}$		3.09		3.58		3.99	ns
$t_{ESBSWC}$		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
$t_{ESBWAH}$	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
$t_{ESBWDH}$	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
$t_{ESBDD}$		2.73		3.17		3.58	ns
$t_{PD}$		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

**Table 110. Selectable I/O Standard Output Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		−0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		−0.48		−0.48		−0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

## Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at <http://www.altera.com>.

## Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to  $V_{CCIO}$  by a built-in weak pull-up resistor.

## Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

### Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

### Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for  $t_{ESB\text{DATAH}}$  parameter.

### Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

### Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$  added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).