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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

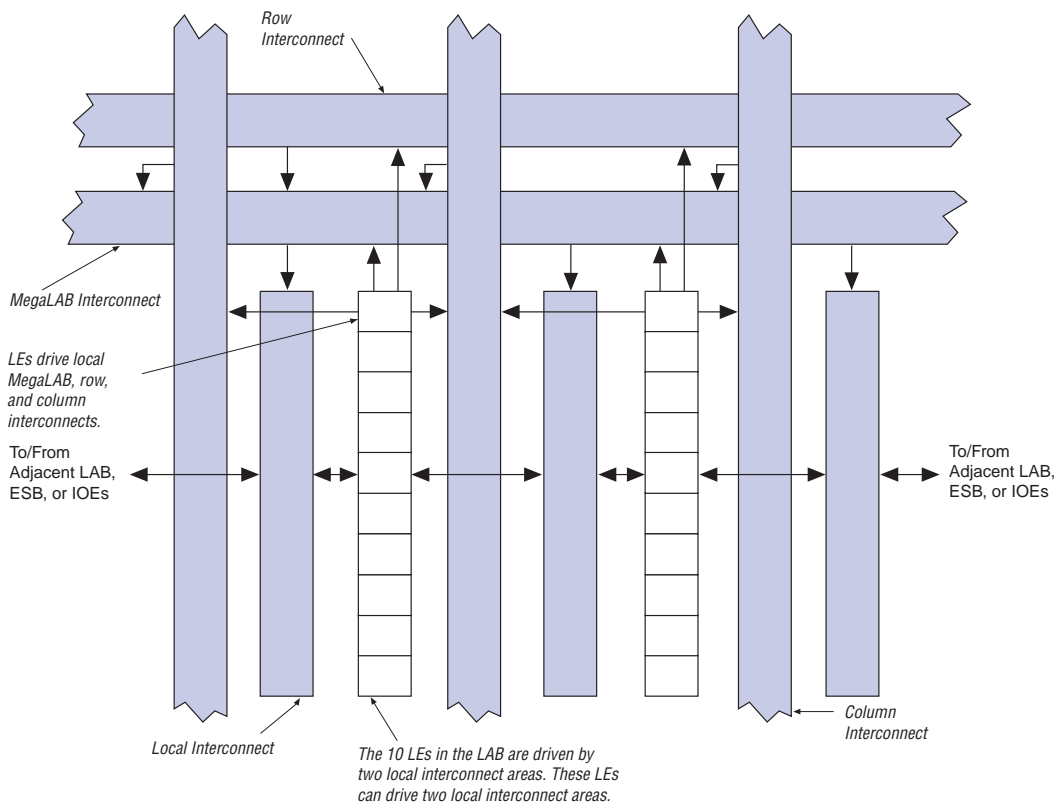
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	246
Number of Gates	263000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	324-BGA
Supplier Device Package	324-FBGA (19x19)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k100efc324-1x">https://www.e-xfl.com/product-detail/intel/ep20k100efc324-1x</a>

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 3. LAB Structure**



### *LE Operating Modes*

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV\_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

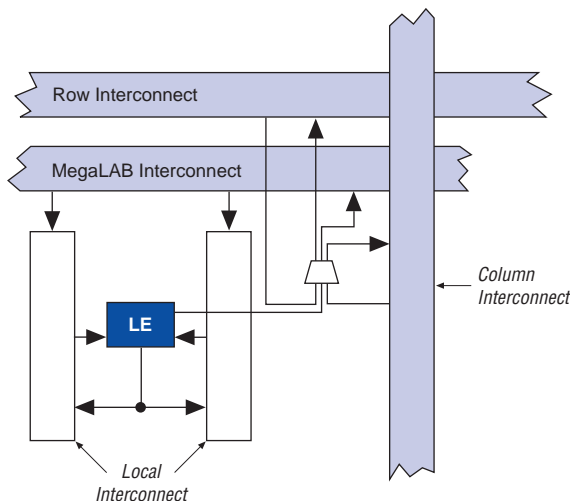
## **FastTrack Interconnect**

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

**Figure 11. Driving the FastTrack Interconnect**



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABs in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

## Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

## Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

<b>Table 10. APEX 20K Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register $t_{CO}$ delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.



**Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}$ (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
$f_{CLOCK0}$	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
$f_{CLOCK1}$	clock1 PLL output frequency for internal use		20	335	20	200	MHz
$f_{CLOCK0\_EXT}$	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
$f_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

<b>Table 22. APEX 20K JTAG Timing Parameters &amp; Values</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.



For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

**Table 30. APEX 20KE Device Capacitance** Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 27 through 30:**

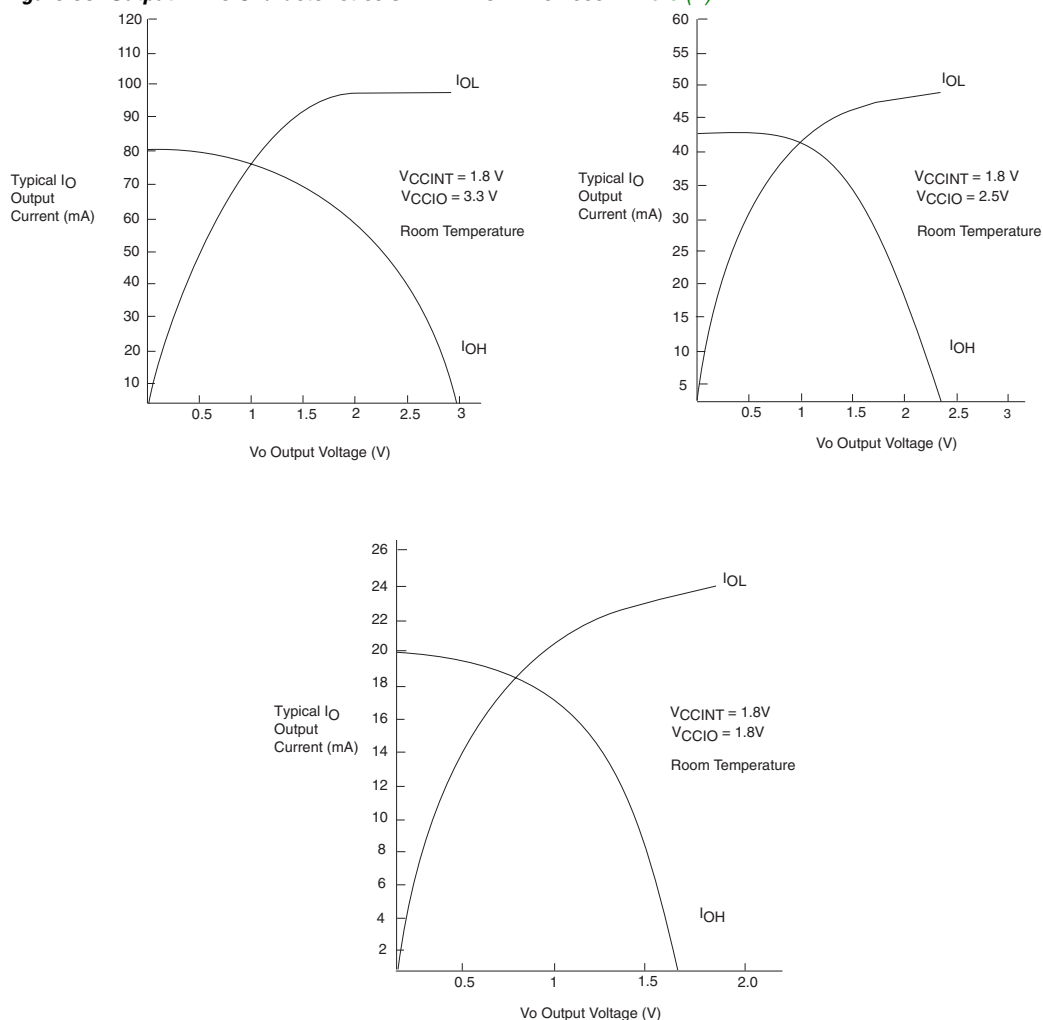
- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than  $100\text{ mA}$ . The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to  $100\%$  duty cycle.

$V_{IN}$	Max. Duty Cycle
$4.0\text{ V}$	$100\%$ (DC)
$4.1$	$90\%$
$4.2$	$50\%$
$4.3$	$30\%$
$4.4$	$17\%$
$4.5$	$10\%$
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 1.8\text{ V}$ , and  $V_{CCIO} = 1.8\text{ V}$ ,  $2.5\text{ V}$  or  $3.3\text{ V}$ .
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ , and  $I_I$  parameters when  $V_{CCIO} = 1.8\text{ V}$ .
- (10) The APEX 20KE input buffers are compatible with  $1.8\text{-V}$ ,  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVCMOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for  $3.3\text{-V}$  PCI compliance on APEX 20K devices.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

**Figure 35. Output Drive Characteristics of APEX 20KE Devices** *Note (1)*

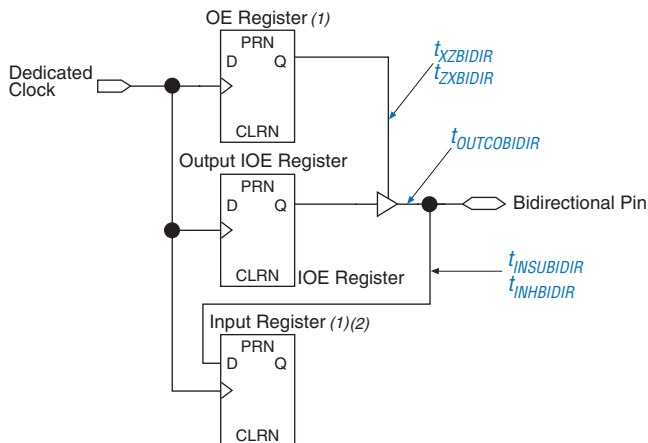


**Note to Figure 35:**

(1) These are transient (AC) currents.

## Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

**Figure 40. Synchronous Bidirectional Pin External Timing****Notes to Figure 40:**

- (1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.
- (2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the  $f_{MAX}$  timing parameters shown in Figure 36 on page 68.

**Table 31. APEX 20K  $f_{MAX}$  Timing Parameters (Part 1 of 2)**

Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LUT delay for data-in
$t_{ESBRC}$	ESB Asynchronous read cycle time
$t_{ESBWC}$	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBADDRSU}$	ESB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers

**Table 43. EP20K100 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub> (1)	2.3		2.8		3.2		ns
t <sub>INH</sub> (1)	0.0		0.0		0.0		ns
t <sub>OUTCO</sub> (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t <sub>INSU</sub> (2)	1.1		1.2		—		ns
t <sub>INH</sub> (2)	0.0		0.0		—		ns
t <sub>OUTCO</sub> (2)	0.5	2.7	0.5	3.1	—	4.8	ns

**Table 44. EP20K100 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub> (1)	2.3		2.8		3.2		ns
t <sub>INHBIDIR</sub> (1)	0.0		0.0		0.0		ns
t <sub>OUTCOBIDIR</sub> (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t <sub>XZBIDIR</sub> (1)		5.0		5.9		6.9	ns
t <sub>ZXBIDIR</sub> (1)		5.0		5.9		6.9	ns
t <sub>INSUBIDIR</sub> (2)	1.0		1.2		—		ns
t <sub>INHBIDIR</sub> (2)	0.0		0.0		—		ns
t <sub>OUTCOBIDIR</sub> (2)	0.5	2.7	0.5	3.1	—	—	ns
t <sub>XZBIDIR</sub> (2)		4.3		5.0		—	ns
t <sub>ZXBIDIR</sub> (2)		4.3		5.0		—	ns

**Table 45. EP20K200 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub> (1)	1.9		2.3		2.6		ns
t <sub>INH</sub> (1)	0.0		0.0		0.0		ns
t <sub>OUTCO</sub> (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t <sub>INSU</sub> (2)	1.1		1.2		—		ns
t <sub>INH</sub> (2)	0.0		0.0		—		ns
t <sub>OUTCO</sub> (2)	0.5	2.7	0.5	3.1	—	—	ns

**Table 46. EP20K200 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.9		2.3		2.6		ns
$t_{\text{INHBIDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{\text{XZBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{ZXBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{INSUBIDIR}} (2)$	1.1		1.2		—		ns
$t_{\text{INHBIDIR}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	2.7	0.5	3.1	—	—	ns
$t_{\text{XZBIDIR}} (2)$		4.3		5.0		—	ns
$t_{\text{ZXBIDIR}} (2)$		4.3		5.0		—	ns

**Table 47. EP20K400 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INH}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{INSU}} (2)$	0.4		1.0		—		ns
$t_{\text{INH}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCO}} (2)$	0.5	3.1	0.5	4.1	—	—	ns

**Table 48. EP20K400 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INHBIDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{XZBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{ZXBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{INSUBIDIR}} (2)$	0.5		1.0		—		ns
$t_{\text{INHBIDIR}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	3.1	0.5	4.1	—	—	ns
$t_{\text{XZBIDIR}} (2)$		6.2		7.6		—	ns
$t_{\text{ZXBIDIR}} (2)$		6.2		7.6		—	ns

**Table 57. EP20K60E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns



**Table 68. EP20K160E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.65		2.02		2.11	ns
$t_{ESBSRC}$		2.21		2.70		3.11	ns
$t_{ESBAWC}$		3.04		3.79		4.42	ns
$t_{ESBSWC}$		2.81		3.56		4.10	ns
$t_{ESBWASU}$	0.54		0.66		0.73		ns
$t_{ESBWAH}$	0.36		0.45		0.47		ns
$t_{ESBWDSU}$	0.68		0.81		0.94		ns
$t_{ESBWDH}$	0.36		0.45		0.47		ns
$t_{ESBRASU}$	1.58		1.87		2.06		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.41		1.71		2.00		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.02		-0.03		0.09		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.14		0.17		0.35		ns
$t_{ESBRADDRSU}$	0.21		0.27		0.43		ns
$t_{ESBDATACO1}$		1.04		1.30		1.46	ns
$t_{ESBDATACO2}$		2.15		2.70		3.16	ns
$t_{ESBDD}$		2.69		3.35		3.97	ns
$t_{PD}$		1.55		1.93		2.29	ns
$t_{PTERMSU}$	1.01		1.23		1.52		ns
$t_{PTERMCO}$		1.06		1.32		1.04	ns

**Table 92. EP20K600E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		2.39		3.11	ns
$t_{ESBSRC}$		2.27		3.07		3.86	ns
$t_{ESBAWC}$		3.19		4.56		5.93	ns
$t_{ESBSWC}$		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATAO1}$		1.01		1.19		1.37	ns
$t_{ESBDATAO2}$		2.18		3.12		4.05	ns
$t_{ESBDD}$		3.19		4.56		5.93	ns
$t_{PD}$		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

**Table 93. EP20K600E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.25		0.26	ns
$t_{F5-20}$		1.26		1.39		1.52	ns
$t_{F20+}$		3.51		3.88		4.26	ns

**Table 102. EP20K1000E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.22		3.33		3.51		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{\text{XZBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{ZXBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.25		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.25	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		2.81		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		2.81		3.80			ns

Tables 103 through 108 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

**Table 103. EP20K1500E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.32		0.33	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns

**Table 106. EP20K1500E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.25		1.43		1.67		ns
t <sub>CL</sub>	1.25		1.43		1.67		ns
t <sub>CLRP</sub>	0.20		0.20		0.20		ns
t <sub>PREP</sub>	0.20		0.20		0.20		ns
t <sub>ESBCH</sub>	1.25		1.43		1.67		ns
t <sub>ESBCL</sub>	1.25		1.43		1.67		ns
t <sub>ESBWP</sub>	1.28		1.51		1.65		ns
t <sub>ESBRP</sub>	1.11		1.29		1.41		ns

**Table 107. EP20K1500E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	3.09		3.30		3.58		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	6.18	2.00	6.81	2.00	7.36	ns
t <sub>INSUPLL</sub>	1.94		2.08		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.67	0.50	2.99	-	-	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 111. Data Sources for Configuration	
Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File



For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information