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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	93
Number of Gates	263000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k100efi144-2n">https://www.e-xfl.com/product-detail/intel/ep20k100efi144-2n</a>

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock<sup>®</sup> feature reducing clock delay and skew
  - ClockBoost<sup>®</sup> feature providing clock multiplication and division
  - ClockShift<sup>™</sup> programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ( $t_{CO} + t_{SU}$ ) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - Programmable clamp to  $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack<sup>®</sup> Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
  - FineLine BGA<sup>®</sup> packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera<sup>®</sup> Quartus<sup>®</sup> II development system for

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP<sup>SM</sup>) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS )

**Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count**    *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

**Table 5. APEX 20K FineLine BGA Package Options & I/O Count** *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

**Notes to Tables 4 and 5:**

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

**Table 6. APEX 20K QFP, BGA & PGA Package Sizes**

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	—
Area (mm <sup>2</sup> )	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

**Table 7. APEX 20K FineLine BGA Package Sizes**

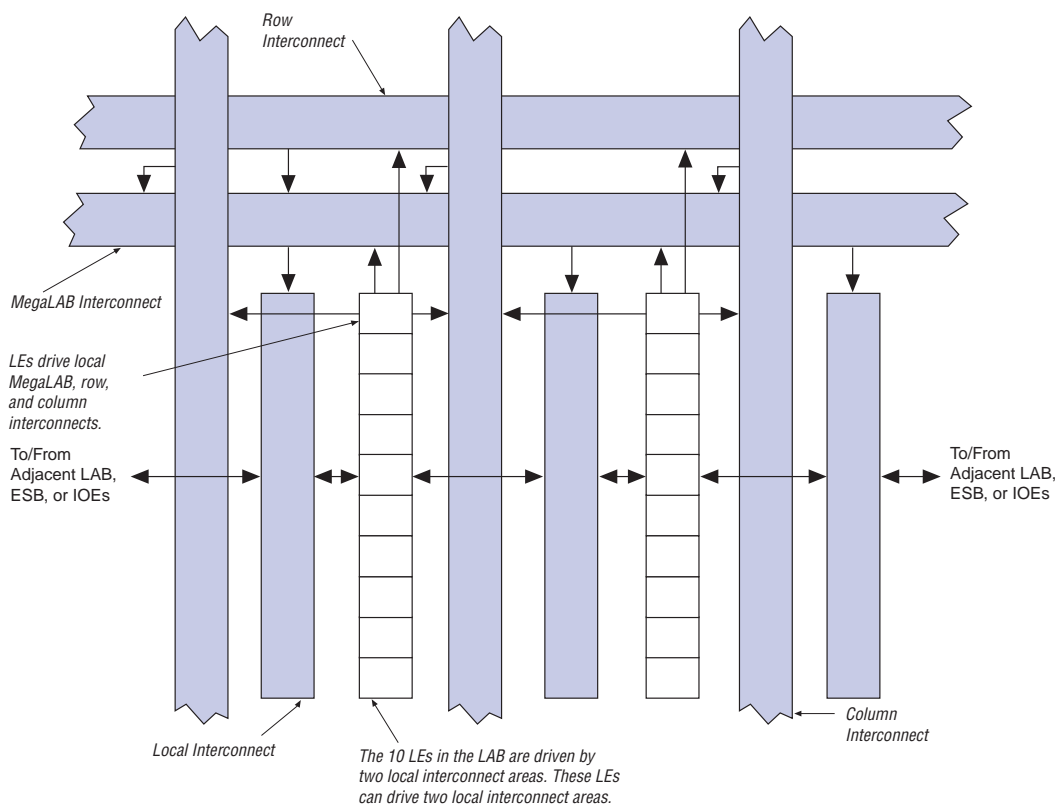
Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm <sup>2</sup> )	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. [Figure 3](#) shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 3. LAB Structure**



Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

### *LE Operating Modes*

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.



Figure 12. APEX 20KE FastRow Interconnect

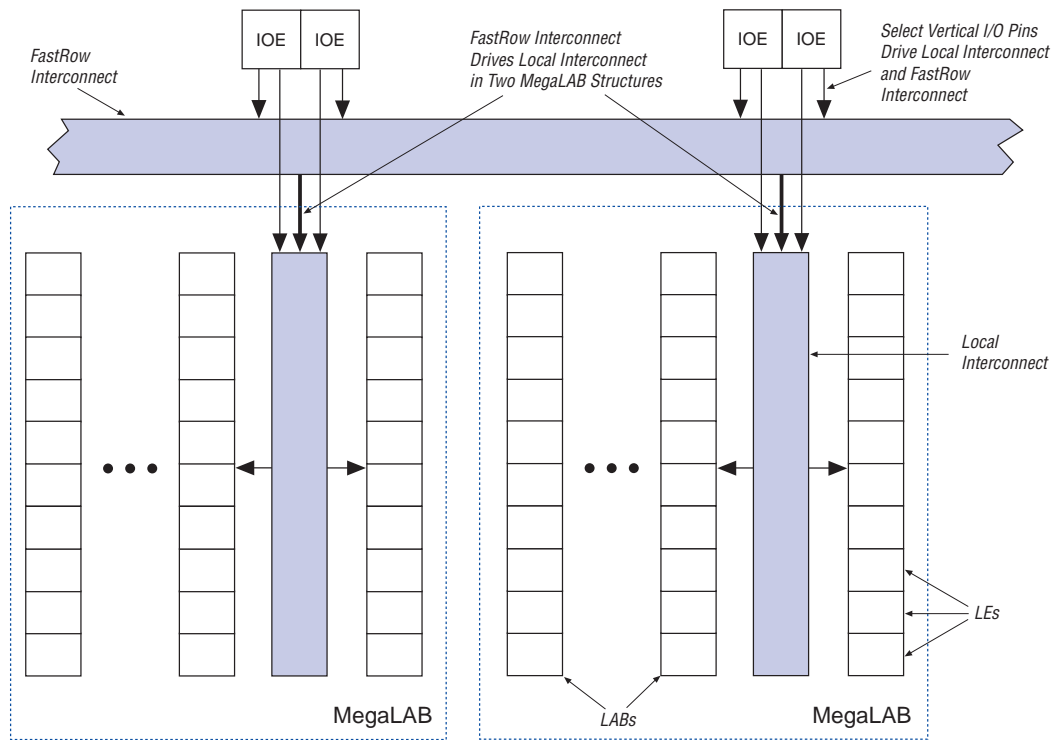
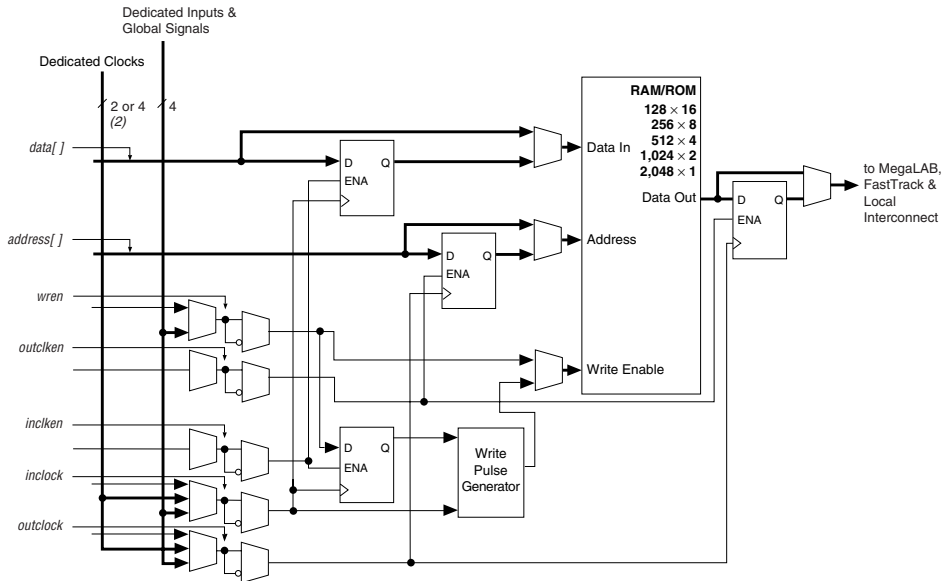


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

Figure 22. ESB in Single-Port Mode *Note (1)*



**Notes to Figure 22:**

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

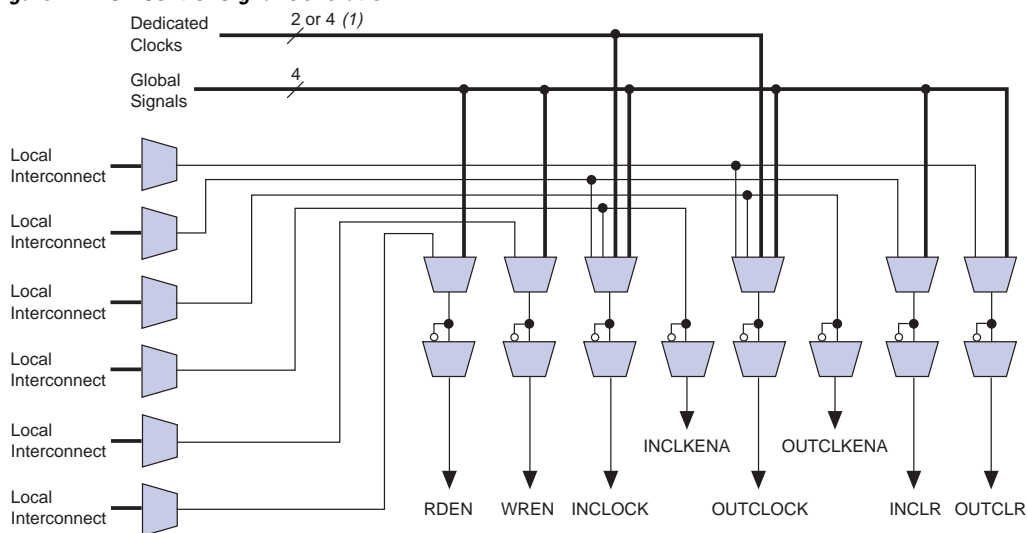


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. [Figure 24](#) shows the ESB control signal generation logic.

**Figure 24. ESB Control Signal Generation**

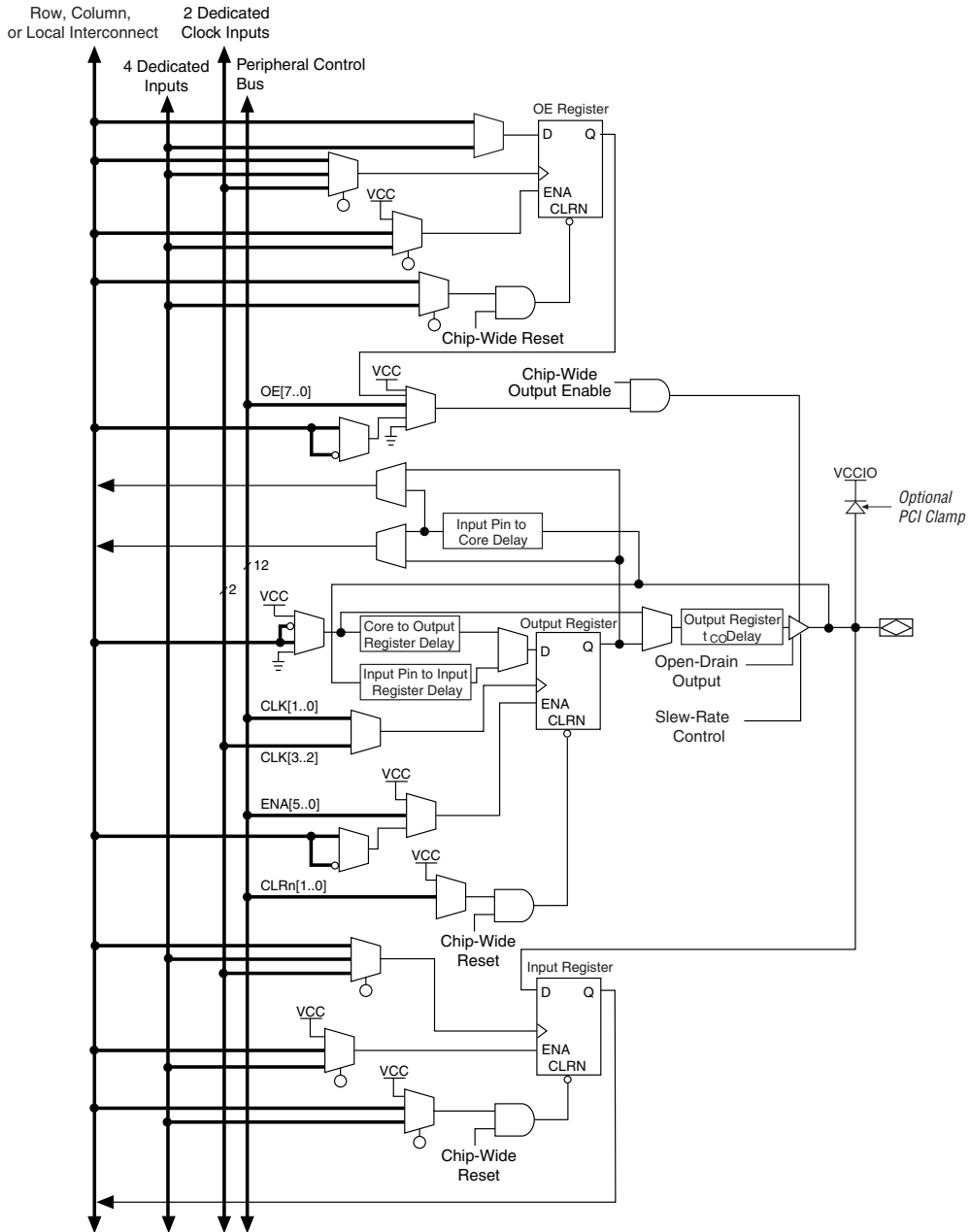


**Note to [Figure 24](#):**

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

**Figure 25. APEX 20K Bidirectional I/O Registers** *Note (1)*



**Note to Figure 25:**

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

**Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}$ (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
$f_{CLOCK0}$	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
$f_{CLOCK1}$	clock1 PLL output frequency for internal use		20	335	20	200	MHz
$f_{CLOCK0\_EXT}$	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
$f_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

Figure 33. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

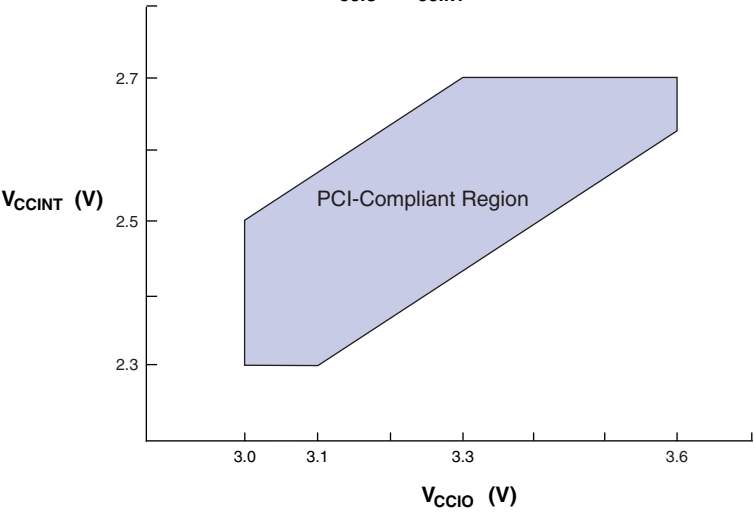
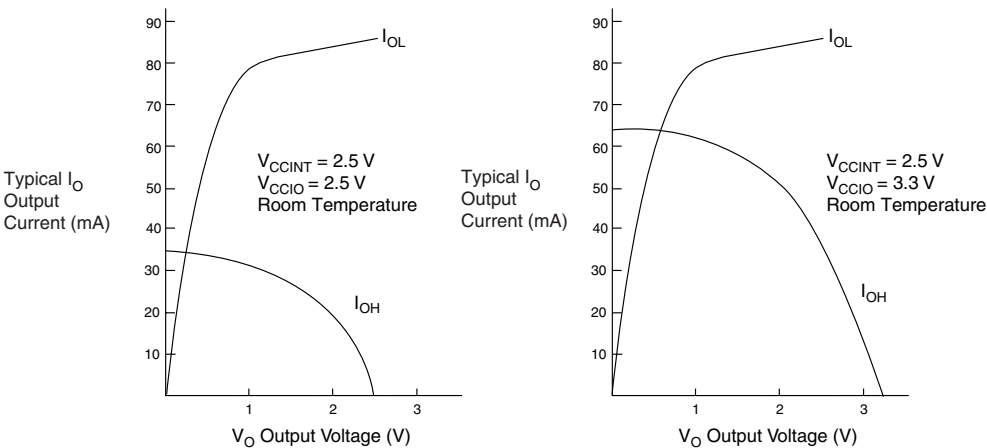


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when  $V_{CCIO}$  pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

Figure 34. Output Drive Characteristics of APEX 20K Device *Note (1)*



*Note to Figure 34:*

(1) These are transient (AC) currents.

**Table 31. APEX 20K  $t_{MAX}$  Timing Parameters (Part 2 of 2)**

Symbol	Parameter
$t_{ESB\text{DATA}CO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
$t_{F1-4}$	Fanout delay using local interconnect
$t_{F5-20}$	Fanout delay using MegaLab Interconnect
$t_{F20+}$	Fanout delay using FastTrack Interconnect
$t_{CH}$	Minimum clock high time from clock pin
$t_{CL}$	Minimum clock low time from clock pin
$t_{CLRP}$	LE clear pulse width
$t_{PREP}$	LE preset pulse width
$t_{ESBCH}$	Clock high time
$t_{ESBCL}$	Clock low time
$t_{ESBWP}$	Write pulse width
$t_{ESBRP}$	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

**Table 32. APEX 20K External Timing Parameters Note (1)**

Symbol	Clock Parameter
$t_{INSU}$	Setup time with global clock at IOE register
$t_{INH}$	Hold time with global clock at IOE register
$t_{OUTCO}$	Clock-to-output delay with global clock at IOE register

**Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)**

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INH\text{BIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCO\text{BIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZ\text{BIDIR}}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{Z\text{BIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF

**Table 43. EP20K100 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub> (1)	2.3		2.8		3.2		ns
t <sub>INH</sub> (1)	0.0		0.0		0.0		ns
t <sub>OUTCO</sub> (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t <sub>INSU</sub> (2)	1.1		1.2		—		ns
t <sub>INH</sub> (2)	0.0		0.0		—		ns
t <sub>OUTCO</sub> (2)	0.5	2.7	0.5	3.1	—	4.8	ns

**Table 44. EP20K100 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub> (1)	2.3		2.8		3.2		ns
t <sub>INHBIDIR</sub> (1)	0.0		0.0		0.0		ns
t <sub>OUTCOBIDIR</sub> (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t <sub>XZBIDIR</sub> (1)		5.0		5.9		6.9	ns
t <sub>ZXBIDIR</sub> (1)		5.0		5.9		6.9	ns
t <sub>INSUBIDIR</sub> (2)	1.0		1.2		—		ns
t <sub>INHBIDIR</sub> (2)	0.0		0.0		—		ns
t <sub>OUTCOBIDIR</sub> (2)	0.5	2.7	0.5	3.1	—	—	ns
t <sub>XZBIDIR</sub> (2)		4.3		5.0		—	ns
t <sub>ZXBIDIR</sub> (2)		4.3		5.0		—	ns

**Table 45. EP20K200 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub> (1)	1.9		2.3		2.6		ns
t <sub>INH</sub> (1)	0.0		0.0		0.0		ns
t <sub>OUTCO</sub> (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t <sub>INSU</sub> (2)	1.1		1.2		—		ns
t <sub>INH</sub> (2)	0.0		0.0		—		ns
t <sub>OUTCO</sub> (2)	0.5	2.7	0.5	3.1	—	—	ns



**Table 46. EP20K200 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$ (1)	1.9		2.3		2.6		ns
$t_{\text{INHBIDIR}}$ (1)	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$ (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{\text{XZBIDIR}}$ (1)		5.0		5.9		6.9	ns
$t_{\text{ZXBIDIR}}$ (1)		5.0		5.9		6.9	ns
$t_{\text{INSUBIDIR}}$ (2)	1.1		1.2		—		ns
$t_{\text{INHBIDIR}}$ (2)	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}}$ (2)	0.5	2.7	0.5	3.1	—	—	ns
$t_{\text{XZBIDIR}}$ (2)		4.3		5.0		—	ns
$t_{\text{ZXBIDIR}}$ (2)		4.3		5.0		—	ns

**Table 47. EP20K400 External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}}$ (1)	1.4		1.8		2.0		ns
$t_{\text{INH}}$ (1)	0.0		0.0		0.0		ns
$t_{\text{OUTCO}}$ (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{INSU}}$ (2)	0.4		1.0		—		ns
$t_{\text{INH}}$ (2)	0.0		0.0		—		ns
$t_{\text{OUTCO}}$ (2)	0.5	3.1	0.5	4.1	—	—	ns

**Table 48. EP20K400 External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$ (1)	1.4		1.8		2.0		ns
$t_{\text{INHBIDIR}}$ (1)	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$ (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{XZBIDIR}}$ (1)		7.3		8.9		10.3	ns
$t_{\text{ZXBIDIR}}$ (1)		7.3		8.9		10.3	ns
$t_{\text{INSUBIDIR}}$ (2)	0.5		1.0		—		ns
$t_{\text{INHBIDIR}}$ (2)	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}}$ (2)	0.5	3.1	0.5	4.1	—	—	ns
$t_{\text{XZBIDIR}}$ (2)		6.2		7.6		—	ns
$t_{\text{ZXBIDIR}}$ (2)		6.2		7.6		—	ns

**Table 80. EP20K300E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.79		2.44		3.25	ns
$t_{ESBSRC}$		2.40		3.12		4.01	ns
$t_{ESBAWC}$		3.41		4.65		6.20	ns
$t_{ESBSWC}$		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
$t_{ESBDD}$		3.41		4.65		6.20	ns
$t_{PD}$		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

**Table 81. EP20K300E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.24		0.26	ns
$t_{F5-20}$		1.33		1.43		1.58	ns
$t_{F20+}$		3.63		3.93		4.35	ns

**Table 102. EP20K1000E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.22		3.33		3.51		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{\text{XZBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{ZXBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.25		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.25	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		2.81		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		2.81		3.80			ns

Tables 103 through 108 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

**Table 103. EP20K1500E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.32		0.33	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 111. Data Sources for Configuration	
Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File



For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information



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