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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	183
Number of Gates	263000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k100eqc240-1x">https://www.e-xfl.com/product-detail/intel/ep20k100eqc240-1x</a>

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock<sup>®</sup> feature reducing clock delay and skew
  - ClockBoost<sup>®</sup> feature providing clock multiplication and division
  - ClockShift<sup>™</sup> programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ( $t_{CO} + t_{SU}$ ) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - Programmable clamp to  $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack<sup>®</sup> Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
  - FineLine BGA<sup>®</sup> packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera<sup>®</sup> Quartus<sup>®</sup> II development system for

**Table 5. APEX 20K FineLine BGA Package Options & I/O Count** *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

**Notes to Tables 4 and 5:**

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

**Table 6. APEX 20K QFP, BGA & PGA Package Sizes**

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	—
Area (mm <sup>2</sup> )	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

**Table 7. APEX 20K FineLine BGA Package Sizes**

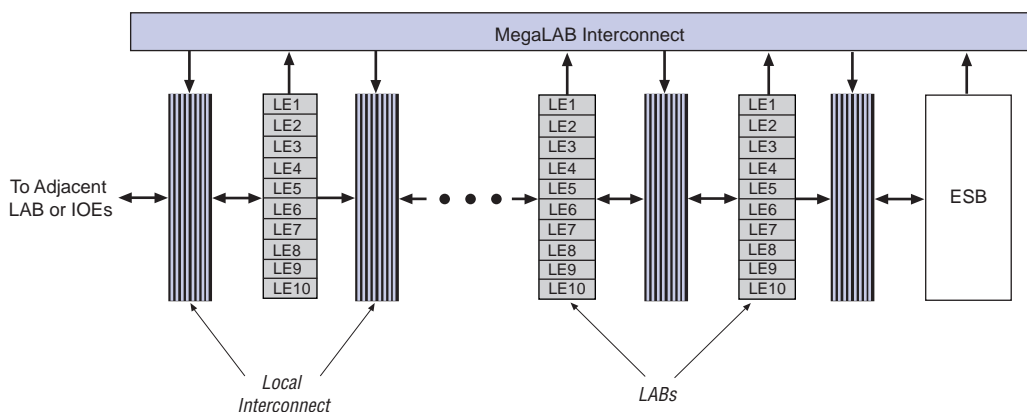
Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm <sup>2</sup> )	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

## MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

**Figure 2. MegaLAB Structure**



### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

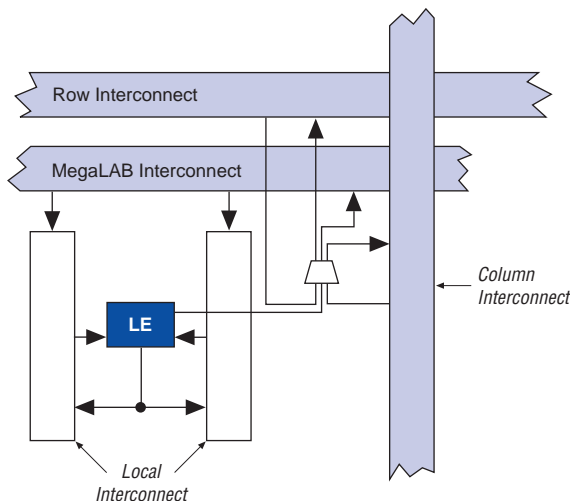
The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

**Figure 11. Driving the FastTrack Interconnect**



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABs in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

**Table 9. APEX 20K Routing Scheme**

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin								✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ (1)				

**Note to Table 9:**

(1) This connection is supported in APEX 20KE devices only.

## Product-Term Logic

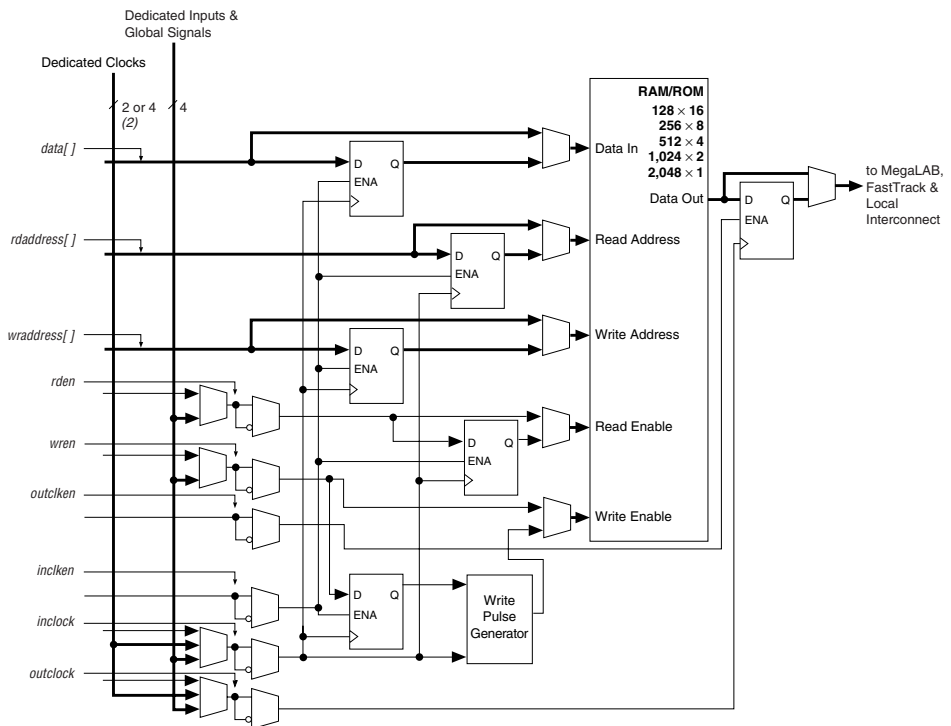
The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

**Figure 21. ESB in Input/Output Clock Mode** Note (1)



### Notes to Figure 21:

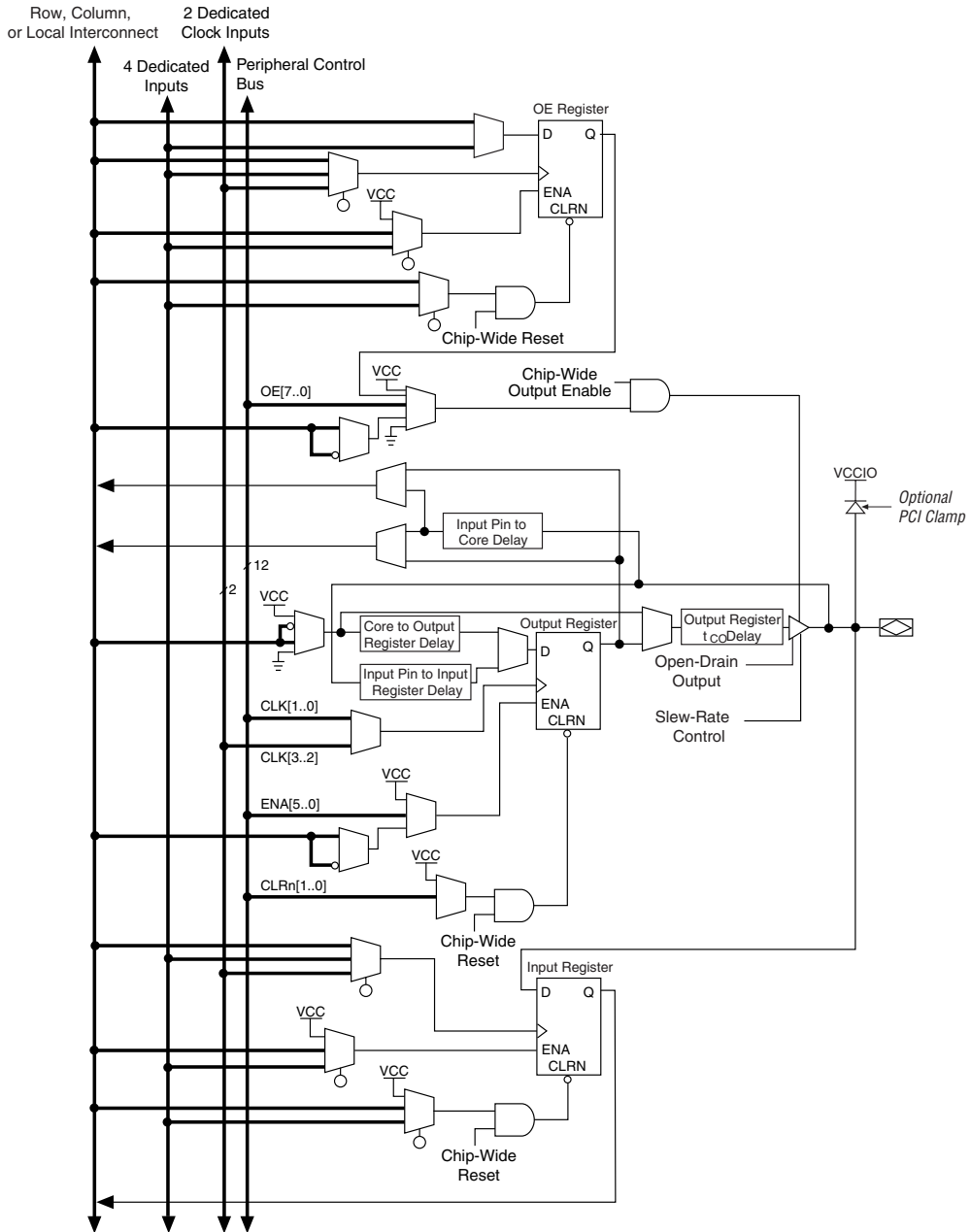
- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

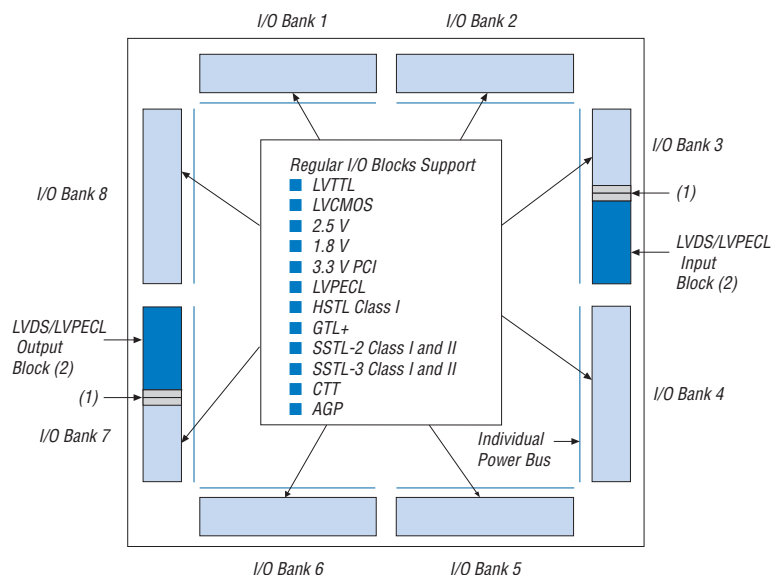


**Figure 25. APEX 20K Bidirectional I/O Registers** *Note (1)*



**Note to Figure 25:**

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

**Figure 29. APEX 20KE I/O Banks**

**Notes to Figure 29:**

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with  $V_{CCIO}$  set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the  $V_{CCIO}$  and  $V_{CCINT}$  power supplies may be powered in any order.



For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

<b>Table 22. APEX 20K JTAG Timing Parameters &amp; Values</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the  $f_{MAX}$  timing model for APEX 20K devices.

**Figure 36. APEX 20K  $t_{MAX}$  Timing Model**

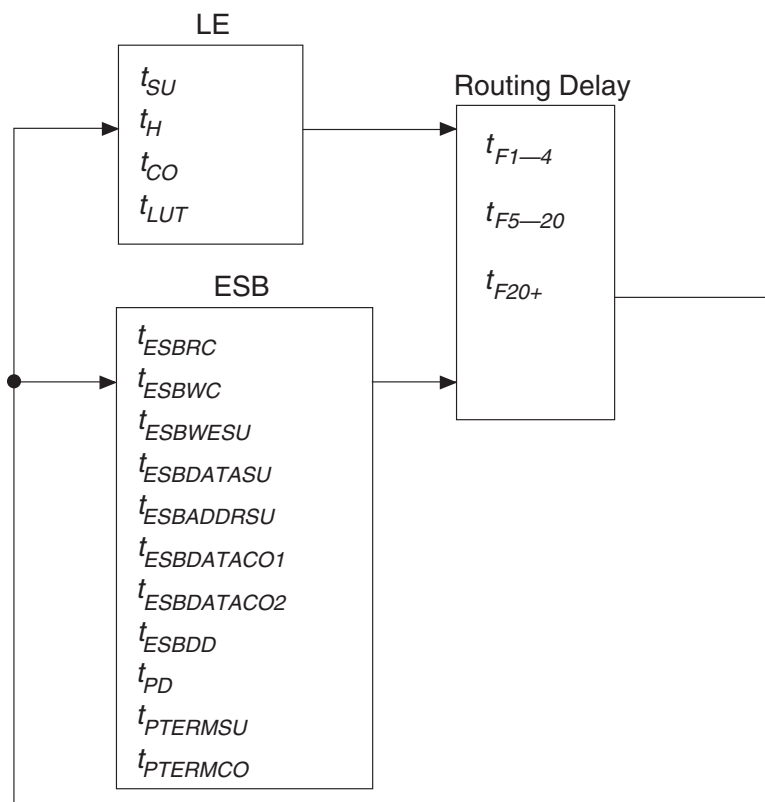


Figure 37 shows the  $f_{MAX}$  timing model for APEX 20KE devices. These parameters can be used to estimate  $f_{MAX}$  for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Tables 40 through 42 show the  $f_{\text{MAX}}$  timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 40. EP20K100  $f_{\text{MAX}}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.5		0.6		0.8		ns
$t_{\text{H}}$	0.7		0.8		1.0		ns
$t_{\text{CO}}$		0.3		0.4		0.5	ns
$t_{\text{LUT}}$		0.8		1.0		1.3	ns
$t_{\text{ESBRC}}$		1.7		2.1		2.4	ns
$t_{\text{ESBWC}}$		5.7		6.9		8.1	ns
$t_{\text{ESBWESU}}$	3.3		3.9		4.6		ns
$t_{\text{ESBDATASU}}$	2.2		2.7		3.1		ns
$t_{\text{ESBDATAH}}$	0.6		0.8		0.9		ns
$t_{\text{ESBADDRSU}}$	2.4		2.9		3.3		ns
$t_{\text{ESBDATACO1}}$		1.3		1.6		1.8	ns
$t_{\text{ESBDATACO2}}$		2.6		3.1		3.6	ns
$t_{\text{ESBDD}}$		2.5		3.3		3.6	ns
$t_{\text{PD}}$		2.5		3.0		3.6	ns
$t_{\text{PTERMSU}}$	2.3		2.6		3.2		ns
$t_{\text{PTERMCO}}$		1.5		1.8		2.1	ns
$t_{\text{F1-4}}$		0.5		0.6		0.7	ns
$t_{\text{F5-20}}$		1.6		1.7		1.8	ns
$t_{\text{F20+}}$		2.2		2.2		2.3	ns
$t_{\text{CH}}$	2.0		2.5		3.0		ns
$t_{\text{CL}}$	2.0		2.5		3.0		ns
$t_{\text{CLRP}}$	0.3		0.4		0.4		ns
$t_{\text{PREP}}$	0.5		0.5		0.5		ns
$t_{\text{ESBCH}}$	2.0		2.5		3.0		ns
$t_{\text{ESBCL}}$	2.0		2.5		3.0		ns
$t_{\text{ESBWP}}$	1.6		1.9		2.2		ns
$t_{\text{ESBRP}}$	1.0		1.3		1.4		ns

Tables 55 through 60 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

**Table 55. EP20K60E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.17		0.15		0.16		ns
$t_H$	0.32		0.33		0.39		ns
$t_{CO}$		0.29		0.40		0.60	ns
$t_{LUT}$		0.77		1.07		1.59	ns

**Table 57. EP20K60E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

**Table 60. EP20K60E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.77		2.91		3.11		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{\text{XZBIDIR}}$		6.47		7.44		8.65	ns
$t_{\text{ZXBIDIR}}$		6.47		7.44		8.65	ns
$t_{\text{INSUBIDIRPLL}}$	3.44		3.24		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.37	0.50	3.69	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.00		5.82		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.00		5.82		-	ns

Tables 61 through 66 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

**Table 61. EP20K100E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.28		0.34	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns



**Table 80. EP20K300E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.79		2.44		3.25	ns
$t_{ESBSRC}$		2.40		3.12		4.01	ns
$t_{ESBAWC}$		3.41		4.65		6.20	ns
$t_{ESBSWC}$		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
$t_{ESBDD}$		3.41		4.65		6.20	ns
$t_{PD}$		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

**Table 81. EP20K300E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.24		0.26	ns
$t_{F5-20}$		1.33		1.43		1.58	ns
$t_{F20+}$		3.63		3.93		4.35	ns

**Table 92. EP20K600E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		2.39		3.11	ns
$t_{ESBSRC}$		2.27		3.07		3.86	ns
$t_{ESBAWC}$		3.19		4.56		5.93	ns
$t_{ESBSWC}$		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATAO1}$		1.01		1.19		1.37	ns
$t_{ESBDATAO2}$		2.18		3.12		4.05	ns
$t_{ESBDD}$		3.19		4.56		5.93	ns
$t_{PD}$		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

**Table 93. EP20K600E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.25		0.26	ns
$t_{F5-20}$		1.26		1.39		1.52	ns
$t_{F20+}$		3.51		3.88		4.26	ns

**Table 110. Selectable I/O Standard Output Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVC MOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		−0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		−0.48		−0.48		−0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

## Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at <http://www.altera.com>.

## Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to  $V_{CCIO}$  by a built-in weak pull-up resistor.

## Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

### Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

### Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for  $t_{\text{ESB DATAH}}$  parameter.

### Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

### Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$  added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).