# Intel - EP20K100EQC240-2 Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 416 |
| Number of Logic Elements/Cells | 4160 |
| Total RAM Bits | 53248 |
| Number of I/O | 183 |
| Number of Gates | 263000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k100eqc240-2 |

*Table 5. APEX 20K FineLine BGA Package Options & I/O Count* *Notes (1), (2)*

| Device | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| EP20K30E | 93 | 128 | | | |
| EP20K60E | 93 | 196 | | | |
| EP20K100 | | 252 | | | |
| EP20K100E | 93 | 246 | | | |
| EP20K160E | | | 316 | | |
| EP20K200 | | | 382 | | |
| EP20K200E | | | 376 | 376 | |
| EP20K300E | | | | 408 | |
| EP20K400 | | | | 502 *(3)* | |
| EP20K400E | | | | 488 *(3)* | |
| EP20K600E | | | | 508 *(3)* | 588 |
| EP20K1000E | | | | 508 *(3)* | 708 |
| EP20K1500E | | | | | 808 |

***Notes to Tables 4 and 5:***

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

*Table 6. APEX 20K QFP, BGA & PGA Package Sizes*

| Feature | 144-Pin TQFP | 208-Pin QFP | 240-Pin QFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.27 | 1.27 | – |
| Area ($mm^2$) | 484 | 924 | 1,218 | 1,225 | 2,025 | 3,906 |
| Length × Width (mm × mm) | 22 × 22 | 30.4 × 30.4 | 34.9 × 34.9 | 35 × 35 | 45 × 45 | 62.5 × 62.5 |

*Table 7. APEX 20K FineLine BGA Package Sizes*

| Feature | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 169 | 361 | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 13 × 13 | 19 × 19 | 23 × 23 | 27 × 27 | 33 × 33 |

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

***Figure 3. LAB Structure***

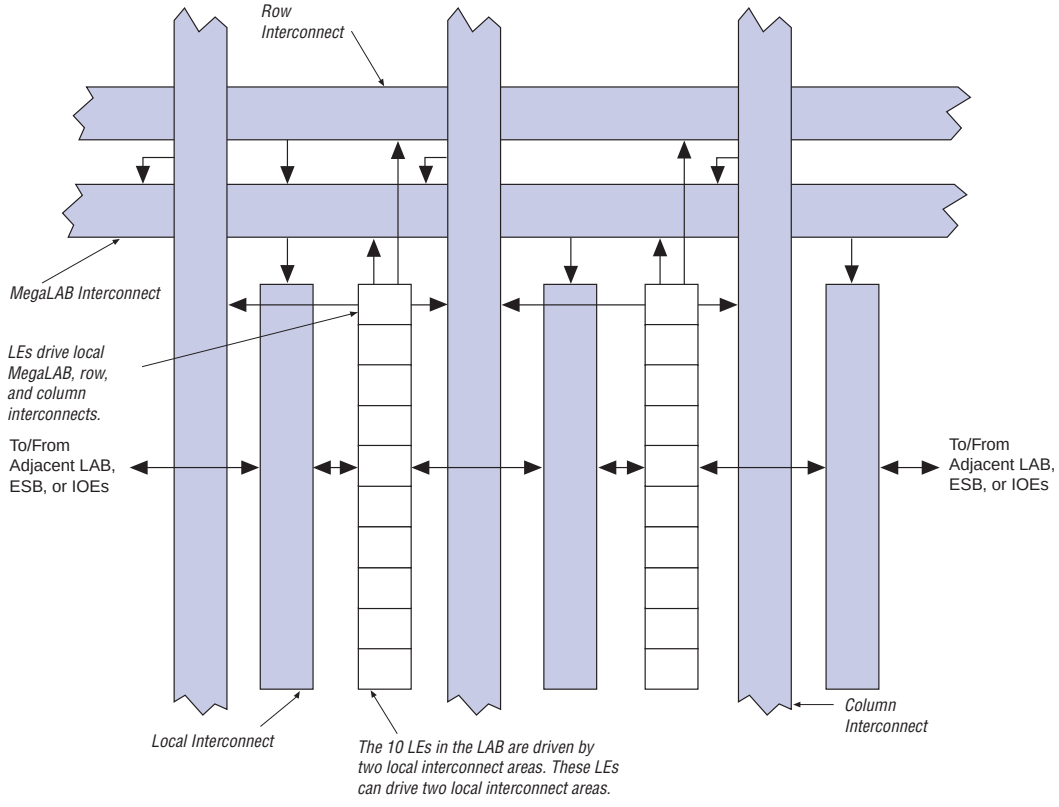
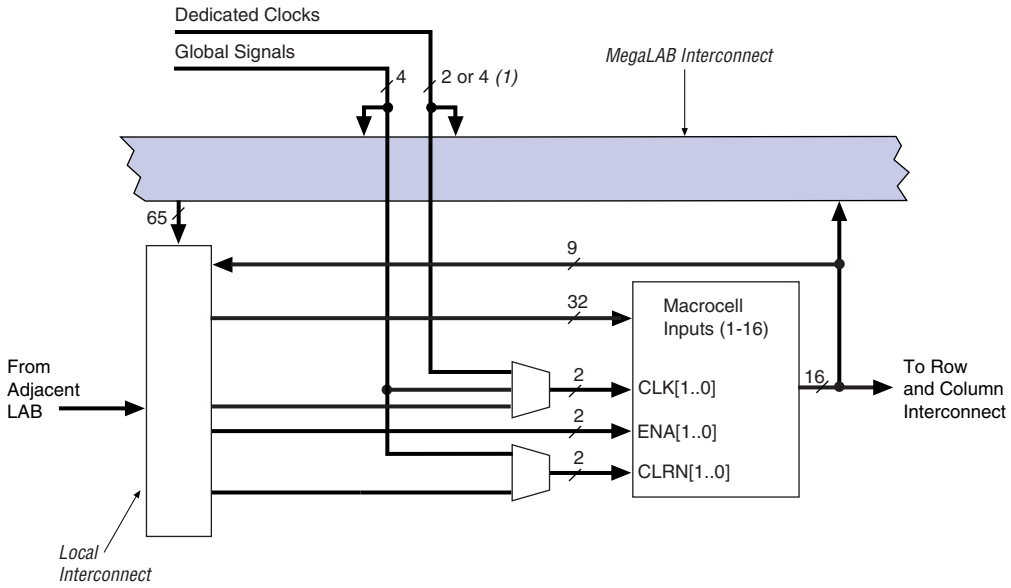


*Figure 13. Product-Term Logic in ESB*




*Note to Figure 13:*
(1) APEX 20KE devices have four dedicated clocks.

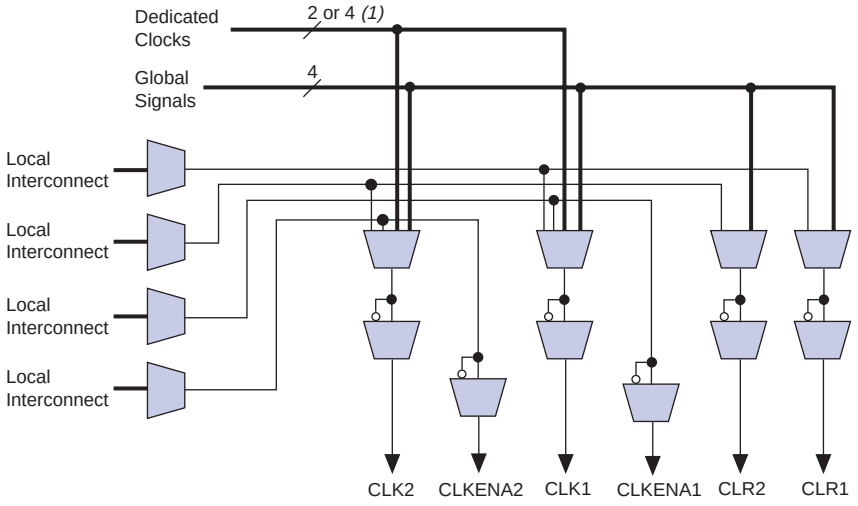
## Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*



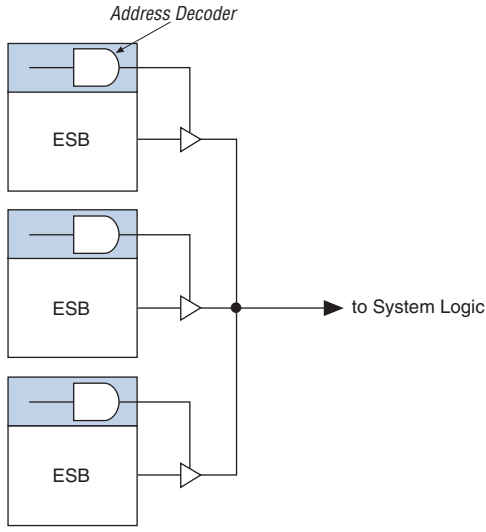

*Note to Figure 15:*
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

*Figure 18. Deep Memory Block Implemented with Multiple ESBs*




The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in Figure 19.

*Figure 19. APEX 20K ESB Implementing Dual-Port RAM*

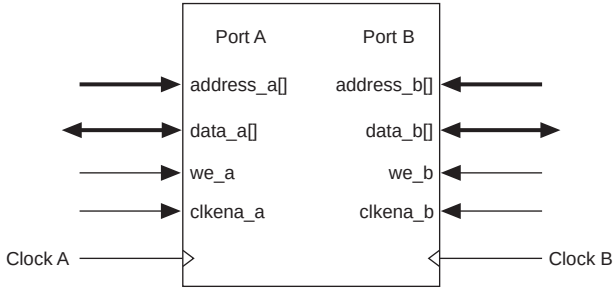
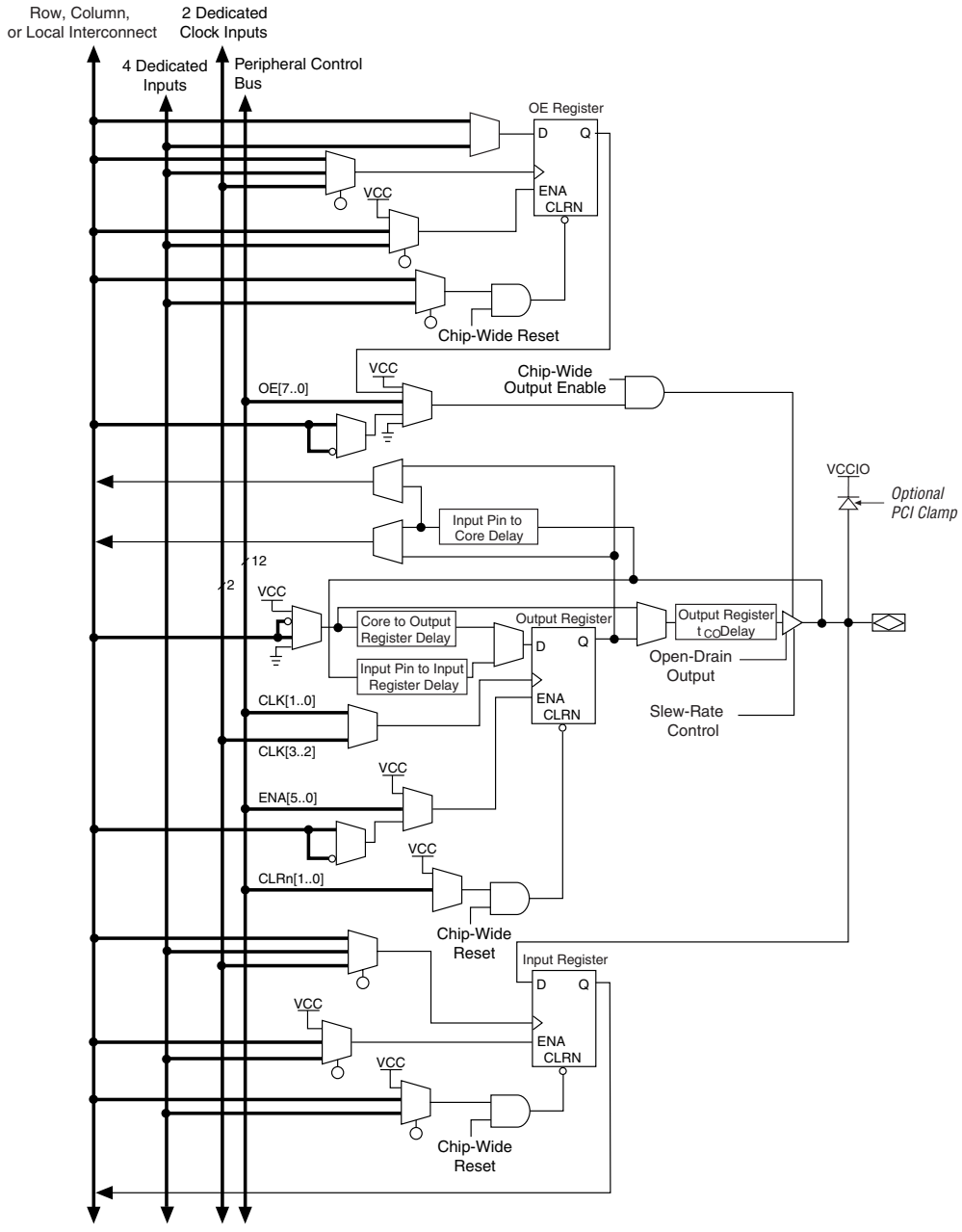


***Figure 25. APEX 20K Bidirectional I/O Registers*** *Note (1)*




*Note to Figure 25:*

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

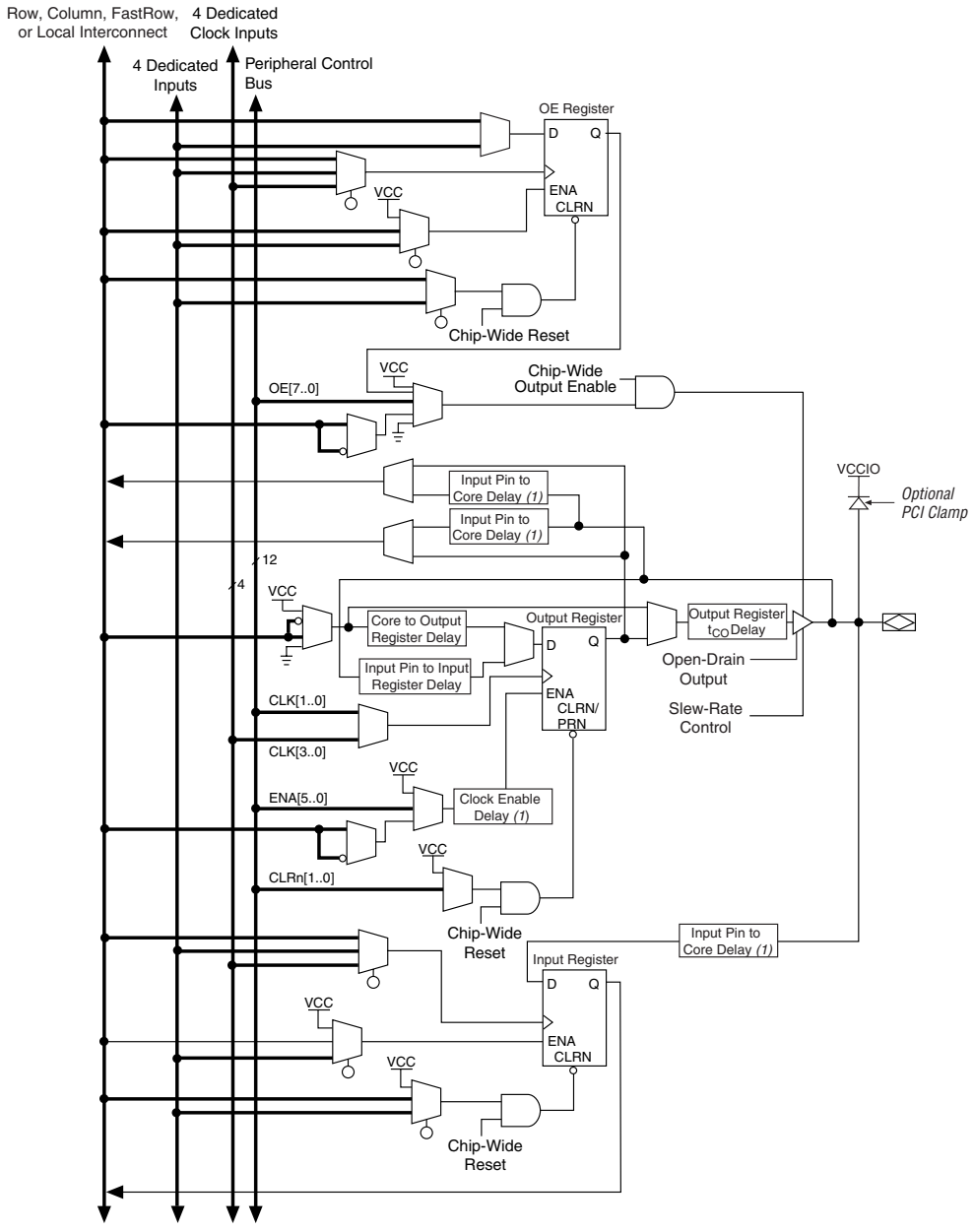
Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

*Table 11. APEX 20KE Programmable Delay Chains*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input Pin to Core Delay | Decrease input delay to internal cells |
| Input Pin to Input Register Delay | Decrease input delay to input registers |
| Core to Output Register Delay | Decrease input delay to output register |
| Output Register $t_{CO}$ Delay | Increase delay to output pin |
| Clock Enable Delay | Increase clock enable delay |

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

***Figure 26. APEX 20KE Bidirectional I/O Registers*** *Notes (1), (2)*




*Notes to Figure 26:*

(1) This programmable delay has four settings: off and three levels of delay.

(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

**Table 30. APEX 20KE Device Capacitance** *Note (15)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 27 through 30:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

| Vin | Max. Duty Cycle |
|---|---|
| 4.0V | 100% (DC) |
| 4.1 | 90% |
| 4.2 | 50% |
| 4.3 | 30% |
| 4.4 | 17% |
| 4.5 | 10% |

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, and $I_I$ parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.

| Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 2 of 2) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB macrocell register clock-to-output delay |
| $t_{F1-4}$ | Fanout delay using local interconnect |
| $t_{F5-20}$ | Fanout delay using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay using FastTrack Interconnect |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 32 and 33 describe APEX 20K external timing parameters.

| Table 32. APEX 20K External Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Clock Parameter** |
| $t_{INSU}$ | Setup time with global clock at IOE register |
| $t_{INH}$ | Hold time with global clock at IOE register |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register |

| Table 33. APEX 20K External Bidirectional Timing Parameters *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | C1 = 10 pF |

*Note to Tables 32 and 33:*
(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the $f_{MAX}$ timing model.

*Table 34. APEX 20KE LE Timing Microparameters*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in to data-out |

*Table 35. APEX 20KE ESB Timing Microparameters*

| Symbol | Parameter |
|---|---|
| $t_{ESBARC}$ | ESB Asynchronous read cycle time |
| $t_{ESBSRC}$ | ESB Synchronous read cycle time |
| $t_{ESBAWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBSWC}$ | ESB Synchronous write cycle time |
| $t_{ESBWASU}$ | ESB write address setup time with respect to WE |
| $t_{ESBWAH}$ | ESB write address hold time with respect to WE |
| $t_{ESBWDSU}$ | ESB data setup time with respect to WE |
| $t_{ESBWDH}$ | ESB data hold time with respect to WE |
| $t_{ESBRASU}$ | ESB read address setup time with respect to RE |
| $t_{ESBRAH}$ | ESB read address hold time with respect to RE |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBWEH}$ | ESB WE hold time after clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBWADDRSU}$ | ESB write address setup time before clock when using input registers |
| $t_{ESBRADDRSU}$ | ESB read address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB Macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB Macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB Macrocell register clock-to-output delay |

Tables 40 through 42 show the $f_{MAX}$ timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 40. EP20K100 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.6 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

*Table 41. EP20K200 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.7 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

*Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

*Table 51. EP20K30E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

*Table 52. EP20K30E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CLRP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{PREP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{ESBCH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBCL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBWP}$ | 1.43 | | 2.01 | | 2.97 | | ns |
| $t_{ESBRP}$ | 1.15 | | 1.62 | | 2.39 | | ns |

*Table 53. EP20K30E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.02 | | 2.13 | | 2.24 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{INSUPLL}$ | 2.11 | | 2.23 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |

*Table 54. EP20K30E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.85 | | 1.77 | | 1.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{XZBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{ZXBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{INSUBIDIRPLL}$ | 4.12 | | 4.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |

*Table 62. EP20K100E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.61 | | 1.84 | | 1.97 | ns |
| $t_{ESBSRC}$ | | 2.57 | | 2.97 | | 3.20 | ns |
| $t_{ESBAWC}$ | | 0.52 | | 4.09 | | 4.39 | ns |
| $t_{ESBSWC}$ | | 3.17 | | 3.78 | | 4.09 | ns |
| $t_{ESBWASU}$ | 0.56 | | 6.41 | | 0.63 | | ns |
| $t_{ESBWAH}$ | 0.48 | | 0.54 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.71 | | 0.80 | | 0.81 | | ns |
| $t_{ESBWDH}$ | .048 | | 0.54 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.57 | | 1.75 | | 1.87 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.20 | | ns |
| $t_{ESBWESU}$ | 1.54 | | 1.72 | | 1.80 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.16 | | -0.20 | | -0.20 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.12 | | 0.08 | | 0.13 | | ns |
| $t_{ESBRADDRSU}$ | 0.17 | | 0.15 | | 0.19 | | ns |
| $t_{ESBDATACO1}$ | | 1.20 | | 1.39 | | 1.52 | ns |
| $t_{ESBDATACO2}$ | | 2.54 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.06 | | 3.56 | | 3.85 | ns |
| $t_{PD}$ | | 1.73 | | 2.02 | | 2.20 | ns |
| $t_{PTERMSU}$ | 1.11 | | 1.26 | | 1.38 | | ns |
| $t_{PTERMCO}$ | | 1.19 | | 1.40 | | 1.08 | ns |

*Table 63. EP20K100E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.04 | | 1.26 | | 1.52 | ns |
| $t_{F20+}$ | | 1.12 | | 1.36 | | 1.86 | ns |

Tables 67 through 72 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

*Table 67. EP20K160E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.25 | | 0.31 | | 0.35 | ns |
| $t_{LUT}$ | | 0.69 | | 0.88 | | 1.12 | ns |

*Table 74. EP20K200E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.68 | | 2.06 | | 2.24 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 2.77 | | 3.18 | ns |
| $t_{ESBAWC}$ | | 3.10 | | 3.86 | | 4.50 | ns |
| $t_{ESBSWC}$ | | 2.90 | | 3.67 | | 4.21 | ns |
| $t_{ESBWASU}$ | 0.55 | | 0.67 | | 0.74 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.83 | | 0.95 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.90 | | 2.09 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.42 | | 1.71 | | 2.01 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.06 | | -0.07 | | 0.05 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.13 | | 0.31 | | ns |
| $t_{ESBRADDRSU}$ | 0.18 | | 0.23 | | 0.39 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.35 | | 1.51 | ns |
| $t_{ESBDATACO2}$ | | 2.19 | | 2.75 | | 3.22 | ns |
| $t_{ESBDD}$ | | 2.75 | | 3.41 | | 4.03 | ns |
| $t_{PD}$ | | 1.58 | | 1.97 | | 2.33 | ns |
| $t_{PTERMSU}$ | 1.00 | | 1.22 | | 1.51 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.37 | | 1.09 | ns |

*Table 75. EP20K200E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.02 | | 1.20 | | 1.41 | ns |
| $t_{F20+}$ | | 1.99 | | 2.23 | | 2.53 | ns |

*Table 86. EP20K400E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 1.91 | | 1.99 | ns |
| $t_{ESBSRC}$ | | 2.30 | | 2.66 | | 2.93 | ns |
| $t_{ESBAWC}$ | | 3.09 | | 3.58 | | 3.99 | ns |
| $t_{ESBSWC}$ | | 3.01 | | 3.65 | | 4.05 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.63 | | 0.65 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.77 | | 0.84 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.77 | | 1.86 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.35 | | 1.47 | | 1.61 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.18 | | -0.30 | | -0.27 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | -0.02 | | -0.11 | | -0.03 | | ns |
| $t_{ESBRADDRSU}$ | 0.06 | | -0.01 | | -0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.16 | | 1.40 | | 1.54 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 2.55 | | 2.85 | ns |
| $t_{ESBDD}$ | | 2.73 | | 3.17 | | 3.58 | ns |
| $t_{PD}$ | | 1.57 | | 1.83 | | 2.07 | ns |
| $t_{PTERMSU}$ | 0.92 | | 0.99 | | 1.18 | | ns |
| $t_{PTERMCO}$ | | 1.18 | | 1.43 | | 1.17 | ns |

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 111. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, EPC16 configuration devices |
| Passive serial (PS) | MasterBlaster or ByteBlasterMV download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File |

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

## Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information