



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	92
Number of Gates	263000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100etc144-1n

Table 5. APEX 20K FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 (3)	
EP20K400E				488 (3)	
EP20K600E				508 (3)	588
EP20K1000E				508 (3)	708
EP20K1500E					808

Notes to Tables 4 and 5:

- (1) I/O counts include dedicated input and clock pins.
- (2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
- (3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	—
Area (mm ²)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 7. APEX 20K FineLine BGA Package Sizes

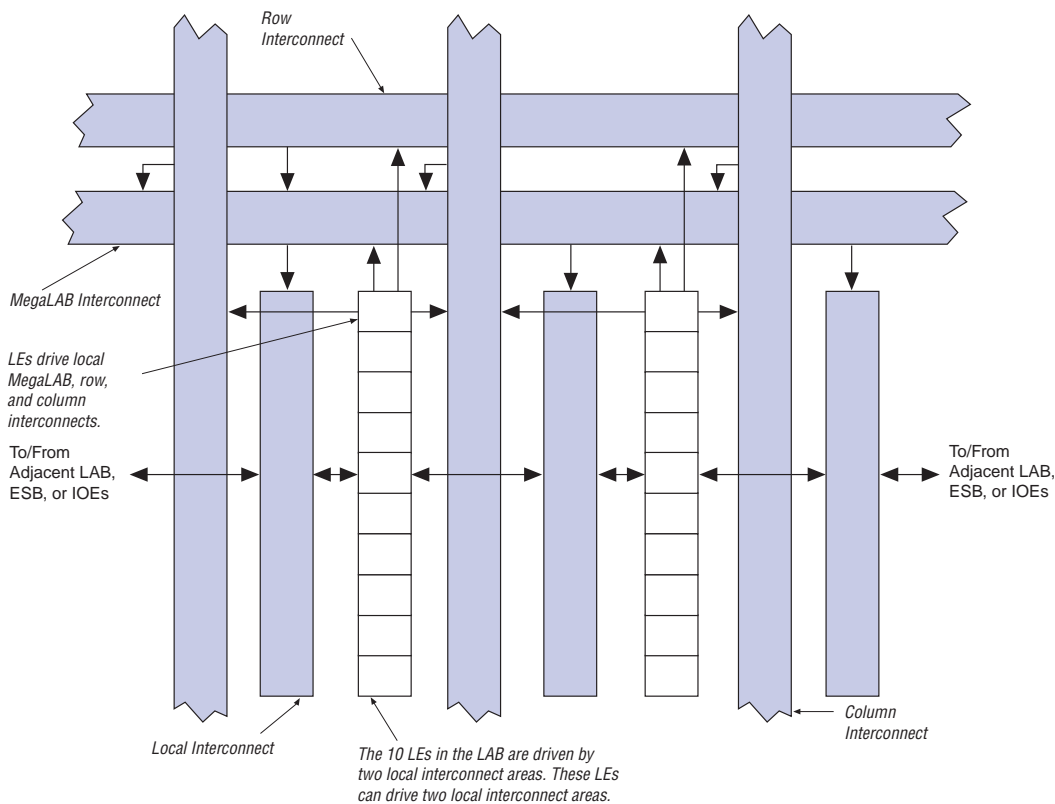
Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

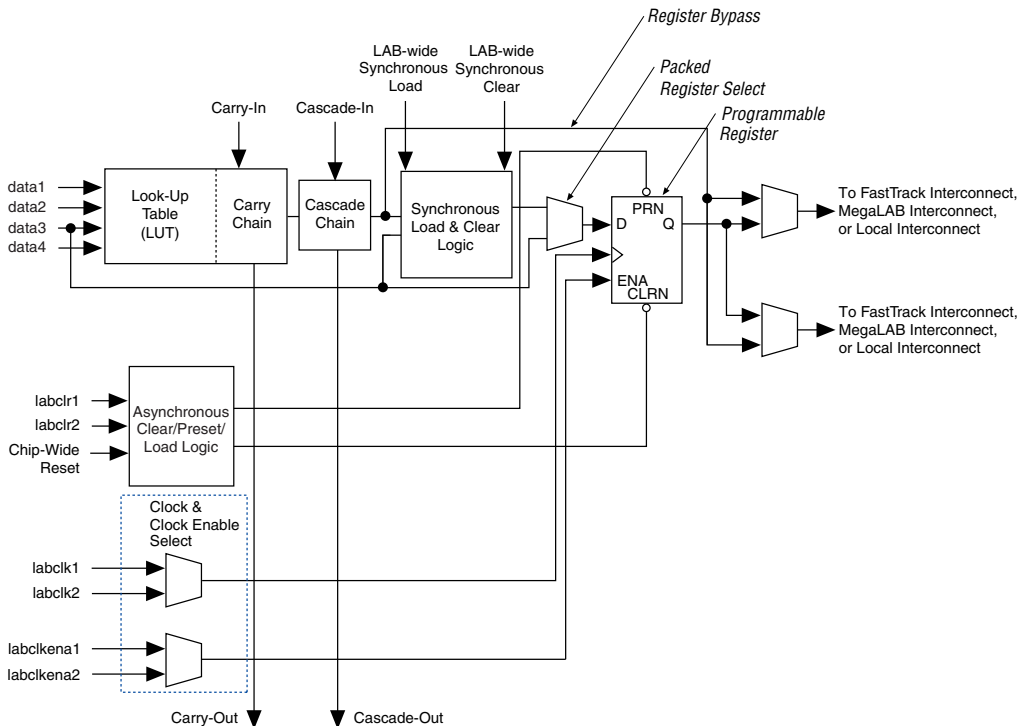
Figure 3. LAB Structure



Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See [Figure 5](#).

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

LE Operating Modes

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. [Figure 8](#) shows the LE operating modes.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

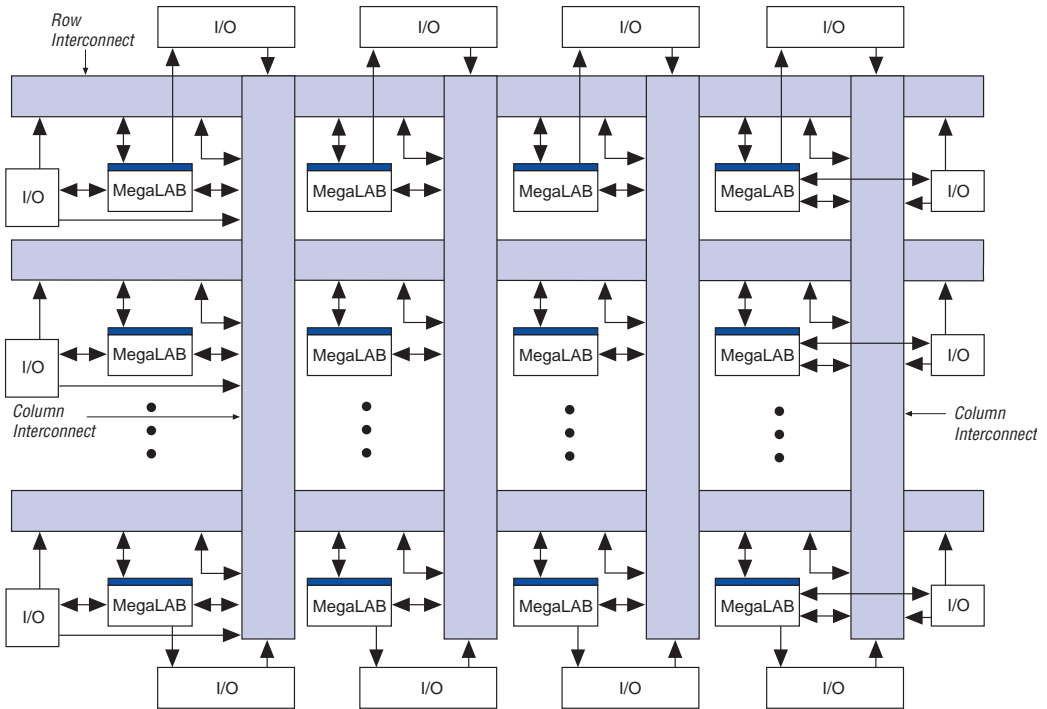
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).

Figure 9. APEX 20K Interconnect Structure

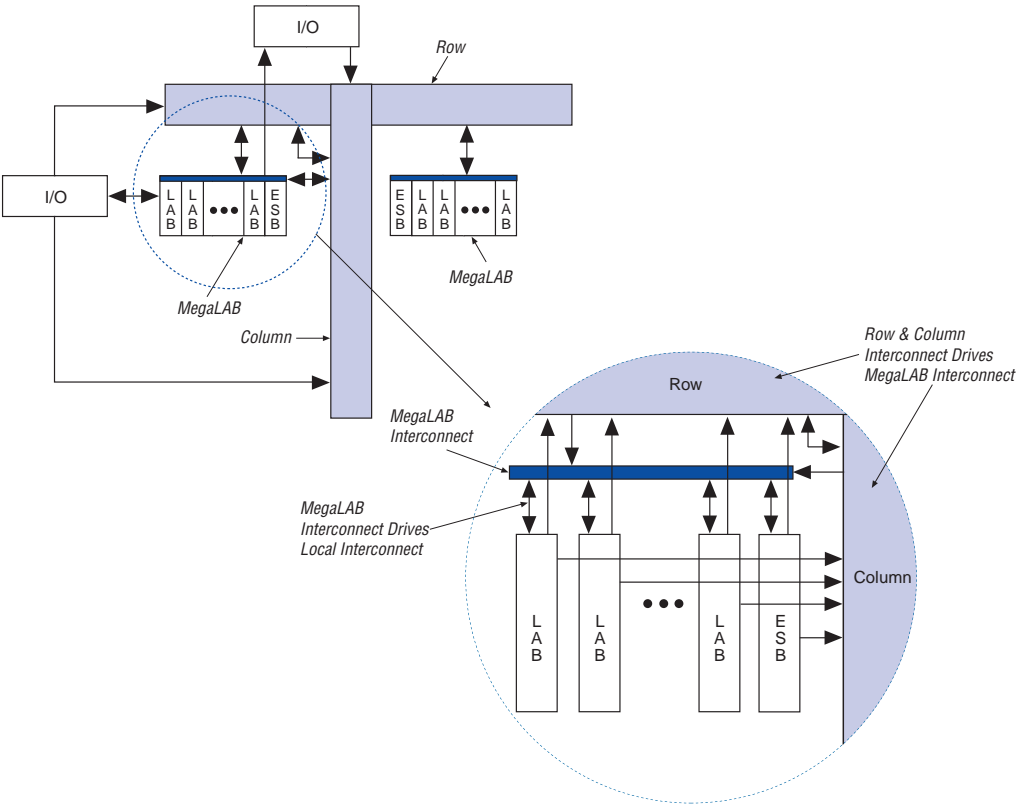


A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect



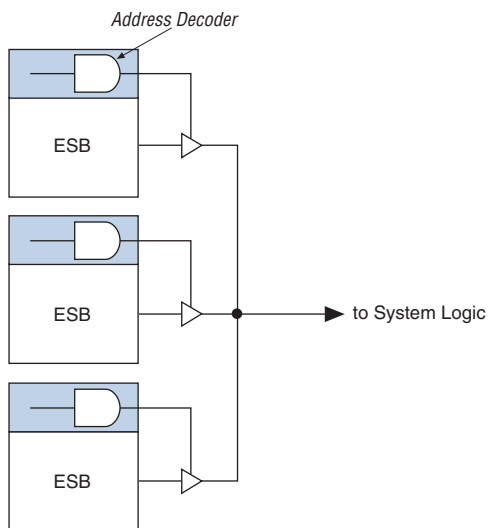
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (*WE*) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the *WE* signal. In contrast, the ESB's synchronous RAM generates its own *WE* signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128×16 , 256×8 , 512×4 , $1,024 \times 2$, or $2,048 \times 1$. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128×16 RAM blocks can be combined to form a 128×32 RAM block, and two 512×4 RAM blocks can be combined to form a 512×8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).

Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in [Figure 19](#).

Figure 19. APEX 20K ESB Implementing Dual-Port RAM

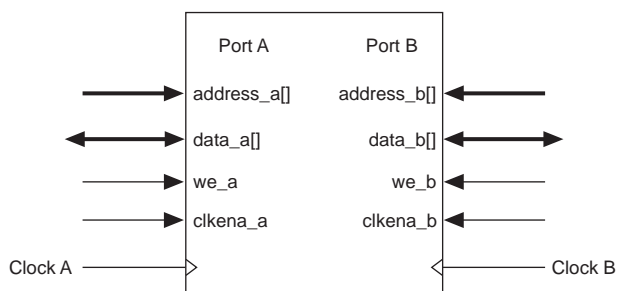
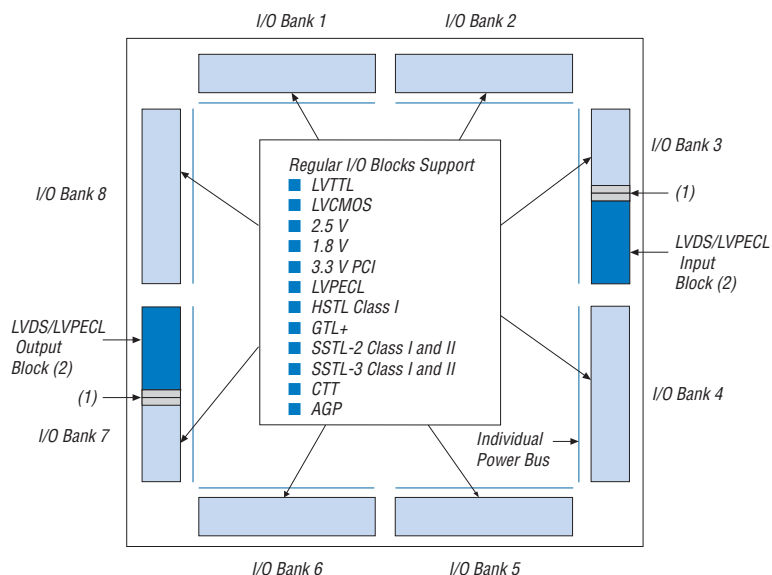


Figure 29. APEX 20KE I/O Banks

Notes to Figure 29:

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.



For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

MultiVolt I/O Interface

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V VCCINT level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

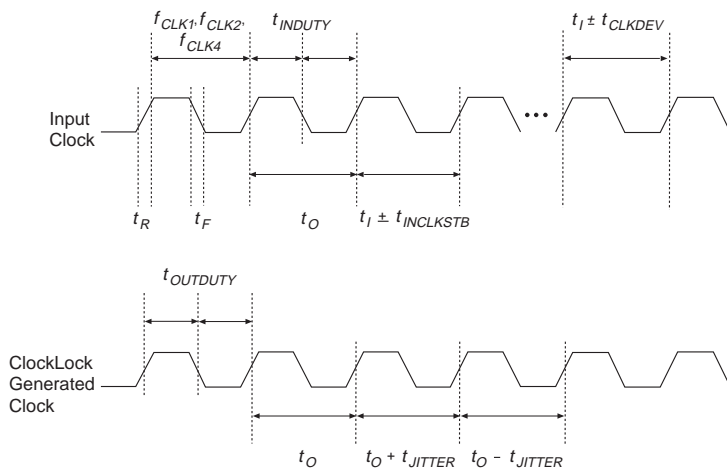
Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support						
V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

Notes to Table 12:

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
- (2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Figure 30. Specifications for the Incoming & Generated Clocks *Note (1)*



Note to Figure 30:

- (1) The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)				
Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	180	MHz
f_{CLK1} (1)	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	180 (1)	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	90	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	48	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) (2)		25,000 (3)	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ClockBoost to acquire lock (4)		10	μ s

Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	(3), (6)	−0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (9)		5.75	V
V_{IL}	Low-level input voltage		−0.5		$0.8, 0.3 \times V_{CCIO}$ (9)	V
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (10)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (10)	1.7			V

Table 28. APEX 20KE Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	(5), (6)	−0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	°C
		For industrial use	−40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms

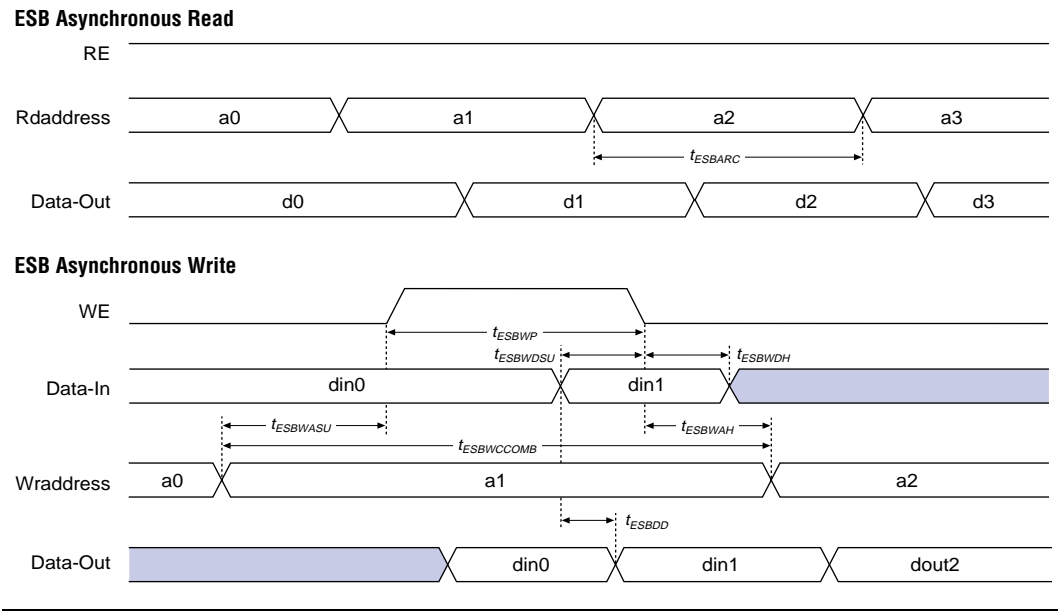


Table 39. APEX 20KE External Bidirectional Timing Parameters *Note (1)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
t_{INHBDIR}	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{\text{OUTCOBDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
t_{XZBDIR}	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
t_{ZXBIDIR}	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{\text{INSUBIDIRPLL}}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{\text{INHBDIRPLL}}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{\text{OUTCOBDIRPLL}}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{\text{XZBDIRPLL}}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{\text{ZXBIDIRPLL}}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

Note to Tables 38 and 39:

(1) These timing parameters are sample-tested only.

Table 46. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.9		2.3		2.6		ns
$t_{\text{INHBIDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{\text{XZBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{ZXBIDIR}} (1)$		5.0		5.9		6.9	ns
$t_{\text{INSUBIDIR}} (2)$	1.1		1.2		—		ns
$t_{\text{INHBIDIR}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	2.7	0.5	3.1	—	—	ns
$t_{\text{XZBIDIR}} (2)$		4.3		5.0		—	ns
$t_{\text{ZXBIDIR}} (2)$		4.3		5.0		—	ns

Table 47. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSU}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INH}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{INSU}} (2)$	0.4		1.0		—		ns
$t_{\text{INH}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCO}} (2)$	0.5	3.1	0.5	4.1	—	—	ns

Table 48. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}} (1)$	1.4		1.8		2.0		ns
$t_{\text{INHBIDIR}} (1)$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}} (1)$	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{\text{XZBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{ZXBIDIR}} (1)$		7.3		8.9		10.3	ns
$t_{\text{INSUBIDIR}} (2)$	0.5		1.0		—		ns
$t_{\text{INHBIDIR}} (2)$	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}} (2)$	0.5	3.1	0.5	4.1	—	—	ns
$t_{\text{XZBIDIR}} (2)$		6.2		7.6		—	ns
$t_{\text{ZXBIDIR}} (2)$		6.2		7.6		—	ns

Table 56. EP20K60E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.83		2.57		3.79	ns
t_{ESBSRC}		2.46		3.26		4.61	ns
t_{ESBAWC}		3.50		4.90		7.23	ns
t_{ESBSWC}		3.77		4.90		6.79	ns
$t_{ESBWASU}$	1.59		2.23		3.29		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.75		2.46		3.62		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.76		2.47		3.64		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.68		2.49		3.87		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.08		0.43		1.04		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.29		0.72		1.46		ns
$t_{ESBRADDRSU}$	0.36		0.81		1.58		ns
$t_{ESBDATACO1}$		1.06		1.24		1.55	ns
$t_{ESBDATACO2}$		2.39		3.35		4.94	ns
t_{ESBDD}		3.50		4.90		7.23	ns
t_{PD}		1.72		2.41		3.56	ns
$t_{PTERMSU}$	0.99		1.56		2.55		ns
$t_{PTERMCO}$		1.07		1.26		1.08	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.47		3.68		3.99		ns
t_{INHBIDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
t_{XZBIDIR}		6.91		7.62		8.38	ns
t_{ZXBIDIR}		6.91		7.62		8.38	ns
$t_{\text{INSUBIDIRPLL}}$	3.05		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.67	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		3.41		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		-0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		-0.24		-0.23		-0.19	ns
SSTL-3 Class I		-0.32		-0.21		-0.47	ns
SSTL-3 Class II		-0.08		0.03		-0.23	ns
SSTL-2 Class I		-0.17		-0.06		-0.32	ns
SSTL-2 Class II		-0.16		-0.05		-0.31	ns
LVDS		-0.12		-0.12		-0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 111. Data Sources for Configuration	
Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File



For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information