Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	93
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100fc144-1

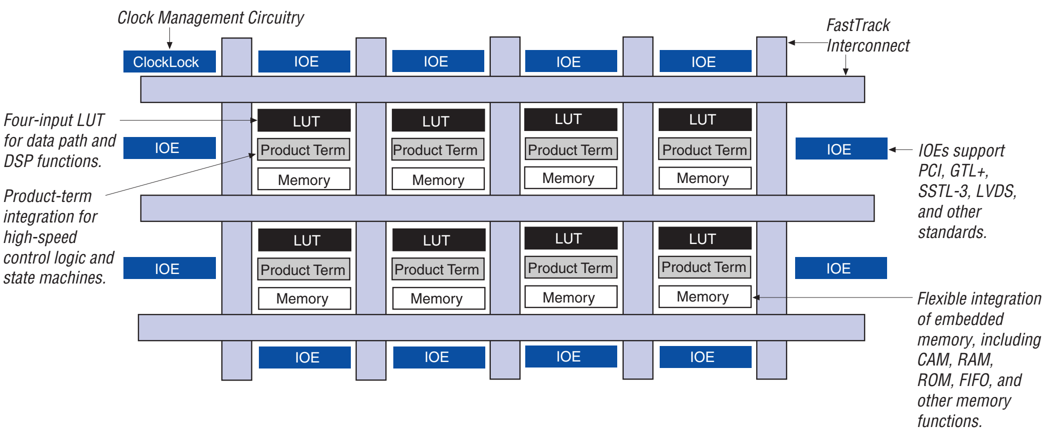
Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

Figure 1. APEX 20K Device Block Diagram



Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain

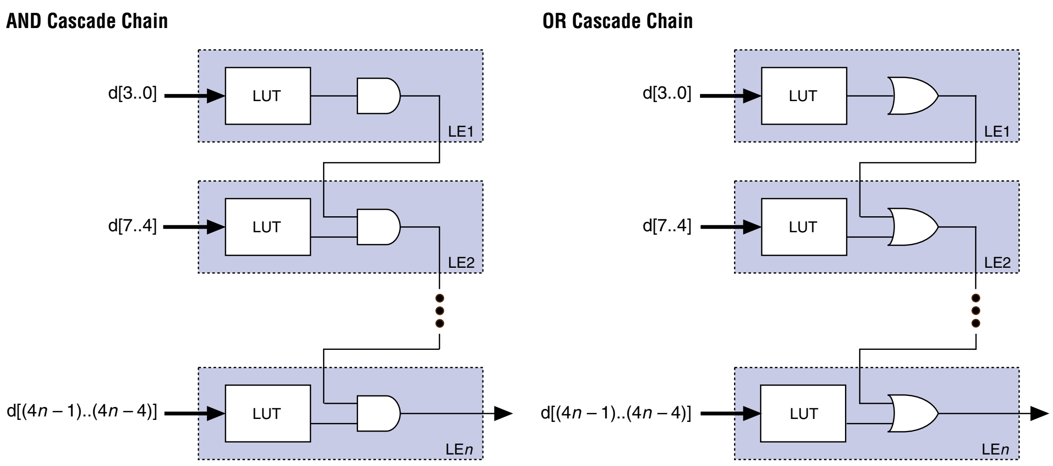
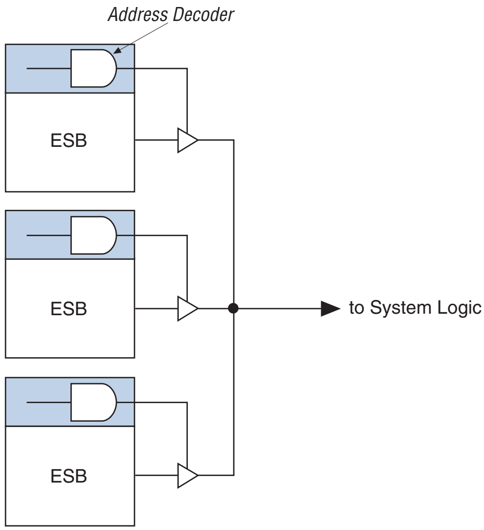
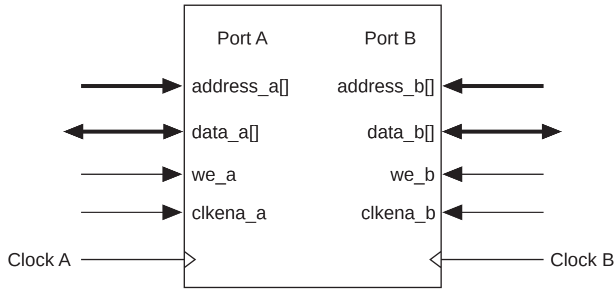


Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in Figure 19.

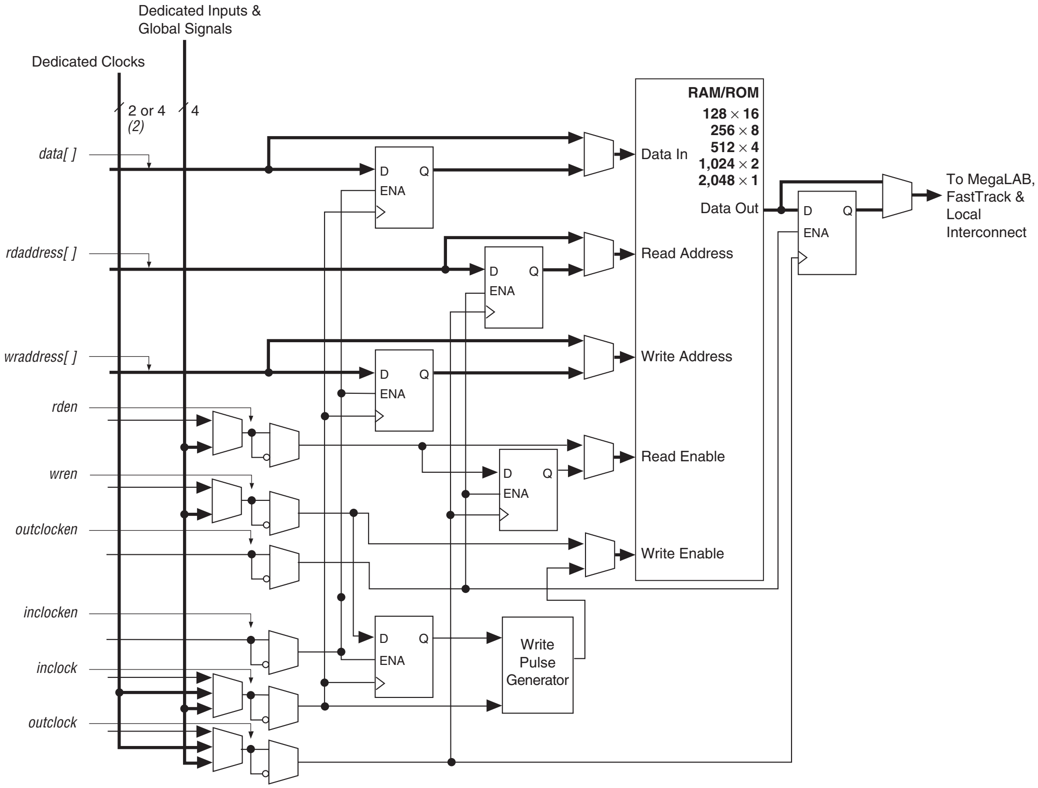
Figure 19. APEX 20K ESB Implementing Dual-Port RAM



Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, `WE`, and write address. The other clock controls all registers associated with reading: read enable (`RE`), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Notes to Figure 20:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

Table 10. APEX 20K Programmable Delay Chains

Programmable Delays	Quartus II Logic Option
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register t_{CO} delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

Table 11. APEX 20KE Programmable Delay Chains

Programmable Delays	Quartus II Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

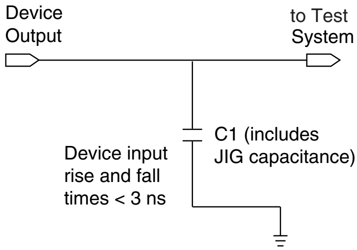
Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 *(1)*

Note to Table 20:

(1) This device does not support JTAG boundary scan testing.

Figure 32. APEX 20K AC Test Conditions *Note (1)*



Note to Figure 32:

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 26. APEX 20K 5.0-V Tolerant Device Capacitance *Notes (2), (14)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 23 through 26:

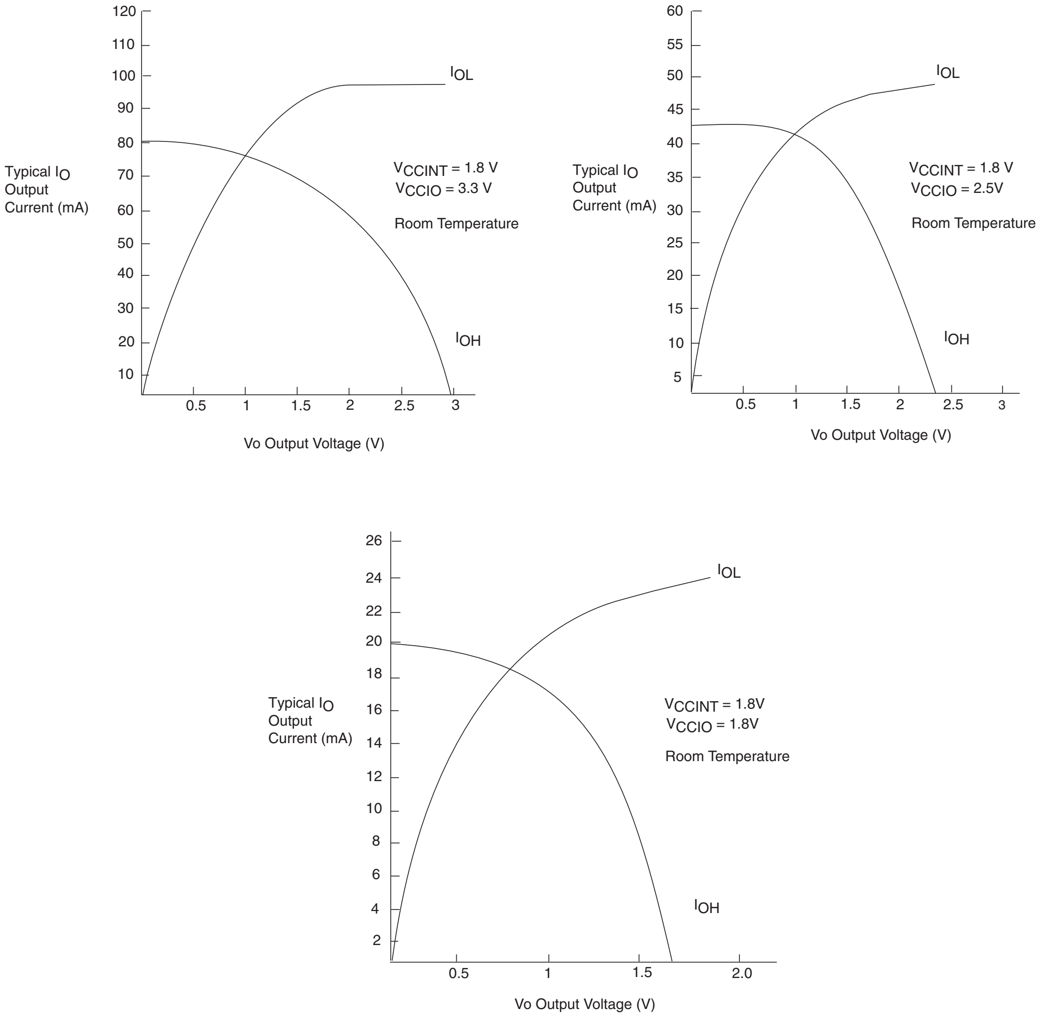
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A= 25° C, V_{CCINT} = 2.5 V, and V_{CCIO} = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
(10) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
(11) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 27. APEX 20KE Device Absolute Maximum Ratings *Note (1)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	2.5	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices *Note (1)*



Note to Figure 35:

(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Table 46. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(1)*	1.9		2.3		2.6		ns
$t_{INHBIDIR}$ *(1)*	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ *(1)*	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{XZBIDIR}$ *(1)*		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ *(1)*		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ *(2)*	1.1		1.2		–		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(2)*	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ *(2)*		4.3		5.0		–	ns
$t_{ZXBIDIR}$ *(2)*		4.3		5.0		–	ns

Table 47. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} *(1)*	1.4		1.8		2.0		ns
t_{INH} *(1)*	0.0		0.0		0.0		ns
t_{OUTCO} *(1)*	2.0	4.9	2.0	6.1	2.0	7.0	ns
t_{INSU} *(2)*	0.4		1.0		–		ns
t_{INH} *(2)*	0.0		0.0		–		ns
t_{OUTCO} *(2)*	0.5	3.1	0.5	4.1	–	–	ns

Table 48. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(1)*	1.4		1.8		2.0		ns
$t_{INHBIDIR}$ *(1)*	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ *(1)*	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{XZBIDIR}$ *(1)*		7.3		8.9		10.3	ns
$t_{ZXBIDIR}$ *(1)*		7.3		8.9		10.3	ns
$t_{INSUBIDIR}$ *(2)*	0.5		1.0		–		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(2)*	0.5	3.1	0.5	4.1	–	–	ns
$t_{XZBIDIR}$ *(2)*		6.2		7.6		–	ns
$t_{ZXBIDIR}$ *(2)*		6.2		7.6		–	ns

Table 56. EP20K60E f_{MAX} ESB Timing Microparameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.83		2.57		3.79	ns
t_{ESBSRC}		2.46		3.26		4.61	ns
t_{ESBAWC}		3.50		4.90		7.23	ns
t_{ESBSWC}		3.77		4.90		6.79	ns
$t_{ESBWASU}$	1.59		2.23		3.29		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.75		2.46		3.62		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.76		2.47		3.64		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.68		2.49		3.87		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.08		0.43		1.04		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.29		0.72		1.46		ns
$t_{ESBRADDRSU}$	0.36		0.81		1.58		ns
$t_{ESBDATACO1}$		1.06		1.24		1.55	ns
$t_{ESBDATACO2}$		2.39		3.35		4.94	ns
t_{ESBDD}		3.50		4.90		7.23	ns
t_{PD}		1.72		2.41		3.56	ns
$t_{PTERMSU}$	0.99		1.56		2.55		ns
$t_{PTERMCO}$		1.07		1.26		1.08	ns

Table 62. EP20K100E f_{MAX} ESB Timing Microparameters							
Symbol	**-1**		**-2**		**-3**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ESBARC}		1.61		1.84		1.97	ns
t_{ESBSRC}		2.57		2.97		3.20	ns
t_{ESBAWC}		0.52		4.09		4.39	ns
t_{ESBSWC}		3.17		3.78		4.09	ns
$t_{ESBWASU}$	0.56		6.41		0.63		ns
t_{ESBWAH}	0.48		0.54		0.55		ns
$t_{ESBWDSU}$	0.71		0.80		0.81		ns
t_{ESBWDH}	.048		0.54		0.55		ns
$t_{ESBRASU}$	1.57		1.75		1.87		ns
t_{ESBRAH}	0.00		0.00		0.20		ns
$t_{ESBWESU}$	1.54		1.72		1.80		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.16		-0.20		-0.20		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.12		0.08		0.13		ns
$t_{ESBRADDRSU}$	0.17		0.15		0.19		ns
$t_{ESBDATACO1}$		1.20		1.39		1.52	ns
$t_{ESBDATACO2}$		2.54		2.99		3.22	ns
t_{ESBDD}		3.06		3.56		3.85	ns
t_{PD}		1.73		2.02		2.20	ns
$t_{PTERMSU}$	1.11		1.26		1.38		ns
$t_{PTERMCO}$		1.19		1.40		1.08	ns

Table 63. EP20K100E f_{MAX} Routing Delays							
Symbol	**-1**		**-2**		**-3**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{F1-4}		0.24		0.27		0.29	ns
t_{F5-20}		1.04		1.26		1.52	ns
t_{F20+}		1.12		1.36		1.86	ns

Tables 67 through 72 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

Table 67. EP20K160E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.24		0.26		ns
t_H	0.22		0.24		0.26		ns
t_{CO}		0.25		0.31		0.35	ns
t_{LUT}		0.69		0.88		1.12	ns

Table 68. EP20K160E f_{MAX} ESB Timing Microparameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.65		2.02		2.11	ns
t_{ESBSRC}		2.21		2.70		3.11	ns
t_{ESBAWC}		3.04		3.79		4.42	ns
t_{ESBSWC}		2.81		3.56		4.10	ns
$t_{ESBWASU}$	0.54		0.66		0.73		ns
t_{ESBWAH}	0.36		0.45		0.47		ns
$t_{ESBWDSU}$	0.68		0.81		0.94		ns
t_{ESBWDH}	0.36		0.45		0.47		ns
$t_{ESBRASU}$	1.58		1.87		2.06		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.41		1.71		2.00		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.02		-0.03		0.09		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.14		0.17		0.35		ns
$t_{ESBRADDRSU}$	0.21		0.27		0.43		ns
$t_{ESBDATACO1}$		1.04		1.30		1.46	ns
$t_{ESBDATACO2}$		2.15		2.70		3.16	ns
t_{ESBDD}		2.69		3.35		3.97	ns
t_{PD}		1.55		1.93		2.29	ns
$t_{PTERMSU}$	1.01		1.23		1.52		ns
$t_{PTERMCO}$		1.06		1.32		1.04	ns

Tables 85 through 90 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

Table 85. EP20K400E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.23		0.23		ns
t_{H}	0.23		0.23		0.23		ns
t_{CO}		0.25		0.29		0.32	ns
t_{LUT}		0.70		0.83		1.01	ns

Table 98. EP20K1000E f_{MAX} ESB Timing Microparameters							
Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 99. EP20K1000E f_{MAX} Routing Delays							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{F1-4}		0.27		0.27		0.27	ns
t_{F5-20}		1.45		1.63		1.75	ns
t_{F20+}		4.15		4.33		4.97	ns

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 101. EP20K1000E External Timing Parameters							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{INSU}	2.70		2.84		2.97		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{INSUPLL}$	1.64		2.09		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns

Table 104. EP20K1500E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 105. EP20K1500E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.28		0.28		0.28	ns
t_{F5-20}		1.36		1.50		1.62	ns
t_{F20+}		4.43		4.48		5.07	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.47		3.68		3.99		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{XZBIDIR}$		6.91		7.62		8.38	ns
$t_{ZXBIDIR}$		6.91		7.62		8.38	ns
$t_{INSUBIDIRPLL}$	3.05		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.67	0.50	2.99			ns
$t_{XZBIDIRPLL}$		3.41		3.80			ns
$t_{ZXBIDIRPLL}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		–0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		–0.24		–0.23		–0.19	ns
SSTL-3 Class I		–0.32		–0.21		–0.47	ns
SSTL-3 Class II		–0.08		0.03		–0.23	ns
SSTL-2 Class I		–0.17		–0.06		–0.32	ns
SSTL-2 Class II		–0.16		–0.05		–0.31	ns
LVDS		–0.12		–0.12		–0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns