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Intel - EP20K100FC144-1X Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	93
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100fc144-1x

Table 5. APEX 20K FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 *(3)*	
EP20K400E				488 *(3)*	
EP20K600E				508 *(3)*	588
EP20K1000E				508 *(3)*	708
EP20K1500E					808

Notes to Tables 4 and 5:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

Table 7. APEX 20K FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

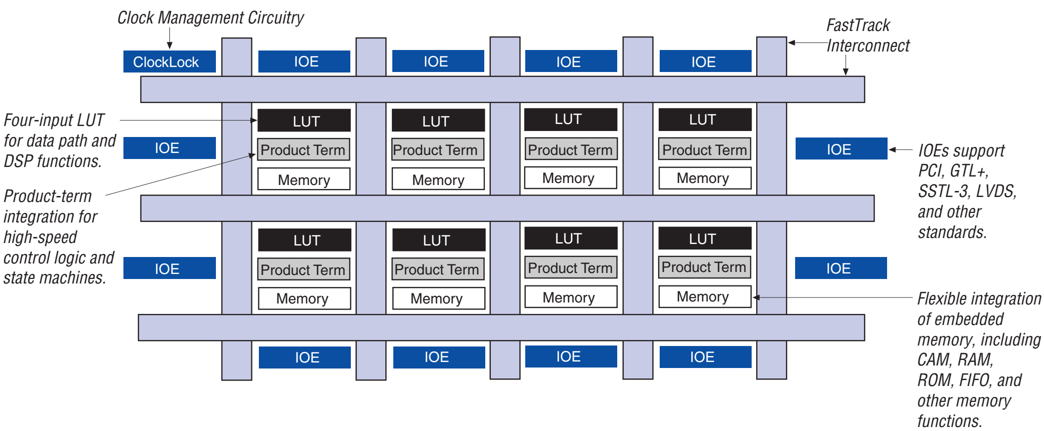
Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

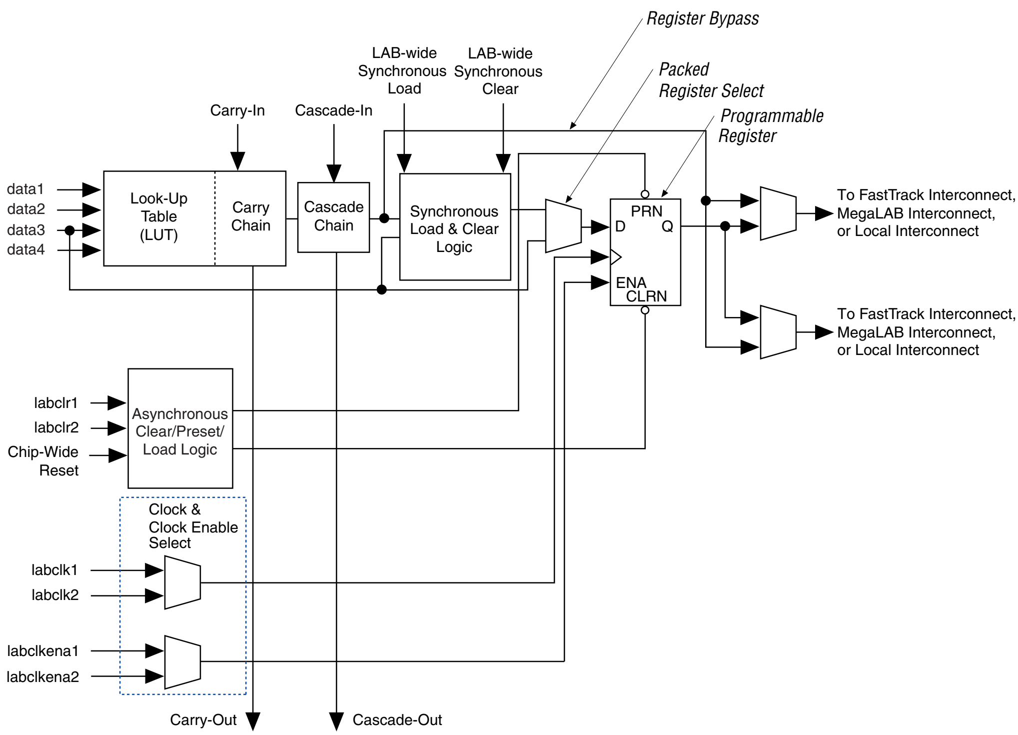
Figure 1. APEX 20K Device Block Diagram



Logic Element

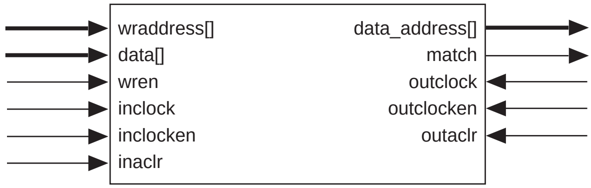
The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Figure 23. APEX 20KE CAM Block Diagram



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't-care" bit can be used as a mask for CAM comparisons; any bit set to "don't-care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address `12`, the ESB output is `12`. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address `12`, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't-care" bits are used, a third clock cycle is required.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

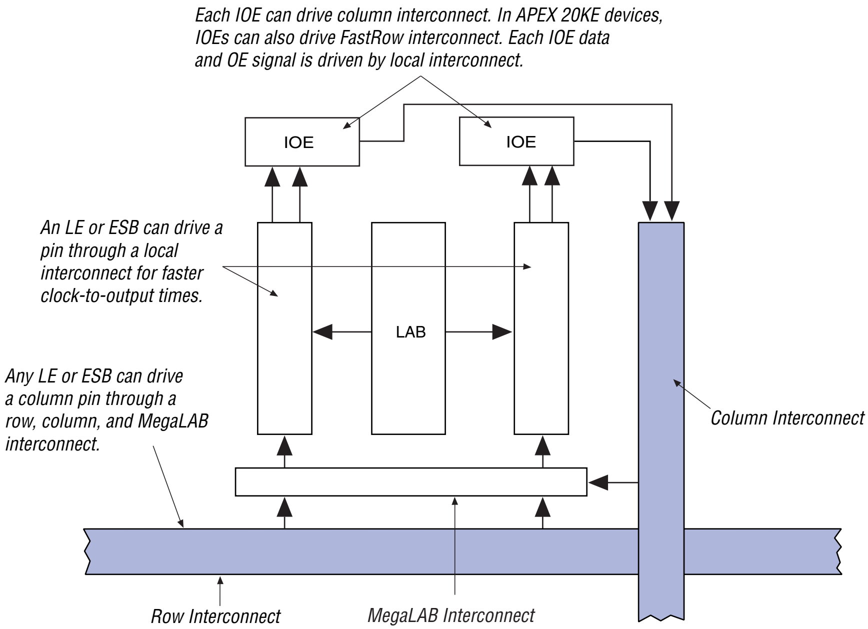
Table 11. APEX 20KE Programmable Delay Chains

Programmable Delays	Quartus II Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2) Note (1)

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f_{VCO} (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	`Clock0` PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	`Clock1` PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external `clock0` output	3.3-V LVTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
f_{CLOCK1_EXT}	Output clock frequency for external `clock1` output	3.3-V LVTTL	20	245	20	226	MHz
		2.5-V LVTTL	20	234	20	221	MHz
		1.8-V LVTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

Table 30. APEX 20KE Device Capacitance Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 27 through 30:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

Vin	Max. Duty Cycle
4.0V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the V_{IH}, V_{IL}, V_{OH}, V_{OL}, and I_I parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance on APEX 20K devices.

Table 31. APEX 20K f_{MAX} Timing Parameters (Part 2 of 2)	
Symbol	**Parameter**
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay
t_{F1-4}	Fanout delay using local interconnect
t_{F5-20}	Fanout delay using MegaLab Interconnect
t_{F20+}	Fanout delay using FastTrack Interconnect
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Tables 32 and 33 describe APEX 20K external timing parameters.

Table 32. APEX 20K External Timing Parameters Note (1)	
Symbol	**Clock Parameter**
t_{INSU}	Setup time with global clock at IOE register
t_{INH}	Hold time with global clock at IOE register
t_{OUTCO}	Clock-to-output delay with global clock at IOE register

Table 33. APEX 20K External Bidirectional Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate = off	C1 = 10 pF

Note to Tables 32 and 33:
(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the f_{MAX} timing model.

Table 34. APEX 20KE LE Timing Microparameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 35. APEX 20KE ESB Timing Microparameters

Symbol	Parameter
t_{ESBARC}	ESB Asynchronous read cycle time
t_{ESBSRC}	ESB Synchronous read cycle time
t_{ESBAWC}	ESB Asynchronous write cycle time
t_{ESBSWC}	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
t_{ESBWEH}	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.6		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 41. EP20K200 f_{MAX} Timing Parameters							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Units**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.7		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.4		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 42. EP20K400 f_{MAX} Timing Parameters							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Units**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{SU}	0.1		0.3		0.6		ns
t_{H}	0.5		0.8		0.9		ns
t_{CO}		0.1		0.4		0.6	ns
t_{LUT}		1.0		1.2		1.4	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
t_{F1-4}		0.4		0.5		0.6	ns
t_{F5-20}		2.6		2.8		2.9	ns
t_{F20+}		3.7		3.8		3.9	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.5		0.6		0.8		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.5		1.9		2.2		ns
t_{ESBRP}	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 57. EP20K60E f_{MAX} Routing Delays							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.26		0.30	ns
t_{F5-20}		1.45		1.58		1.79	ns
t_{F20+}		1.96		2.14		2.45	ns

Table 58. EP20K60E Minimum Pulse Width Timing Parameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.00		2.50		2.75		ns
t_{CL}	2.00		2.50		2.75		ns
t_{CLRP}	0.20		0.28		0.41		ns
t_{PREP}	0.20		0.28		0.41		ns
t_{ESBCH}	2.00		2.50		2.75		ns
t_{ESBCL}	2.00		2.50		2.75		ns
t_{ESBWP}	1.29		1.80		2.66		ns
t_{ESBRP}	1.04		1.45		2.14		ns

Table 59. EP20K60E External Timing Parameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.03		2.12		2.23		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

Table 62. EP20K100E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.61		1.84		1.97	ns
t_{ESBSRC}		2.57		2.97		3.20	ns
t_{ESBAWC}		0.52		4.09		4.39	ns
t_{ESBSWC}		3.17		3.78		4.09	ns
$t_{ESBWASU}$	0.56		6.41		0.63		ns
t_{ESBWAH}	0.48		0.54		0.55		ns
$t_{ESBWDSU}$	0.71		0.80		0.81		ns
t_{ESBWDH}	.048		0.54		0.55		ns
$t_{ESBRASU}$	1.57		1.75		1.87		ns
t_{ESBRAH}	0.00		0.00		0.20		ns
$t_{ESBWESU}$	1.54		1.72		1.80		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.16		-0.20		-0.20		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.12		0.08		0.13		ns
$t_{ESBRADDRSU}$	0.17		0.15		0.19		ns
$t_{ESBDATACO1}$		1.20		1.39		1.52	ns
$t_{ESBDATACO2}$		2.54		2.99		3.22	ns
t_{ESBDD}		3.06		3.56		3.85	ns
t_{PD}		1.73		2.02		2.20	ns
$t_{PTERMSU}$	1.11		1.26		1.38		ns
$t_{PTERMCO}$		1.19		1.40		1.08	ns

Table 63. EP20K100E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.29	ns
t_{F5-20}		1.04		1.26		1.52	ns
t_{F20+}		1.12		1.36		1.86	ns

Table 76. EP20K200E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.44		2.65		ns
t_{CL}	1.36		2.44		2.65		ns
t_{CLRP}	0.18		0.19		0.21		ns
t_{PREP}	0.18		0.19		0.21		ns
t_{ESBCH}	1.36		2.44		2.65		ns
t_{ESBCL}	1.36		2.44		2.65		ns
t_{ESBWP}	1.18		1.48		1.76		ns
t_{ESBRP}	0.95		1.17		1.41		ns

Table 77. EP20K200E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.24		2.35		2.47		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{INSUPLL}$	2.13		2.07		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.01	0.50	3.36	-	-	ns

Table 80. EP20K300E f_{MAX} ESB Timing Microparameters							
Symbol	**-1**		**-2**		**-3**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ESBARC}		1.79		2.44		3.25	ns
t_{ESBSRC}		2.40		3.12		4.01	ns
t_{ESBAWC}		3.41		4.65		6.20	ns
t_{ESBSWC}		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
t_{ESBDD}		3.41		4.65		6.20	ns
t_{PD}		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

Table 81. EP20K300E f_{MAX} Routing Delays							
Symbol	**-1**		**-2**		**-3**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{F1-4}		0.22		0.24		0.26	ns
t_{F5-20}		1.33		1.43		1.58	ns
t_{F20+}		3.63		3.93		4.35	ns

Table 82. EP20K300E Minimum Pulse Width Timing Parameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.19		0.26		0.35		ns
t_{PREP}	0.19		0.26		0.35		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.25		1.71		2.28		ns
t_{ESBRP}	1.01		1.38		1.84		ns

Table 83. EP20K300E External Timing Parameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.31		2.44		2.57		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.29	2.00	5.82	2.00	6.24	ns
$t_{INSUPLL}$	1.76		1.85		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.65	0.50	2.95	-	-	ns

Table 84. EP20K300E External Bidirectional Timing Parameters							
Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.77		2.85		3.11		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.29	2.00	5.82	2.00	6.24	ns
$t_{XZBIDIR}$		7.59		8.30		9.09	ns
$t_{ZXBIDIR}$		7.59		8.30		9.09	ns
$t_{INSUBIDIRPLL}$	2.50		2.76		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.65	0.50	2.95	-	-	ns
$t_{XZBIDIRPLL}$		5.00		5.43		-	ns
$t_{ZXBIDIRPLL}$		5.00		5.43		-	ns

Tables 85 through 90 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

Table 85. EP20K400E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.23		0.23		ns
t_H	0.23		0.23		0.23		ns
t_{CO}		0.25		0.29		0.32	ns
t_{LUT}		0.70		0.83		1.01	ns

Table 110. Selectable I/O Standard Output Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.09		0.10	ns
1.8 V		2.49		2.98		3.03	ns
PCI		–0.03		0.17		0.16	ns
GTL+		0.75		0.75		0.76	ns
SSTL-3 Class I		1.39		1.51		1.50	ns
SSTL-3 Class II		1.11		1.23		1.23	ns
SSTL-2 Class I		1.35		1.48		1.47	ns
SSTL-2 Class II		1.00		1.12		1.12	ns
LVDS		–0.48		–0.48		–0.48	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to V_{CCIO} by a built-in weak pull-up resistor.