# Altera - EP20K100QC208-2 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 416 |
| Number of Logic Elements/Cells | 4160 |
| Total RAM Bits | 53248 |
| Number of I/O | 159 |
| Number of Gates | 263000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k100qc208-2 |

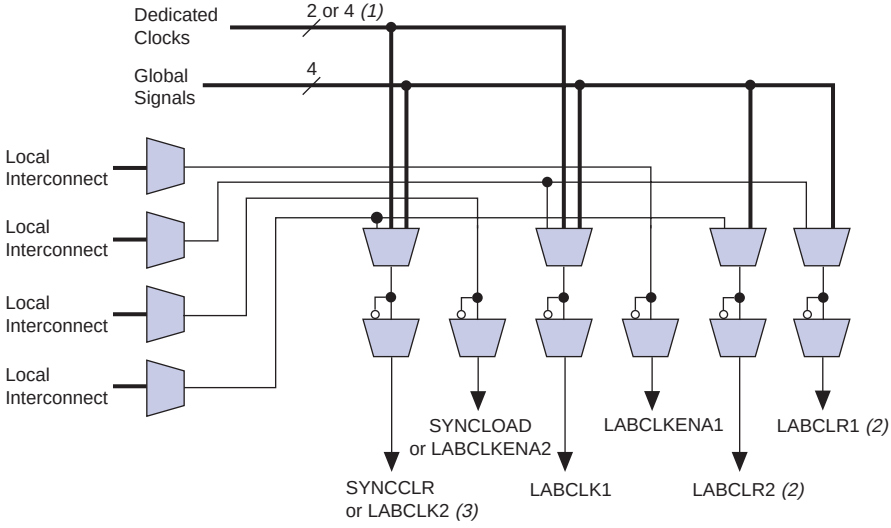
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

***Figure 4. LAB Control Signal Generation***



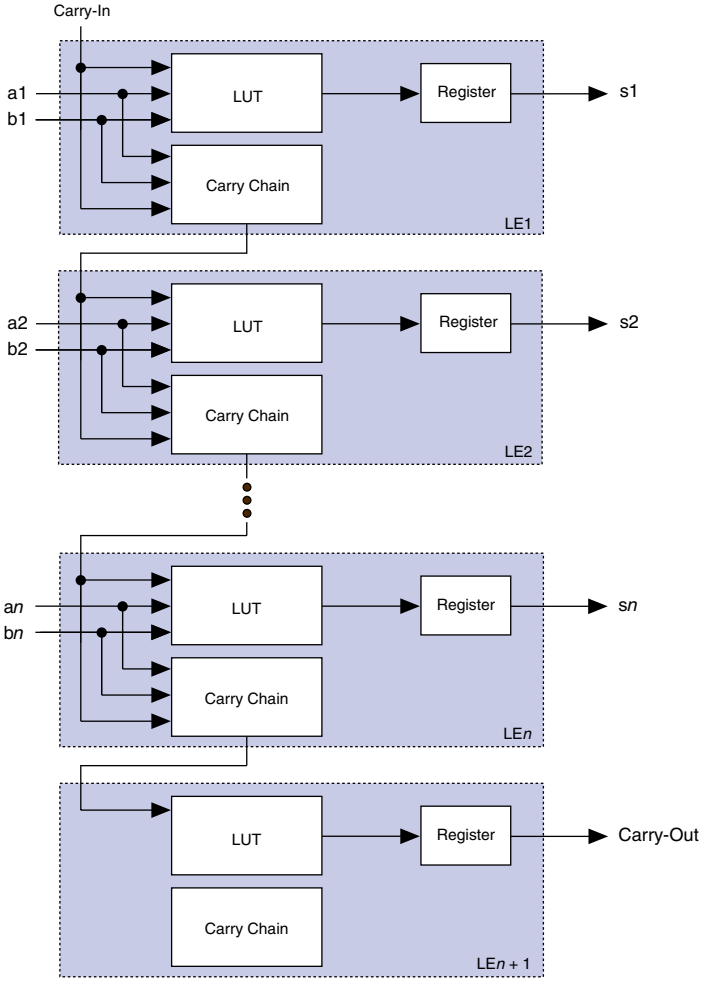

*Notes to Figure 4:*

(1) APEX 20KE devices have four dedicated clocks.

(2) The `LABCLR1` and `LABCLR2` signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(3) The `SYNCCLR` signal can be generated by the local interconnect or global signals.

*Figure 6. APEX 20K Carry Chain*



### *Cascade Chain*

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

***Figure 7. APEX 20K Cascade Chain***

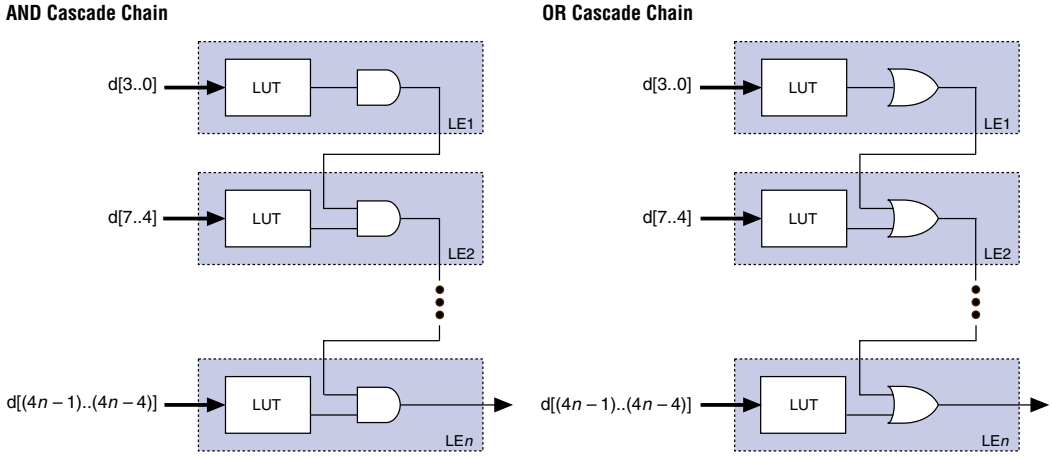


*Figure 12. APEX 20KE FastRow Interconnect*

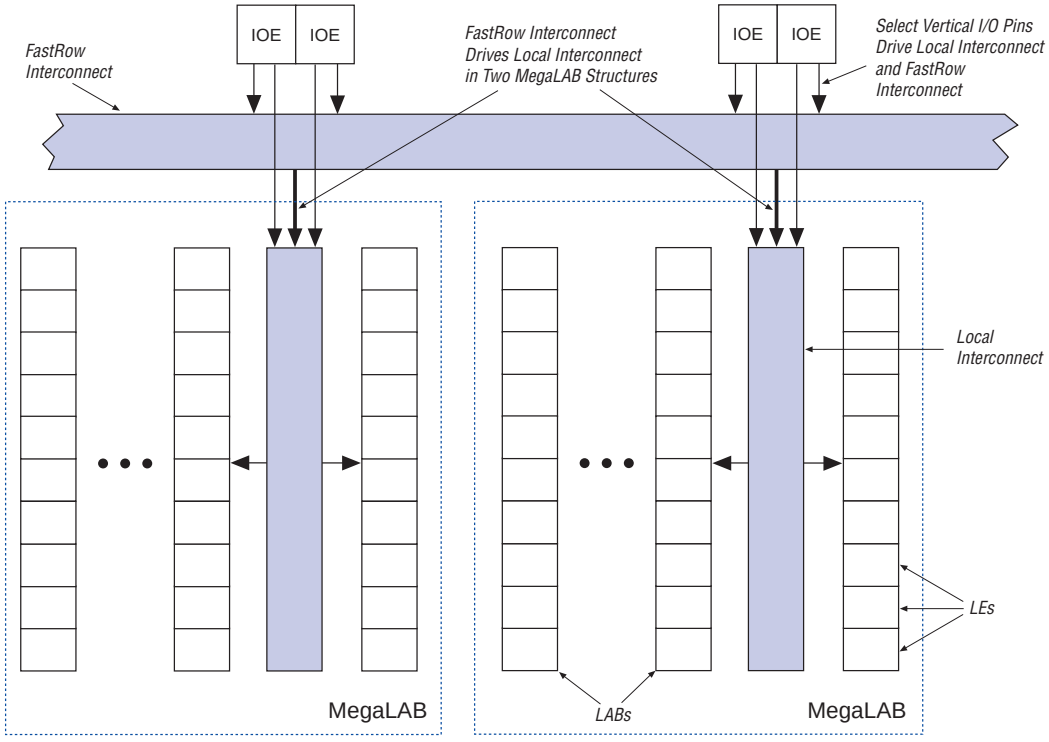
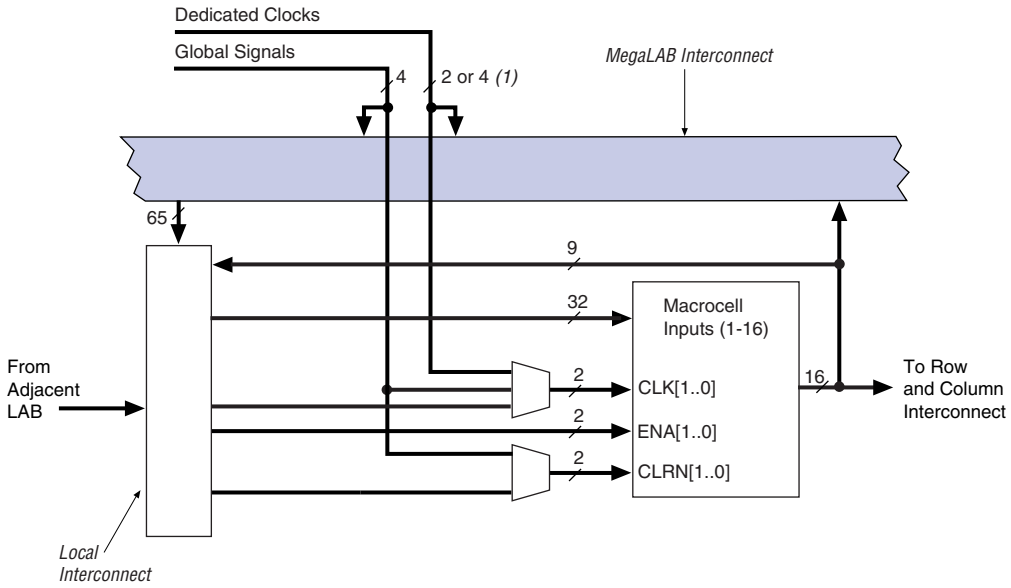



Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

*Figure 13. Product-Term Logic in ESB*




*Note to Figure 13:*
(1) APEX 20KE devices have four dedicated clocks.

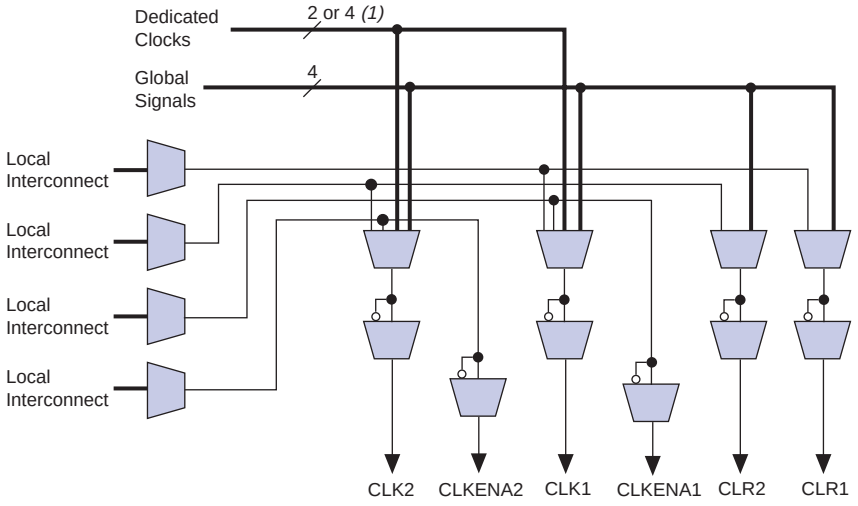
## Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*



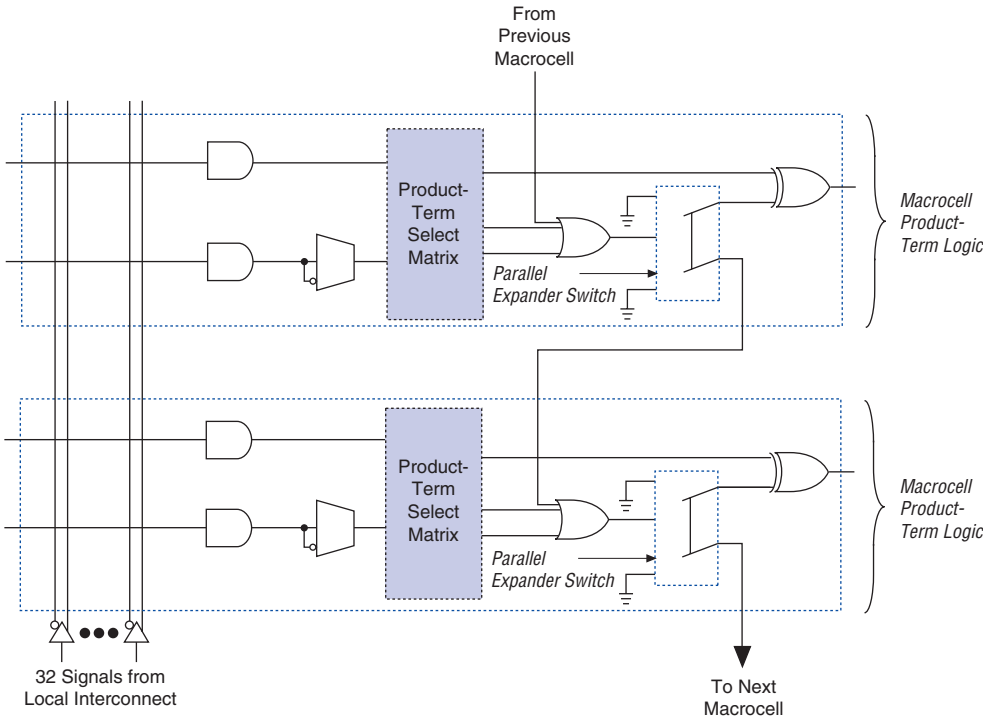

*Note to Figure 15:*
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

*Figure 16. APEX 20K Parallel Expanders*




## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*

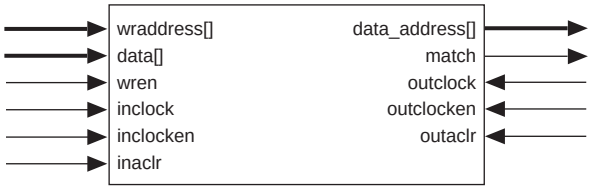
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

*Figure 23. APEX 20KE CAM Block Diagram*




CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't-care" bit can be used as a mask for CAM comparisons; any bit set to "don't-care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address `12`, the ESB output is `12`. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address `12`, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

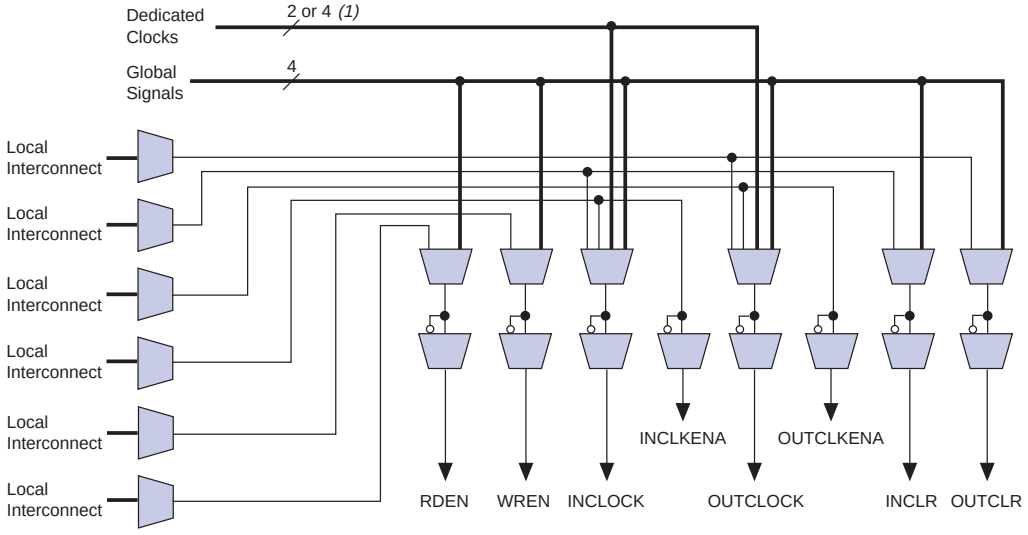
CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't-care" bits are used, a third clock cycle is required.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

***Figure 24. ESB Control Signal Generation***




*Note to Figure 24:*
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

*Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions* *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4), (5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4), (5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3), (6)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(9)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 1.7 | | | V |

*Table 26. APEX 20K 5.0-V Tolerant Device Capacitance* *Notes (2), (14)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 23 through 26:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 2.5 V, and $V_{CCIO}$ = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when $V_{CCIO}$ and $V_{CCINT}$ meet the relationship shown in Figure 33 on page 68.
(10) The $I_{OH}$ parameter refers to high-level TTL, PCI or CMOS output current.
(11) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

*Table 27. APEX 20KE Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 2.5 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Note to Tables 32 and 33:*
(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the $f_{MAX}$ timing model.

*Table 34. APEX 20KE LE Timing Microparameters*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in to data-out |

*Table 35. APEX 20KE ESB Timing Microparameters*

| Symbol | Parameter |
|---|---|
| $t_{ESBARC}$ | ESB Asynchronous read cycle time |
| $t_{ESBSRC}$ | ESB Synchronous read cycle time |
| $t_{ESBAWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBSWC}$ | ESB Synchronous write cycle time |
| $t_{ESBWASU}$ | ESB write address setup time with respect to WE |
| $t_{ESBWAH}$ | ESB write address hold time with respect to WE |
| $t_{ESBWDSU}$ | ESB data setup time with respect to WE |
| $t_{ESBWDH}$ | ESB data hold time with respect to WE |
| $t_{ESBRASU}$ | ESB read address setup time with respect to RE |
| $t_{ESBRAH}$ | ESB read address hold time with respect to RE |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBWEH}$ | ESB WE hold time after clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBWADDRSU}$ | ESB write address setup time before clock when using input registers |
| $t_{ESBRADDRSU}$ | ESB read address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB Macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB Macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB Macrocell register clock-to-output delay |

*Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

*Table 51. EP20K30E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

*Table 52. EP20K30E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CLRP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{PREP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{ESBCH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBCL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBWP}$ | 1.43 | | 2.01 | | 2.97 | | ns |
| $t_{ESBRP}$ | 1.15 | | 1.62 | | 2.39 | | ns |

*Table 53. EP20K30E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.02 | | 2.13 | | 2.24 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{INSUPLL}$ | 2.11 | | 2.23 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |

*Table 54. EP20K30E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.85 | | 1.77 | | 1.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{XZBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{ZXBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{INSUBIDIRPLL}$ | 4.12 | | 4.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |

*Table 60. EP20K60E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.91 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{XZBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{ZXBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{INSUBIDIRPLL}$ | 3.44 | | 3.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |

Tables 61 through 66 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

*Table 61. EP20K100E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.28 | | 0.34 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

Tables 67 through 72 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

*Table 67. EP20K160E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.25 | | 0.31 | | 0.35 | ns |
| $t_{LUT}$ | | 0.69 | | 0.88 | | 1.12 | ns |

*Table 78. EP20K200E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.81 | | 3.19 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.12 | 2.00 | 5.62 | 2.00 | 6.11 | ns |
| $t_{XZBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{ZXBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{INSUBIDIRPLL}$ | 3.30 | | 3.64 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.01 | 0.50 | 3.36 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |

Tables 79 through 84 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

*Table 79. EP20K300E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.17 | | 0.18 | | ns |
| $t_{H}$ | 0.31 | | 0.33 | | 0.38 | | ns |
| $t_{CO}$ | | 0.28 | | 0.38 | | 0.51 | ns |
| $t_{LUT}$ | | 0.79 | | 1.07 | | 1.43 | ns |

*Table 86. EP20K400E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 1.91 | | 1.99 | ns |
| $t_{ESBSRC}$ | | 2.30 | | 2.66 | | 2.93 | ns |
| $t_{ESBAWC}$ | | 3.09 | | 3.58 | | 3.99 | ns |
| $t_{ESBSWC}$ | | 3.01 | | 3.65 | | 4.05 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.63 | | 0.65 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.77 | | 0.84 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.77 | | 1.86 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.35 | | 1.47 | | 1.61 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.18 | | -0.30 | | -0.27 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | -0.02 | | -0.11 | | -0.03 | | ns |
| $t_{ESBRADDRSU}$ | 0.06 | | -0.01 | | -0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.16 | | 1.40 | | 1.54 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 2.55 | | 2.85 | ns |
| $t_{ESBDD}$ | | 2.73 | | 3.17 | | 3.58 | ns |
| $t_{PD}$ | | 1.57 | | 1.83 | | 2.07 | ns |
| $t_{PTERMSU}$ | 0.92 | | 0.99 | | 1.18 | | ns |
| $t_{PTERMCO}$ | | 1.18 | | 1.43 | | 1.17 | ns |

Tables 97 through 102 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

*Table 97. EP20K1000E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |