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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 416 |
| Number of Logic Elements/Cells | 4160 |
| Total RAM Bits | 53248 |
| Number of I/O | 159 |
| Number of Gates | 263000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k100qc208-3 |

Windows-based PCs, SunSPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP SM) megafunctions
- NativeLink ™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS )

Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Counts (1), (2)

| Device | 144-Pin TQFP | 208-Pin PQFP RQFP | 240-Pin PQFP RQFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| EP20K30E | 92 | 125 | | | | |
| EP20K60E | 92 | 148 | 151 | 196 | | |
| EP20K100 | 101 | 159 | 189 | 252 | | |
| EP20K100E | 92 | 151 | 183 | 246 | | |
| EP20K160E | 88 | 143 | 175 | 271 | | |
| EP20K200 | | 144 | 174 | 277 | | |
| EP20K200E | | 136 | 168 | 271 | 376 | |
| EP20K300E | | | 152 | | 408 | |
| EP20K400 | | | | | 502 | 502 |
| EP20K400E | | | | | 488 | |
| EP20K600E | | | | | 488 | |
| EP20K1000E | | | | | 488 | |
| EP20K1500E | | | | | 488 | |

## LE Operating Modes

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

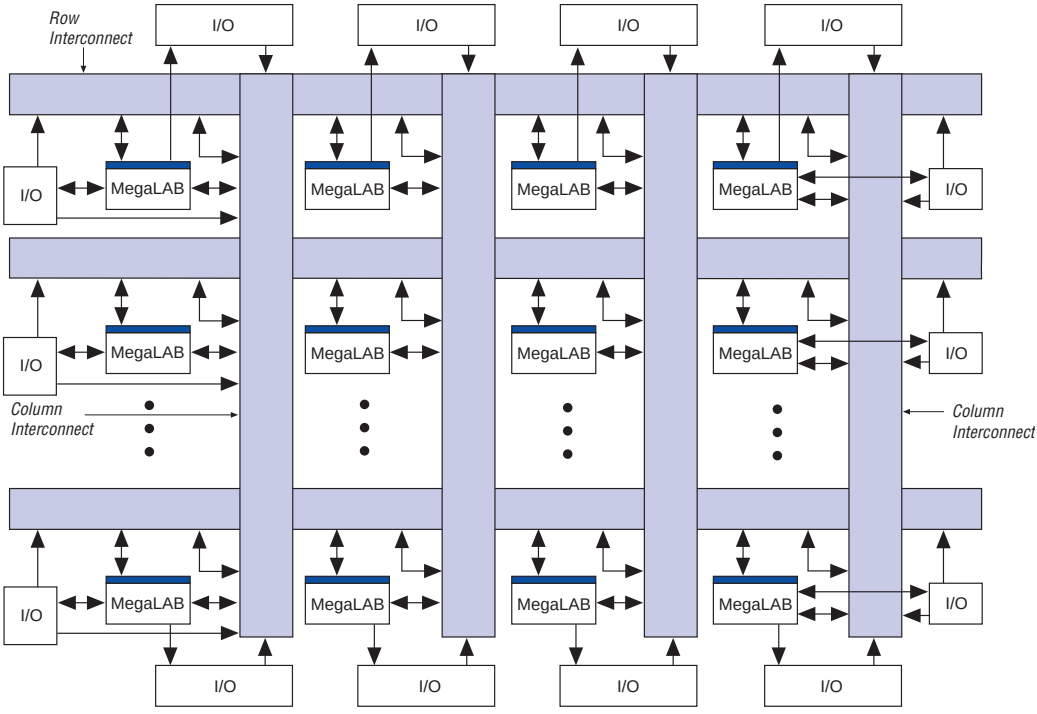
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 9. APEX 20K Interconnect Structure




A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

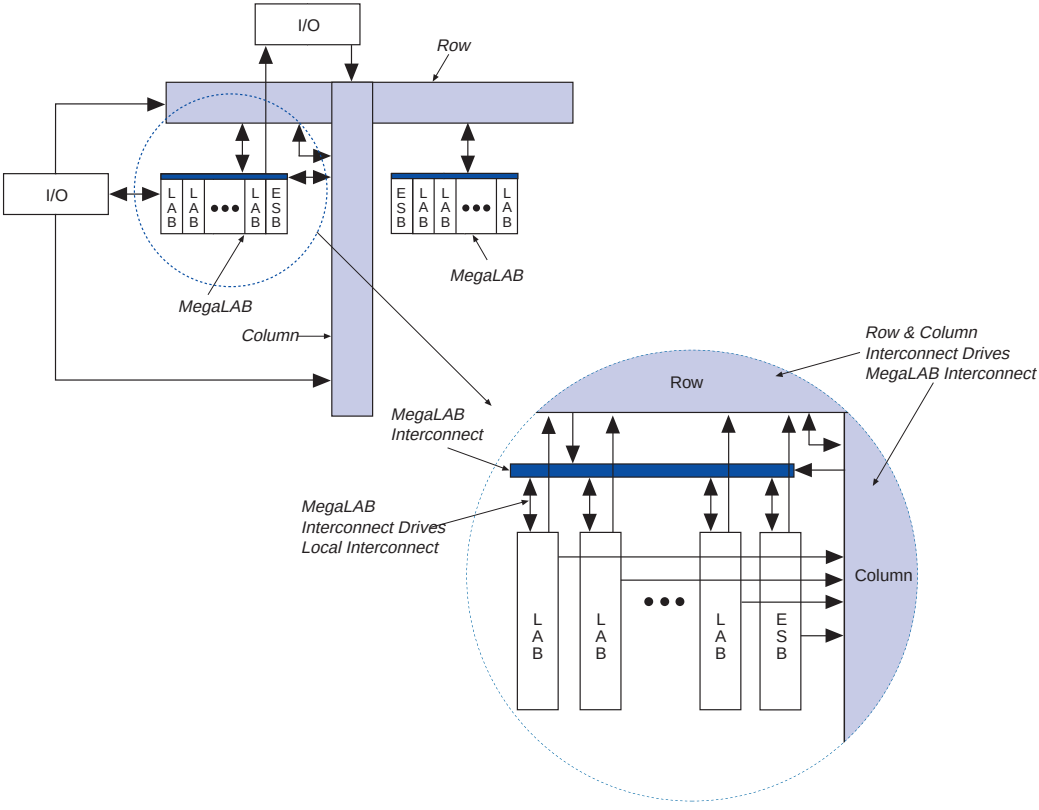
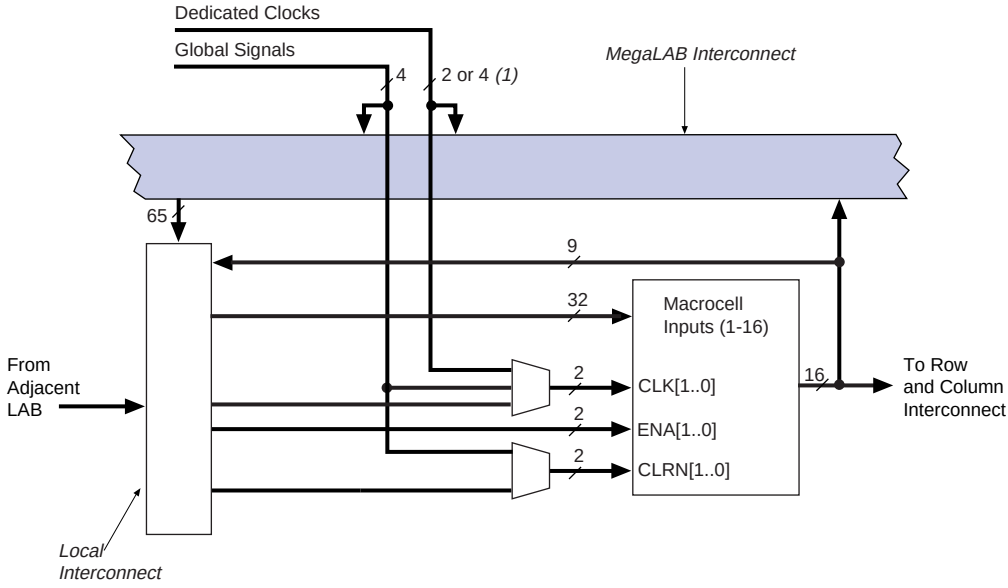


Figure 13. Product-Term Logic in ESB



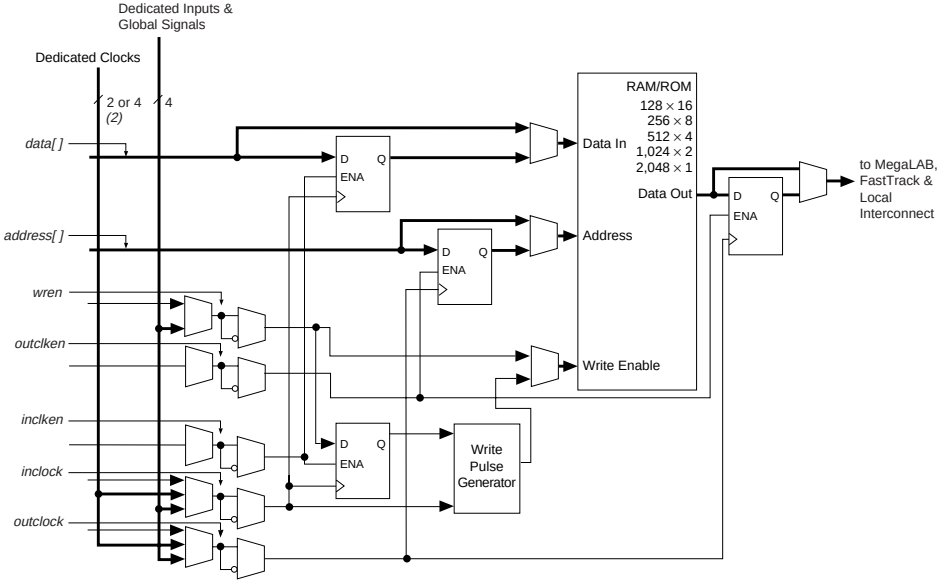

Note to Figure 13:
(1) APEX 20KE devices have four dedicated clocks.

## Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

Figure 22. ESB in Single-Port Mode Note (1)




Notes to Figure 22:

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.

(2) APEX 20KE devices have four dedicated clocks.

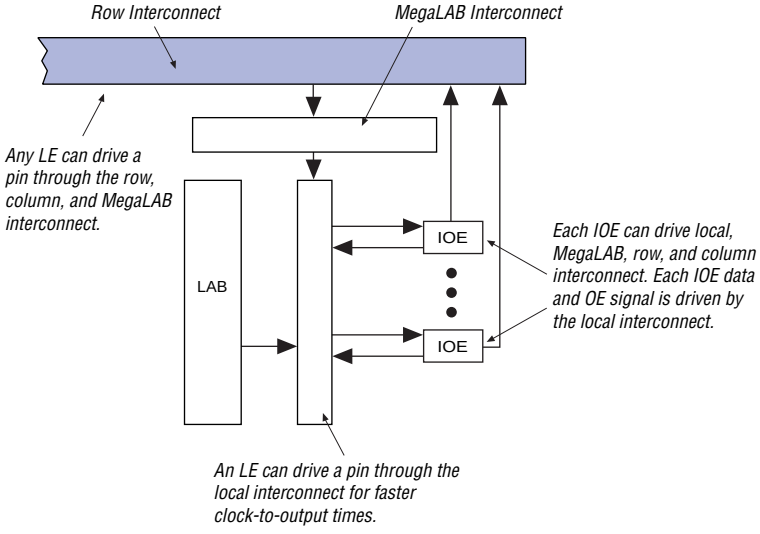
## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27 shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect



For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 14. Multiplication Factor Combinations

| Clock 1 | Clock 2 |
|---|---|
| ×1 | ×1 |
| ×1, ×2 | ×2 |
| ×1, ×2, ×4 | ×4 |

## APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

### External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

### Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where m and k range from 2 to 160, and n and v range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Table 26. APEX 20K 5.0-V Tolerant Device Capacitance Notes (2), (14)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

Notes to Tables 23 through 26:
(1) See the Operating Requirements for Altera Devices Data Sheet
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 2.5 V, and $V_{CCIO}$ = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when $V_{CCIO}$ and $V_{CCINT}$ meet the relationship shown in Figure 33 on page 68.
(10) The $I_{OH}$ parameter refers to high-level TTL, PCI or CMOS output current.
(11) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 27. APEX 20KE Device Absolute Maximum Ratings Note (1)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground (2) | –0.5 | 2.5 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

1 For DC Operating Specifications on APEX 20KE I/O standards, please refer to Application Note 117 (Using Selectable I/O Standards in Altera Devices).

Table 30. APEX 20KE Device Capacitance Note (15)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

Notes to Tables 27 through 30:

(1) See the Operating Requirements for Altera Devices Data Sheet
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

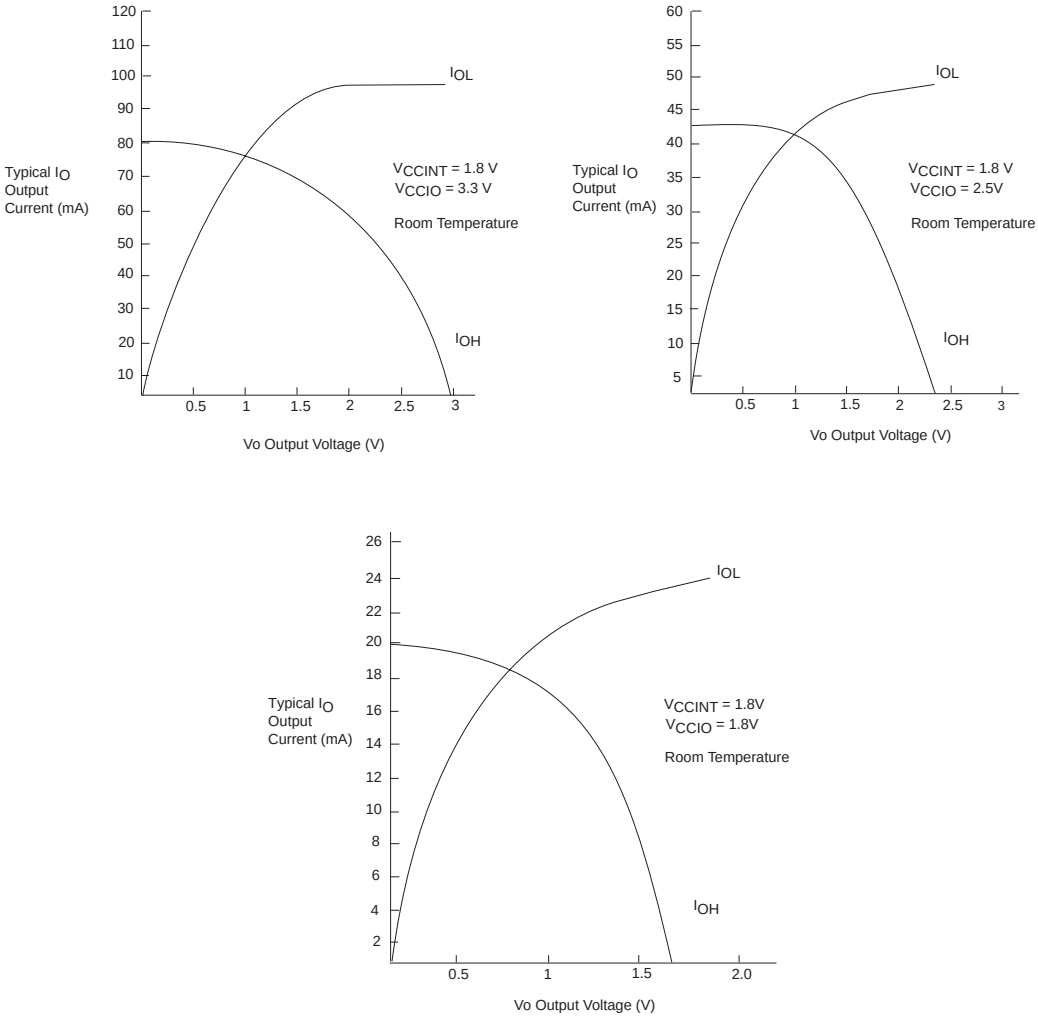
| Vin | Max. Duty Cycle |
|---|---|
| 4.0V | 100% (DC) |
| 4.1 | 90% |
| 4.2 | 50% |
| 4.3 | 30% |
| 4.4 | 17% |
| 4.5 | 10% |

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to Application Note 117 (Using Selectable I/O Standards in Altera Devices) for the $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, and $I_I$ parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices Note (1)




Note to Figure 35:
(1) These are transient (AC) currents.

# Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 39. ESB Synchronous Timing Waveforms

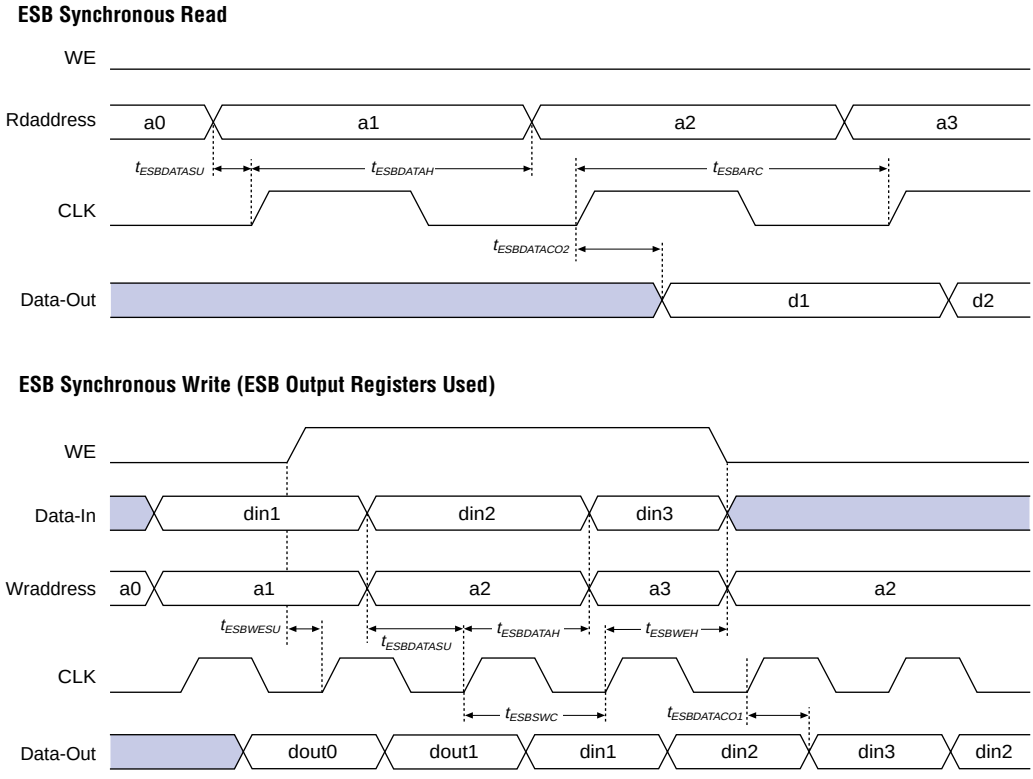
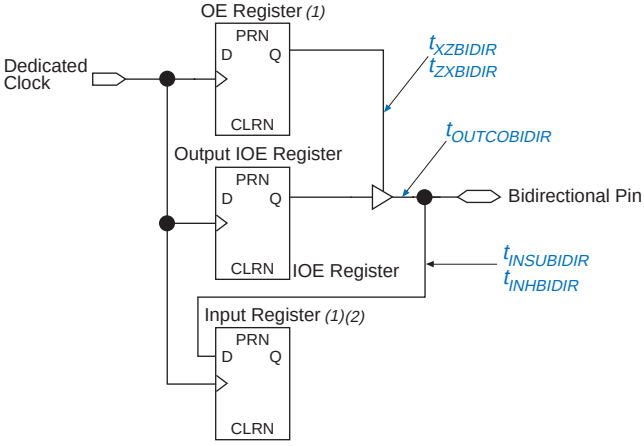



Figure 40 shows the timing model for bidirectional I/O pin timing.

Figure 40. Synchronous Bidirectional Pin External Timing




Notes to Figure 40:

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the $f_{MAX}$ timing parameters shown in Figure 36 on page 68.

Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 1 of 2)

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{ESBRC}$ | ESB Asynchronous read cycle time |
| $t_{ESBWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |