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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	416
Number of Logic Elements/Cells	4160
Total RAM Bits	53248
Number of I/O	159
Number of Gates	263000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k100qi208-2

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock® feature reducing clock delay and skew
  - ClockBoost® feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance (t_{CO} + t_{SU}) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - Programmable clamp to V_{CCIO}
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
  - FineLine BGA® packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus® II development system for

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

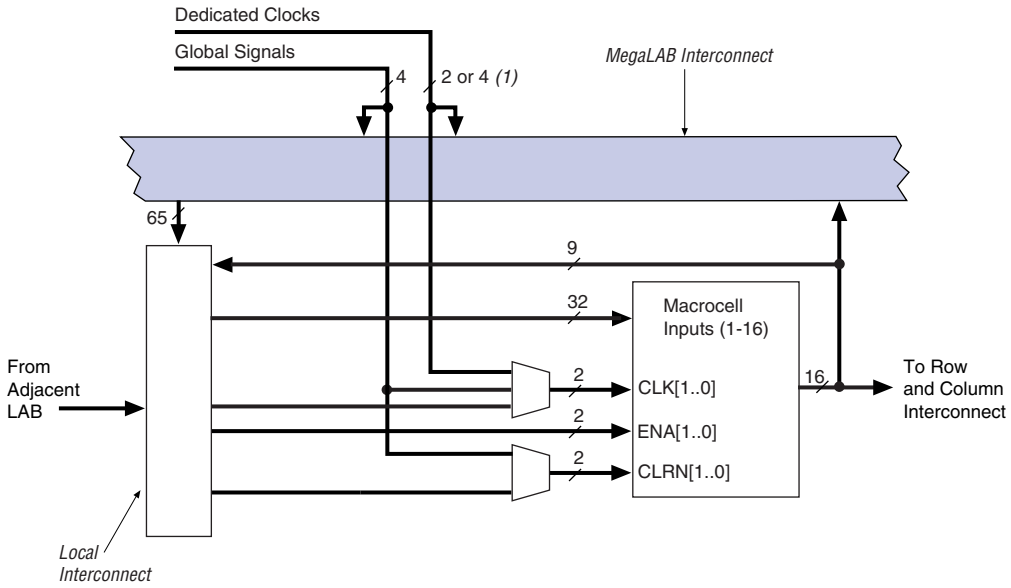
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 13. Product-Term Logic in ESB



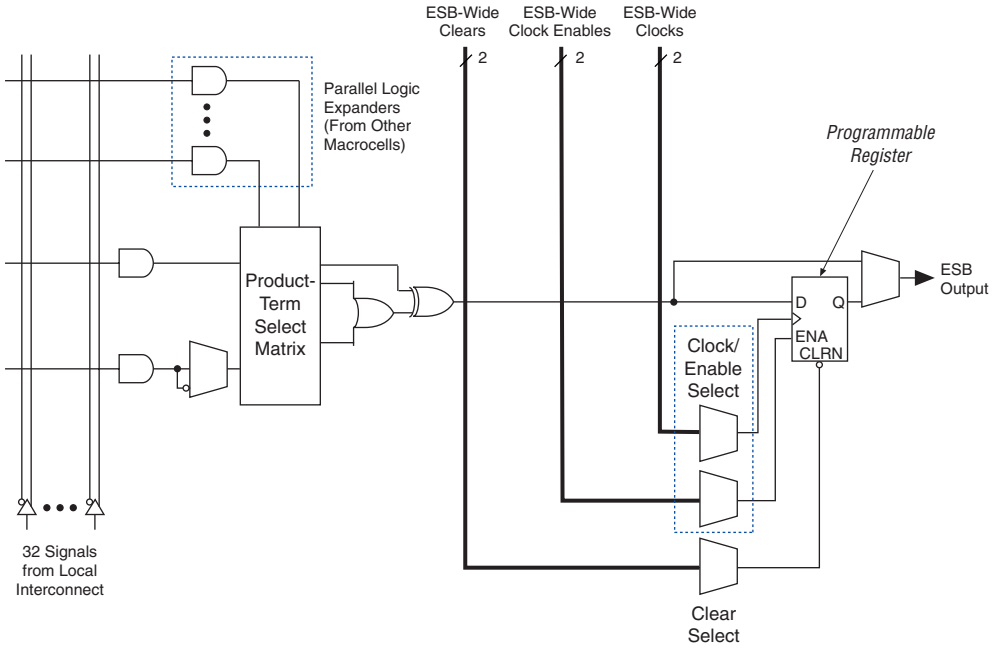
Note to Figure 13:
(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

Figure 14. APEX 20K Macrocell



For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

Table 11. APEX 20KE Programmable Delay Chains

Programmable Delays	Quartus II Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support

V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

Notes to Table 12:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V V_{CCINT} level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

Table 13. APEX 20KE MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signals (V)				Output Signals (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓	*(2)*			✓ *(3)*	

Notes to Table 13:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

(3) When V_{CCIO} = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock *(5)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:

(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)*		25,000 *(2)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock *(3)*		10	µs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock *(4)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

Table 19. APEX 20K JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions *(1)*	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 19:
(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) *(2)*
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 21:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

Figure 31. APEX 20K JTAG Waveforms

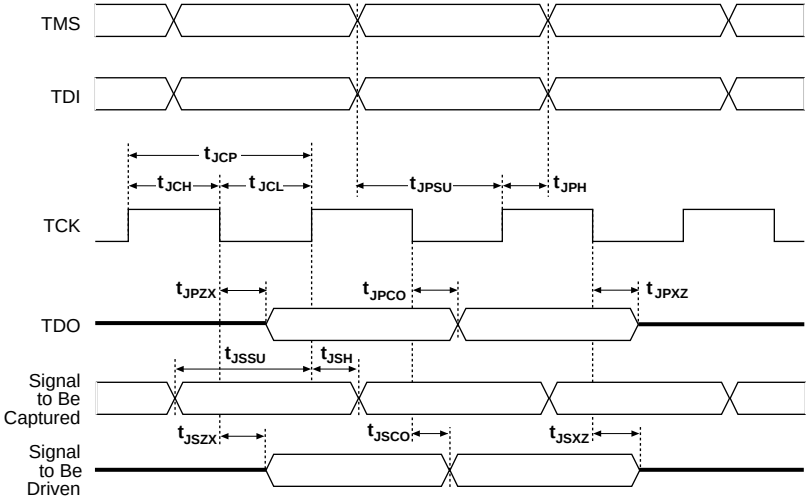
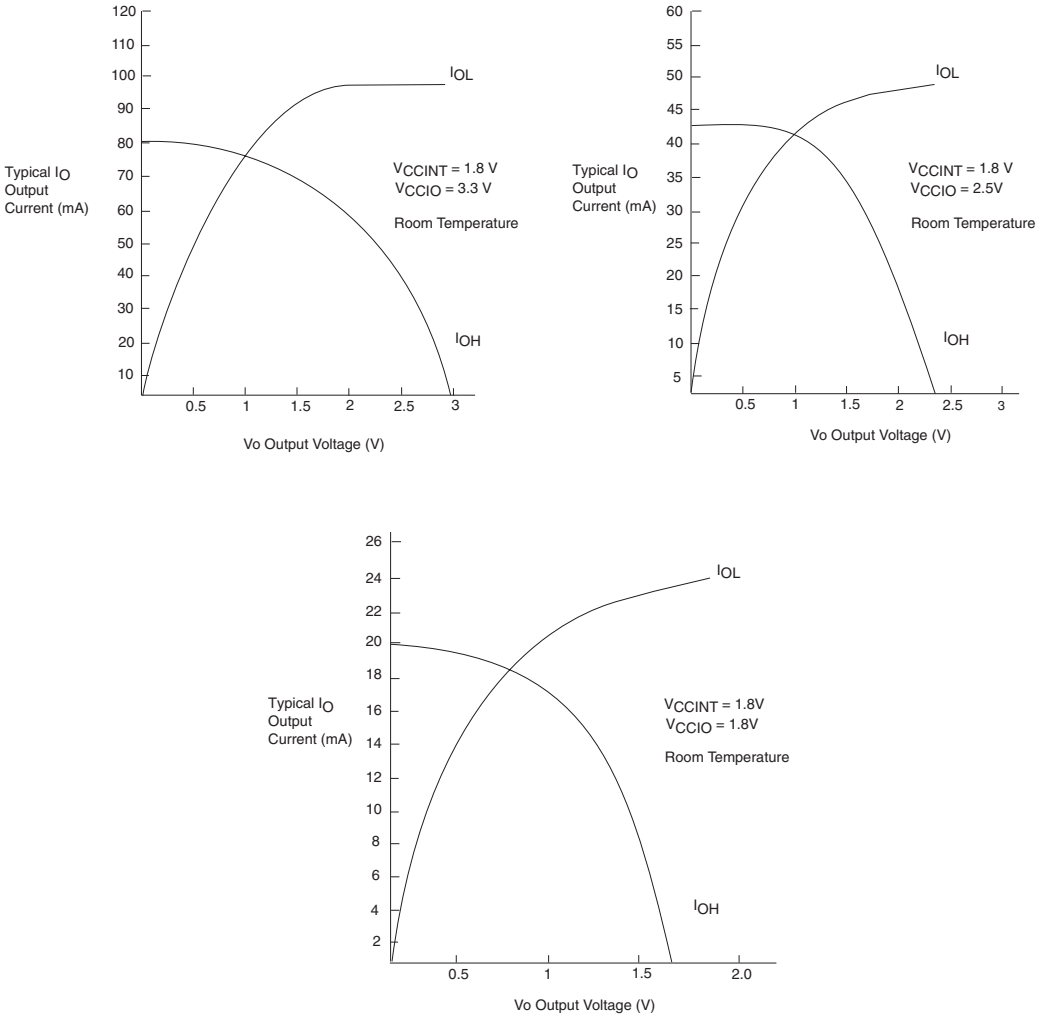


Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(11)*			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(11)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(11)*			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(11)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(11)*			0.7	V
I_I	Input pin leakage current	V_I = 5.75 to –0.5 V	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 5.75 to –0.5 V	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade *(12)*		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades *(12)*		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(13)*	20		50	W
		V_{CCIO} = 2.375 V *(13)*	30		80	W

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices *Note (1)*



Note to Figure 35:
(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Note to Tables 32 and 33:
(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the f_{MAX} timing model.

Table 34. APEX 20KE LE Timing Microparameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 35. APEX 20KE ESB Timing Microparameters

Symbol	Parameter
t_{ESBARC}	ESB Asynchronous read cycle time
t_{ESBSRC}	ESB Synchronous read cycle time
t_{ESBAWC}	ESB Asynchronous write cycle time
t_{ESBSWC}	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
t_{ESBWEH}	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

Table 36. APEX 20KE Routing Timing Microparameters Note (1)	
Symbol	**Parameter**
t_{F1-4}	Fanout delay using Local Interconnect
t_{F5-20}	Fanout delay estimate using MegaLab Interconnect
t_{F20+}	Fanout delay estimate using FastTrack Interconnect

Note to Table 36:

(1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 37. APEX 20KE Functional Timing Microparameters	
Symbol	**Parameter**
TCH	Minimum clock high time from clock pin
TCL	Minimum clock low time from clock pin
TCLRP	LE clear Pulse Width
TPREP	LE preset pulse width
TESBCH	Clock high time for ESB
TESBCL	Clock low time for ESB
TESBWP	Write pulse width
TESBRP	Read pulse width

Tables 38 and 39 describe the APEX 20KE external timing parameters.

Table 38. APEX 20KE External Timing Parameters Note (1)		
Symbol	**Clock Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF

Table 52. EP20K30E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	0.55		0.78		1.15		ns
t_{CL}	0.55		0.78		1.15		ns
t_{CLRP}	0.22		0.31		0.46		ns
t_{PREP}	0.22		0.31		0.46		ns
t_{ESBCH}	0.55		0.78		1.15		ns
t_{ESBCL}	0.55		0.78		1.15		ns
t_{ESBWP}	1.43		2.01		2.97		ns
t_{ESBRP}	1.15		1.62		2.39		ns

Table 53. EP20K30E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.02		2.13		2.24		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{INSUPLL}$	2.11		2.23		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.88	-	-	ns

Table 54. EP20K30E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.85		1.77		1.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{XZBIDIR}$		7.48		8.46		9.83	ns
$t_{ZXBIDIR}$		7.48		8.46		9.83	ns
$t_{INSUBIDIRPLL}$	4.12		4.24		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.60	0.50	2.88	-	-	ns
$t_{XZBIDIRPLL}$		5.21		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.21		5.99		-	ns

Tables 55 through 60 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

Table 55. EP20K60E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.17		0.15		0.16		ns
t_{H}	0.32		0.33		0.39		ns
t_{CO}		0.29		0.40		0.60	ns
t_{LUT}		0.77		1.07		1.59	ns

Table 86. EP20K400E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		1.91		1.99	ns
t_{ESBSRC}		2.30		2.66		2.93	ns
t_{ESBAWC}		3.09		3.58		3.99	ns
t_{ESBSWC}		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
t_{ESBWAH}	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
t_{ESBWDH}	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
t_{ESBDD}		2.73		3.17		3.58	ns
t_{PD}		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

Table 102. EP20K1000E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.22		3.33		3.51		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{XZBIDIR}$		6.31		7.09		7.76	ns
$t_{ZXBIDIR}$		6.31		7.09		7.76	ns
$t_{INSUBIDIRPLL}$	3.25		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.25	0.50	2.99			ns
$t_{XZBIDIRPLL}$		2.81		3.80			ns
$t_{ZXBIDIRPLL}$		2.81		3.80			ns

Tables 103 through 108 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

Table 103. EP20K1500E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.32		0.33	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 104. EP20K1500E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 105. EP20K1500E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.28		0.28		0.28	ns
t_{F5-20}		1.36		1.50		1.62	ns
t_{F20+}		4.43		4.48		5.07	ns

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.