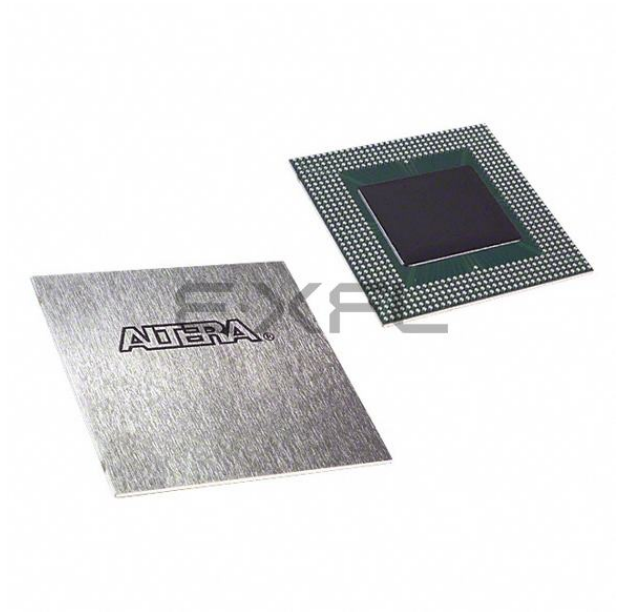
# Intel - EP20K1500EBC652-1 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 5184 |
| Number of Logic Elements/Cells | 51840 |
| Total RAM Bits | 442368 |
| Number of I/O | 488 |
| Number of Gates | 2392000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 652-BGA |
| Supplier Device Package | 652-BGA (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k1500ebc652-1 |

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS )

*Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count* *Notes (1), (2)*

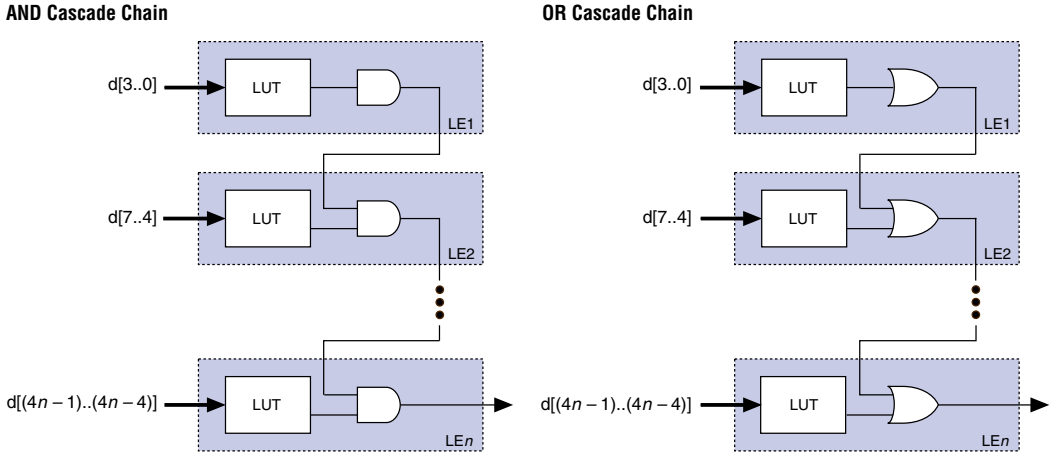
| Device | 144-Pin TQFP | 208-Pin PQFP RQFP | 240-Pin PQFP RQFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| EP20K30E | 92 | 125 | | | | |
| EP20K60E | 92 | 148 | 151 | 196 | | |
| EP20K100 | 101 | 159 | 189 | 252 | | |
| EP20K100E | 92 | 151 | 183 | 246 | | |
| EP20K160E | 88 | 143 | 175 | 271 | | |
| EP20K200 | | 144 | 174 | 277 | | |
| EP20K200E | | 136 | 168 | 271 | 376 | |
| EP20K300E | | | 152 | | 408 | |
| EP20K400 | | | | | 502 | 502 |
| EP20K400E | | | | | 488 | |
| EP20K600E | | | | | 488 | |
| EP20K1000E | | | | | 488 | |
| EP20K1500E | | | | | 488 | |

### *Cascade Chain*

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

***Figure 7. APEX 20K Cascade Chain***



The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

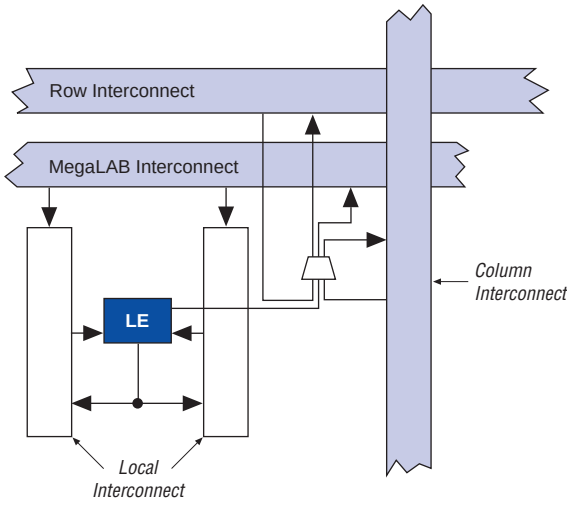
## FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

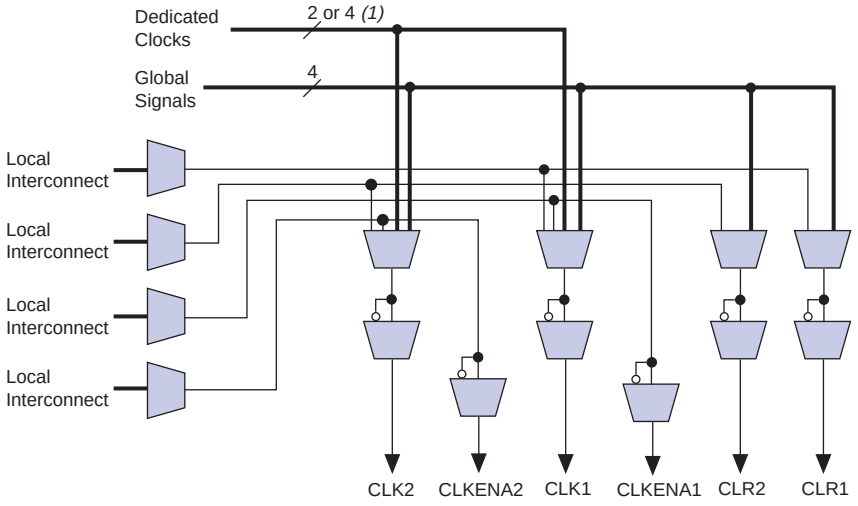
*Figure 11. Driving the FastTrack Interconnect*




APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABS in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*



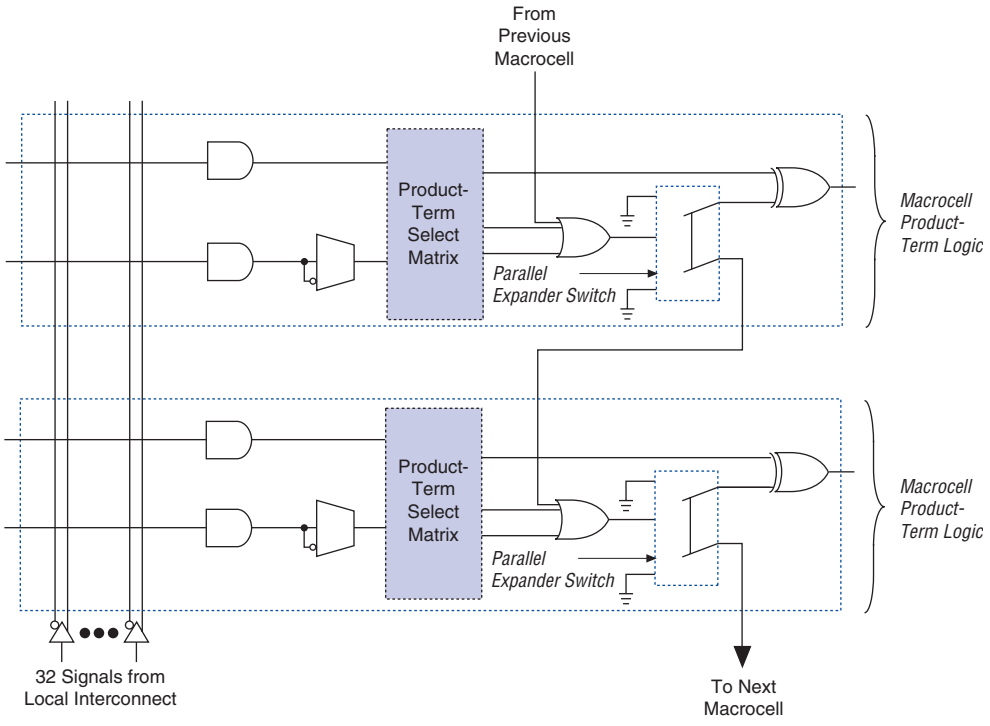

*Note to Figure 15:*
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

*Figure 16. APEX 20K Parallel Expanders*

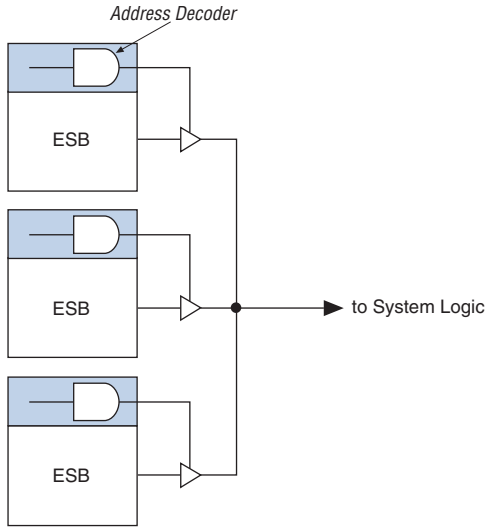



## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

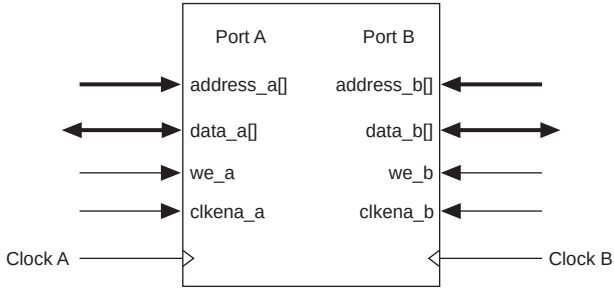
*Figure 17. ESB Block Diagram*

*Figure 18. Deep Memory Block Implemented with Multiple ESBs*




The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in Figure 19.

*Figure 19. APEX 20K ESB Implementing Dual-Port RAM*

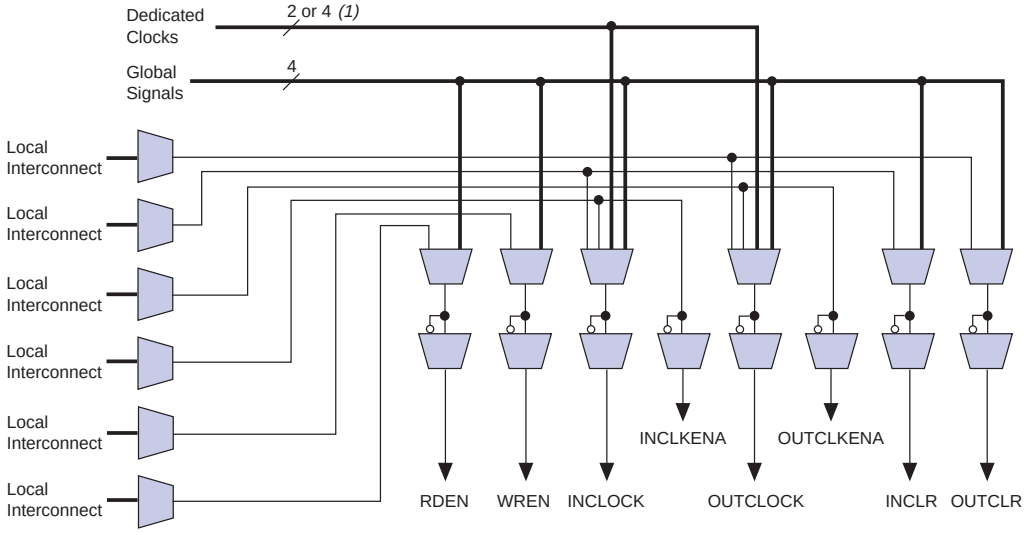


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

***Figure 24. ESB Control Signal Generation***




*Note to Figure 24:*
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

*Table 13. APEX 20KE MultiVolt I/O Support* *Note (1)*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | *(2)* | | | ✓ *(3)* | |

*Notes to Table 13:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

*Table 22. APEX 20K JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

| Table 39. APEX 20KE External Bidirectional Timing Parameters Note (1) | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous Output Enable Register to output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous Output Enable Register output buffer enable delay | C1 = 10 pF |
| $t_{INSUBIDIRPLL}$ | Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{INHBIDIRPLL}$ | Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIRPLL}$ | Clock-to-output delay for bidirectional pins with PLL clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIRPLL}$ | Synchronous Output Enable Register to output buffer disable delay with PLL | C1 = 10 pF |
| $t_{ZXBIDIRPLL}$ | Synchronous Output Enable Register output buffer enable delay with PLL | C1 = 10 pF |

*Note to Tables 38 and 39:*
(1) These timing parameters are sample-tested only.

Tables 55 through 60 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

*Table 55. EP20K60E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.17 | | 0.15 | | 0.16 | | ns |
| $t_{H}$ | 0.32 | | 0.33 | | 0.39 | | ns |
| $t_{CO}$ | | 0.29 | | 0.40 | | 0.60 | ns |
| $t_{LUT}$ | | 0.77 | | 1.07 | | 1.59 | ns |

*Table 57. EP20K60E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.26 | | 0.30 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.58 | | 1.79 | ns |
| $t_{F20+}$ | | 1.96 | | 2.14 | | 2.45 | ns |

*Table 58. EP20K60E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.28 | | 0.41 | | ns |
| $t_{PREP}$ | 0.20 | | 0.28 | | 0.41 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBWP}$ | 1.29 | | 1.80 | | 2.66 | | ns |
| $t_{ESBRP}$ | 1.04 | | 1.45 | | 2.14 | | ns |

*Table 59. EP20K60E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.03 | | 2.12 | | 2.23 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{INSUPLL}$ | 1.12 | | 1.15 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |

*Table 64. EP20K100E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{CL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.29 | | 1.53 | | 1.66 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 65. EP20K100E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.23 | | 2.32 | | 2.43 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| $t_{INSUPLL}$ | 1.58 | | 1.66 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |

*Table 66. EP20K100E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.74 | | 2.96 | | 3.19 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| $t_{XZBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| $t_{ZXBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| $t_{INSUBIDIRPLL}$ | 4.64 | | 5.03 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |

*Table 86. EP20K400E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 1.91 | | 1.99 | ns |
| $t_{ESBSRC}$ | | 2.30 | | 2.66 | | 2.93 | ns |
| $t_{ESBAWC}$ | | 3.09 | | 3.58 | | 3.99 | ns |
| $t_{ESBSWC}$ | | 3.01 | | 3.65 | | 4.05 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.63 | | 0.65 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.77 | | 0.84 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.77 | | 1.86 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.35 | | 1.47 | | 1.61 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.18 | | -0.30 | | -0.27 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | -0.02 | | -0.11 | | -0.03 | | ns |
| $t_{ESBRADDRSU}$ | 0.06 | | -0.01 | | -0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.16 | | 1.40 | | 1.54 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 2.55 | | 2.85 | ns |
| $t_{ESBDD}$ | | 2.73 | | 3.17 | | 3.58 | ns |
| $t_{PD}$ | | 1.57 | | 1.83 | | 2.07 | ns |
| $t_{PTERMSU}$ | 0.92 | | 0.99 | | 1.18 | | ns |
| $t_{PTERMCO}$ | | 1.18 | | 1.43 | | 1.17 | ns |

*Table 94. EP20K600E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.26 | | 0.34 | | ns |
| $t_{PREP}$ | 0.18 | | 0.26 | | 0.34 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBWP}$ | 1.17 | | 1.68 | | 2.18 | | ns |
| $t_{ESBRP}$ | 0.95 | | 1.35 | | 1.76 | | ns |

*Table 95. EP20K600E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.74 | | 2.74 | | 2.87 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.51 | 2.00 | 6.06 | 2.00 | 6.61 | ns |
| $t_{INSUPLL}$ | 1.86 | | 1.96 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.62 | 0.50 | 2.91 | - | - | ns |

*Table 96. EP20K600E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 0.64 | | 0.98 | | 1.08 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.51 | 2.00 | 6.06 | 2.00 | 6.61 | ns |
| $t_{XZBIDIR}$ | | 6.10 | | 6.74 | | 7.10 | ns |
| $t_{ZXBIDIR}$ | | 6.10 | | 6.74 | | 7.10 | ns |
| $t_{INSUBIDIRPLL}$ | 2.26 | | 2.68 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.62 | 0.50 | 2.91 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 3.21 | | 3.59 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 3.21 | | 3.59 | | - | ns |

*Table 98. EP20K1000E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.78 | | 2.02 | | 1.95 | ns |
| $t_{ESBSRC}$ | | 2.52 | | 2.91 | | 3.14 | ns |
| $t_{ESBAWC}$ | | 3.52 | | 4.11 | | 4.40 | ns |
| $t_{ESBSWC}$ | | 3.23 | | 3.84 | | 4.16 | ns |
| $t_{ESBWASU}$ | 0.62 | | 0.67 | | 0.61 | | ns |
| $t_{ESBWAH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.77 | | 0.79 | | 0.81 | | ns |
| $t_{ESBWDH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.74 | | 1.92 | | 1.85 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.01 | | 0.23 | | ns |
| $t_{ESBWESU}$ | 2.07 | | 2.28 | | 2.41 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.25 | | 0.27 | | 0.29 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.04 | | 0.11 | | ns |
| $t_{ESBRADDRSU}$ | 0.14 | | 0.11 | | 0.16 | | ns |
| $t_{ESBDATACO1}$ | | 1.29 | | 1.50 | | 1.63 | ns |
| $t_{ESBDATACO2}$ | | 2.55 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.12 | | 3.57 | | 3.85 | ns |
| $t_{PD}$ | | 1.84 | | 2.13 | | 2.32 | ns |
| $t_{PTERMSU}$ | 1.08 | | 1.19 | | 1.32 | | ns |
| $t_{PTERMCO}$ | | 1.31 | | 1.53 | | 1.66 | ns |

*Table 102. EP20K1000E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 3.22 | | 3.33 | | 3.51 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{XZBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{ZXBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{INSUBIDIRPLL}$ | 3.25 | | 3.26 | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | | | ns |
| $t_{XZBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |
| $t_{ZXBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |

Tables 103 through 108 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

*Table 103. EP20K1500E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

# Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

## Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

## Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for $t_{ESBDATAH}$ parameter.

## Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

## Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.