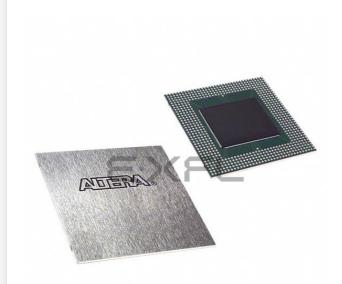
E·XFL

Intel - EP20K1500EBC652-2 Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	5184
Number of Logic Elements/Cells	51840
Total RAM Bits	442368
Number of I/O	488
Number of Gates	2392000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1500ebc652-2

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
 - Built-in low-skew clock tree
 - Up to eight global clock signals
 - ClockLock[®] feature reducing clock delay and skew
 - ClockBoost[®] feature providing clock multiplication and division
 - ClockShiftTM programmable clock phase and delay shifting
- Powerful I/O features
 - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
 - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
 - Bidirectional I/O performance $(t_{CO} + t_{SU})$ up to 250 MHz
 - LVDS performance up to 840 Mbits per channel
 - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
 - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
 - Programmable clamp to V_{CCIO}
 - Individual tri-state output enable control for each pin
 - Programmable output slew-rate control to reduce switching noise
 - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stubseries terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
 - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
 - Four-level hierarchical FastTrack[®] Interconnect structure providing fast, predictable interconnect delays
 - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
 - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
 - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
 - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
 - FineLine BGA[®] packages maximize board space efficiency
- Advanced software support
 - Software design support and automatic place-and-route provided by the Altera[®] Quartus[®] II development system for

General Description

APEX[™] 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and productterm-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, registerintensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices. Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LABwide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

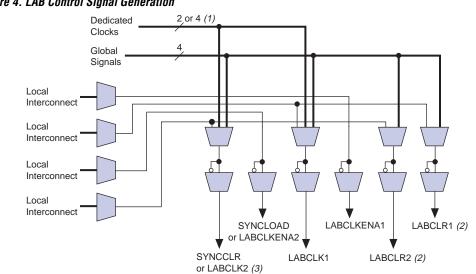
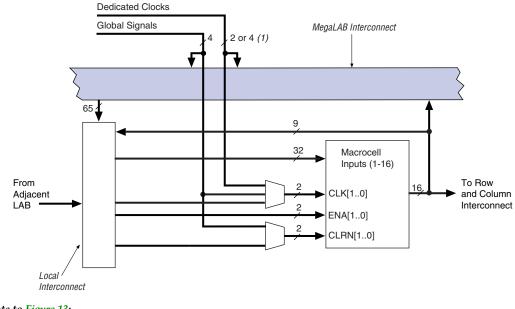


Figure 4. LAB Control Signal Generation

Notes to Figure 4:

- APEX 20KE devices have four dedicated clocks. (1)
- The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the (2) LAB.
- (3)The SYNCCLR signal can be generated by the local interconnect or global signals.

Figure 13. Product-Term Logic in ESB



Note to Figure 13:

(1) APEX 20KE devices have four dedicated clocks.

Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The productterm select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell. The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

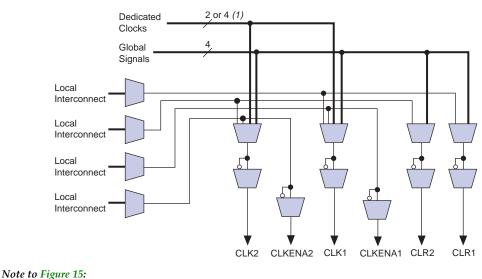


Figure 15. ESB Product-Term Mode Control Logic

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support									
V _{CCIO} (V)	Input Signals (V) Output Signals (V)								
-	2.5	3.3	5.0	2.5	3.3	5.0			
2.5	\checkmark	√(1)	√ (1)	✓					
3.3	\checkmark	\checkmark	√ (1)	√ (2)	\checkmark	 Image: A start of the start of			

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Notes to Table 12:

- The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
- (2) When $V_{CCIO} = 3.3 \text{ V}$, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pullup resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pullup resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

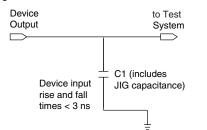


Figure 32. APEX 20K AC Test Conditions Note (1)

Note to Figure 32:

Power supply transients can affect AC measurements. Simultaneous transitions of (1) multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-groundcurrent transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating **Conditions**

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 2	Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings Notes (1), (2)									
Symbol	Parameter	Conditions	Min	Max	Unit					
V _{CCINT}	Supply voltage	With respect to ground (3)	-0.5	3.6	V					
V _{CCIO}			-0.5	4.6	V					
VI	DC input voltage		-2.0	5.75	V					
I _{OUT}	DC output current, per pin		-25	25	mA					
T _{STG}	Storage temperature	No bias	-65	150	°C					
T _{AMB}	Ambient temperature	Under bias	-65	135	°C					
Т _Ј	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C					
		Ceramic PGA packages, under bias		150	°C					

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings	Notes (1), (2)
---	----------------

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V _{CCIO} (10)		4.1	V
V _{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		-0.5		0.8, 0.3 × V _{CCIO} (10)	V
V _{OH}	3.3-V high-level LVTTL output voltage	I _{OH} = -12 mA DC, V _{CCIO} = 3.00 V <i>(11)</i>	2.4			۷
	3.3-V high-level LVCMOS output voltage	I _{OH} = -0.1 mA DC, V _{CCIO} = 3.00 V <i>(11)</i>	V _{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I _{OH} = -0.5 mA DC, V _{CCIO} = 3.00 to 3.60 V (<i>11</i>)	$0.9 imes V_{CCIO}$			V
	2.5-V high-level output voltage	I _{OH} = -0.1 mA DC, V _{CCIO} = 2.30 V (11)	2.1			V
		I _{OH} = -1 mA DC, V _{CCIO} = 2.30 V <i>(11)</i>	2.0			۷
		I _{OH} = -2 mA DC, V _{CCIO} = 2.30 V <i>(11)</i>	1.7			v
V _{OL}	3.3-V low-level LVTTL output voltage	I _{OL} = 12 mA DC, V _{CCIO} = 3.00 V <i>(12)</i>			0.4	V
	3.3-V low-level LVCMOS output voltage	I _{OL} = 0.1 mA DC, V _{CCIO} = 3.00 V (<i>12</i>)			0.2	V
	3.3-V low-level PCI output voltage	I _{OL} = 1.5 mA DC, V _{CCIO} = 3.00 to 3.60 V (<i>12</i>)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	I _{OL} = 0.1 mA DC, V _{CCIO} = 2.30 V <i>(12)</i>			0.2	V
		I _{OL} = 1 mA DC, V _{CCIO} = 2.30 V <i>(12)</i>			0.4	V
		I _{OL} = 2 mA DC, V _{CCIO} = 2.30 V <i>(12)</i>			0.7	V
l _l	Input pin leakage current	V _I = 4.1 to -0.5 V (13)	-10		10	μA
I _{OZ}	Tri-stated I/O pin leakage current	V _O = 4.1 to -0.5 V (13)	-10		10	μΑ
I _{CC0}	V _{CC} supply current (standby) (All ESBs in power-down mode)	V _I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V ₁ = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R _{CONF}	Value of I/O pin pull-up resistor	V _{CCIO} = 3.0 V (14)	20		50	kΩ
	before and during configuration	V _{CCIO} = 2.375 V (14)	30		80	kΩ
		V _{CCIO} = 1.71 V (14)	60		150	kΩ

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

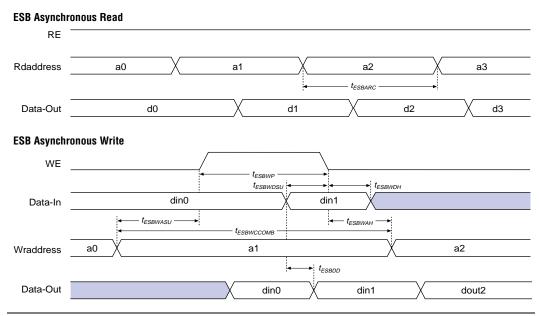


Figure 38. ESB Asynchronous Timing Waveforms

Note to Tables 32 and 33:

(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the f_{MAX} timing model.

Table 34. APEX 20KE LE Timing Microparameters							
Symbol Parameter							
t _{SU}	LE register setup time before clock						
t _H	LE register hold time after clock						
t _{CO}	LE register clock-to-output delay						
t _{LUT}	LUT delay for data-in to data-out						

Table 35. APE	X 20KE ESB Timing Microparameters
Symbol	Parameter
t _{ESBARC}	ESB Asynchronous read cycle time
t _{ESBSRC}	ESB Synchronous read cycle time
t _{ESBAWC}	ESB Asynchronous write cycle time
t _{ESBSWC}	ESB Synchronous write cycle time
t _{ESBWASU}	ESB write address setup time with respect to WE
t _{ESBWAH}	ESB write address hold time with respect to WE
t _{ESBWDSU}	ESB data setup time with respect to WE
t _{ESBWDH}	ESB data hold time with respect to WE
t _{ESBRASU}	ESB read address setup time with respect to RE
t _{ESBRAH}	ESB read address hold time with respect to RE
t _{ESBWESU}	ESB WE setup time before clock when using input register
t _{ESBWEH}	ESB WE hold time after clock when using input register
t _{ESBDATASU}	ESB data setup time before clock when using input register
t _{ESBDATAH}	ESB data hold time after clock when using input register
^t ESBWADDRSU	ESB write address setup time before clock when using input registers
t _{ESBRADDRSU}	ESB read address setup time before clock when using input registers
t _{ESBDATACO1}	ESB clock-to-output delay when using output registers
t _{ESBDATACO2}	ESB clock-to-output delay without output registers
t _{ESBDD}	ESB data-in to data-out delay for RAM mode
t _{PD}	ESB Macrocell input to non-registered output
t _{PTERMSU}	ESB Macrocell register setup time before clock
t _{PTERMCO}	ESB Macrocell register clock-to-output delay

Symbol	-	1	-	-2		-3	Unit
-	Min	Max	Min	Max	Min	Max	
t _{insubidir}	2.77		2.91		3.11		ns
t _{inhbidir}	0.00		0.00		0.00		ns
toutcobidir	2.00	4.84	2.00	5.31	2.00	5.81	ns
t _{xzbidir}		6.47		7.44		8.65	ns
t _{ZXBIDIR}		6.47		7.44		8.65	ns
t _{insubidirpll}	3.44		3.24		-		ns
t _{inhbidirpll}	0.00		0.00		-		ns
toutcobidirpll	0.50	3.37	0.50	3.69	-	-	ns
t _{xzbidirpll}		5.00		5.82		-	ns
t _{zxbidirpll}		5.00		5.82		-	ns

Tables 61 through 66 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

Table 61. EP20K100E f _{MAX} LE Timing Microparameters										
Symbol	-1		-2		-3		Unit			
	Min	Max	Min	Max	Min	Max	1			
t _{SU}	0.25		0.25		0.25		ns			
t _H	0.25		0.25		0.25		ns			
t _{CO}		0.28		0.28		0.34	ns			
t _{LUT}		0.80		0.95		1.13	ns			

Symbol	-'	1	-	2	-:	3	Unit
	Min	Max	Min	Max	Min	Max	
t _{ESBARC}		1.61		1.84		1.97	ns
t _{ESBSRC}		2.57		2.97		3.20	ns
t _{ESBAWC}		0.52		4.09		4.39	ns
t _{ESBSWC}		3.17		3.78		4.09	ns
t _{ESBWASU}	0.56		6.41		0.63		ns
t _{ESBWAH}	0.48		0.54		0.55		ns
t _{ESBWDSU}	0.71		0.80		0.81		ns
t _{ESBWDH}	.048		0.54		0.55		ns
t _{ESBRASU}	1.57		1.75		1.87		ns
t _{ESBRAH}	0.00		0.00		0.20		ns
t _{ESBWESU}	1.54		1.72		1.80		ns
t _{ESBWEH}	0.00		0.00		0.00		ns
t _{ESBDATASU}	-0.16		-0.20		-0.20		ns
t _{ESBDATAH}	0.13		0.13		0.13		ns
t _{ESBWADDRSU}	0.12		0.08		0.13		ns
t _{ESBRADDRSU}	0.17		0.15		0.19		ns
t _{ESBDATACO1}		1.20		1.39		1.52	ns
t _{ESBDATACO2}		2.54		2.99		3.22	ns
t _{ESBDD}		3.06		3.56		3.85	ns
t _{PD}		1.73		2.02		2.20	ns
t _{PTERMSU}	1.11		1.26		1.38		ns
t _{PTERMCO}		1.19		1.40		1.08	ns

Table 63. EP20K100E f _{MAX} Routing Delays										
Symbol	I -1			-2		-3				
	Min	Max	Min	Max	Min	Мах				
t _{F1-4}		0.24		0.27		0.29	ns			
t _{F5-20}		1.04		1.26		1.52	ns			
t _{F20+}		1.12		1.36		1.86	ns			

Tables 67 through 72 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

Table 67. EP20K160E f _{MAX} LE Timing Microparameters										
Symbol	-1		-2		-3		Unit			
	Min	Max	Min	Max	Min	Max				
t _{SU}	0.22		0.24		0.26		ns			
t _H	0.22		0.24		0.26		ns			
t _{CO}		0.25		0.31		0.35	ns			
t _{LUT}		0.69		0.88		1.12	ns			

Symbol	-	1	-	-2		3	Unit
	Min	Max	Min	Max	Min	Max	
t _{ESBARC}		1.65		2.02		2.11	ns
t _{ESBSRC}		2.21		2.70		3.11	ns
t _{ESBAWC}		3.04		3.79		4.42	ns
t _{ESBSWC}		2.81		3.56		4.10	ns
t _{ESBWASU}	0.54		0.66		0.73		ns
t _{ESBWAH}	0.36		0.45		0.47		ns
t _{ESBWDSU}	0.68		0.81		0.94		ns
t _{ESBWDH}	0.36		0.45		0.47		ns
t _{ESBRASU}	1.58		1.87		2.06		ns
t _{ESBRAH}	0.00		0.00		0.01		ns
t _{ESBWESU}	1.41		1.71		2.00		ns
t _{ESBWEH}	0.00		0.00		0.00		ns
t _{ESBDATASU}	-0.02		-0.03		0.09		ns
t _{ESBDATAH}	0.13		0.13		0.13		ns
t _{ESBWADDRSU}	0.14		0.17		0.35		ns
t _{ESBRADDRSU}	0.21		0.27		0.43		ns
t _{ESBDATACO1}		1.04		1.30		1.46	ns
t _{ESBDATACO2}		2.15		2.70		3.16	ns
t _{ESBDD}		2.69		3.35		3.97	ns
t _{PD}		1.55		1.93		2.29	ns
t _{PTERMSU}	1.01		1.23		1.52		ns
t _{PTERMCO}		1.06		1.32		1.04	ns

Tables 85 through 90 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

Table 85. EP20K400E f _{MAX} LE Timing Microparameters											
Symbol	-1 Spee	ed Grade	-2 Spe	ed Grade	-3 Spee	Unit					
	Min	Max	Min	Max	Min	Max					
t _{SU}	0.23		0.23		0.23		ns				
t _H	0.23		0.23		0.23		ns				
t _{CO}		0.25		0.29		0.32	ns				
t _{LUT}		0.70		0.83		1.01	ns				

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Table 87. EP2	OK400E f _{max}	Routing Delays	s					
Symbol	-1 Spee	d Grade	-2 Spe	ed Grade	-3 Speed Grade		Unit	
	Min	Max	Min	Max	Min	Мах		
t _{F1-4}		0.25		0.25		0.26	ns	
t _{F5-20}		1.01		1.12		1.25	ns	
t _{F20+}		3.71		3.92		4.17	ns	

Symbol	-1 Spee	-1 Speed Grade		d Grade	-3 Spee	Unit	
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.36		2.22		2.35		ns
t _{CL}	1.36		2.26		2.35		ns
t _{CLRP}	0.18		0.18		0.19		ns
t _{PREP}	0.18		0.18		0.19		ns
t _{ESBCH}	1.36		2.26		2.35		ns
t _{ESBCL}	1.36		2.26		2.35		ns
t _{ESBWP}	1.17		1.38		1.56		ns
t _{ESBRP}	0.94		1.09		1.25		ns

Table 89. EP20K400E External Timing Parameters											
Symbol	-1 Spee	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade					
	Min	Max	Min	Max	Min	Max					
t _{INSU}	2.51		2.64		2.77		ns				
t _{INH}	0.00		0.00		0.00		ns				
t _{outco}	2.00	5.25	2.00	5.79	2.00	6.32	ns				
tINSUPLL	3.221		3.38		-		ns				
t _{INHPLL}	0.00		0.00		-		ns				
t _{outcopll}	0.50	2.25	0.50	2.45	-	-	ns				

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Symbol	-1 Speed Grade		-2 Spee	d Grade	-3 Spee	Unit	
	Min	Max	Min	Max	Min	Max	
t _{insubidir}	3.22		3.33		3.51		ns
t _{inhbidir}	0.00		0.00		0.00		ns
t _{outcobidir}	2.00	5.75	2.00	6.33	2.00	6.90	ns
t _{xzbidir}		6.31		7.09		7.76	ns
t _{ZXBIDIR}		6.31		7.09		7.76	ns
t _{insubidirpl} L	3.25		3.26				ns
t _{inhbidirpll}	0.00		0.00				ns
toutcobidirpll	0.50	2.25	0.50	2.99			ns
t _{xzbidirpll}		2.81		3.80			ns
t _{zxbidirpll}		2.81		3.80			ns

Tables 103 through 108 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

Table 103. EP	20K1500E f _{MA}	_{NX} LE Timing N	Microparamet	ers				
Symbol	-1 Spee	d Grade	-2 Spee	ed Grade	-3 Speed Grade		Unit	
	Min	Max	Min	Max	Min	Max		
t _{SU}	0.25		0.25		0.25		ns	
t _H	0.25		0.25		0.25		ns	
t _{co}		0.28		0.32		0.33	ns	
t _{LUT}		0.80		0.95		1.13	ns	

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Symbol	-1 Spee	d Grade	-2 Spee	ed Grade	-3 Spee	d Grade	Unit
	Min	Max	Min	Max	Min	Мах	
t _{ESBARC}		1.78		2.02		1.95	ns
t _{ESBSRC}		2.52		2.91		3.14	ns
t _{ESBAWC}		3.52		4.11		4.40	ns
t _{ESBSWC}		3.23		3.84		4.16	ns
t _{ESBWASU}	0.62		0.67		0.61		ns
t _{ESBWAH}	0.41		0.55		0.55		ns
t _{ESBWDSU}	0.77		0.79		0.81		ns
t _{ESBWDH}	0.41		0.55		0.55		ns
t _{ESBRASU}	1.74		1.92		1.85		ns
t _{ESBRAH}	0.00		0.01		0.23		ns
t _{ESBWESU}	2.07		2.28		2.41		ns
t _{ESBWEH}	0.00		0.00		0.00		ns
t _{ESBDATASU}	0.25		0.27		0.29		ns
t _{ESBDATAH}	0.13		0.13		0.13		ns
t _{ESBWADDRSU}	0.11		0.04		0.11		ns
t _{ESBRADDRSU}	0.14		0.11		0.16		ns
t _{ESBDATACO1}		1.29		1.50		1.63	ns
t _{ESBDATACO2}		2.55		2.99		3.22	ns
t _{ESBDD}		3.12		3.57		3.85	ns
t _{PD}		1.84		2.13		2.32	ns
t _{PTERMSU}	1.08		1.19		1.32		ns
t _{PTERMCO}		1.31		1.53		1.66	ns

Table 105. EP.	Table 105. EP20K1500E f _{MAX} Routing Delays											
Symbol	-1 Spee	ed Grade	-2 Spec	ed Grade	-3 Speed Grade		Unit					
	Min	Max	Min	Мах	Min	Max						
t _{F1-4}		0.28		0.28		0.28	ns					
t _{F5-20}		1.36		1.50		1.62	ns					
t _{F20+}		4.43		4.48		5.07	ns					

Table 108. EP20K1500E External Bidirectional Timing Parameters									
Symbol	-1 Speed Grade		-2 Spee	d Grade	-3 Spee	Unit			
	Min	Мах	Min	Max	Min	Max			
t _{insubidir}	3.47		3.68		3.99		ns		
t _{inhbidir}	0.00		0.00		0.00		ns		
t _{outcobidir}	2.00	6.18	2.00	6.81	2.00	7.36	ns		
t _{XZBIDIR}		6.91		7.62		8.38	ns		
t _{ZXBIDIR}		6.91		7.62		8.38	ns		
t _{insubidirpll}	3.05		3.26				ns		
t _{inhbidirpll}	0.00		0.00				ns		
t _{outcobidirpll}	0.50	2.67	0.50	2.99			ns		
t _{xzbidirpll}		3.41		3.80			ns		
t _{ZXBIDIRPLL}		3.41		3.80			ns		

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectab	le I/O Standa	ard Input Dela	ays				
Symbol	-1 Spee	ed Grade	-2 Spe	-2 Speed Grade		-3 Speed Grade	
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		-0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		-0.24		-0.23		-0.19	ns
SSTL-3 Class I		-0.32		-0.21		-0.47	ns
SSTL-3 Class II		-0.08		0.03		-0.23	ns
SSTL-2 Class I		-0.17		-0.06		-0.32	ns
SSTL-2 Class II		-0.16		-0.05		-0.31	ns
LVDS		-0.12		-0.12		-0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

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Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- *t*_{ESBWEH} added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.