# Altera - EP20K1500EBC652-3 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 488 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 652-BGA |
| Supplier Device Package | 652-BGA (45x45) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k1500ebc652-3 |

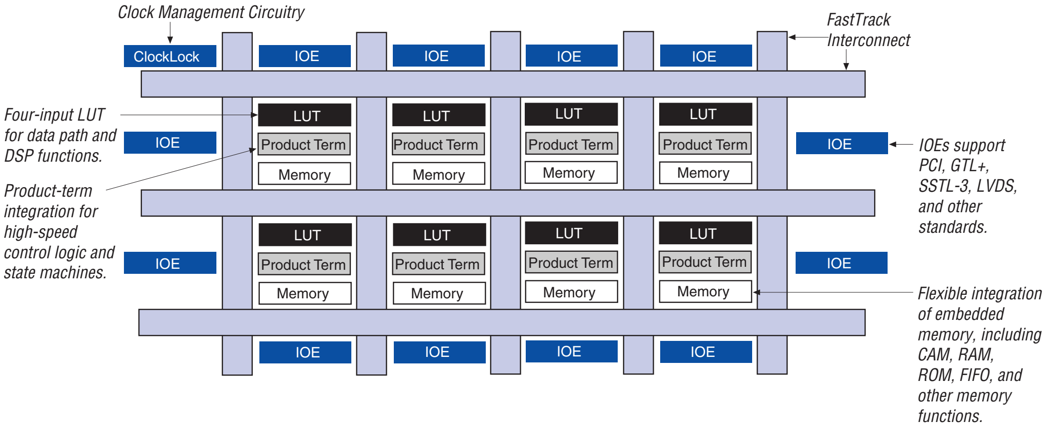
## Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

**Figure 1. APEX 20K Device Block Diagram**



### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the `DATA3` signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: `DATA1`, `DATA2`, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

*Figure 12. APEX 20KE FastRow Interconnect*

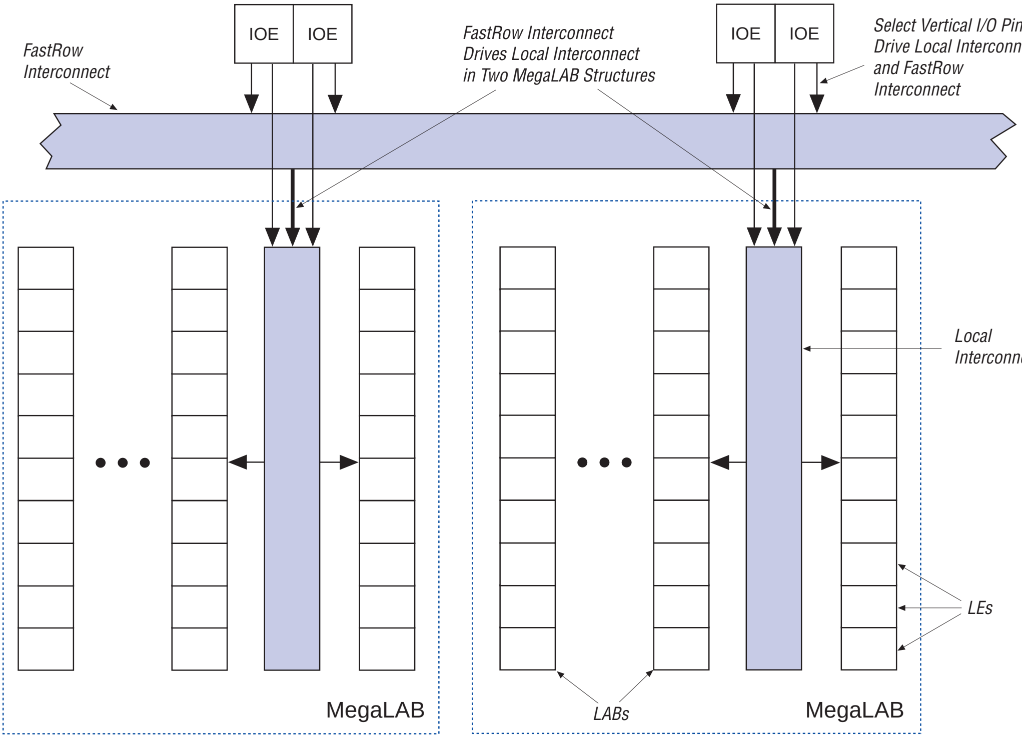


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

*Table 9. APEX 20K Routing Scheme*

| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Row I/O Pin | Column I/O Pin | LE | ESB | Local Interconnect | MegaLAB Interconnect | Row FastTrack Interconnect | Column FastTrack Interconnect | FastRow Interconnect |
| Row I/O Pin | ▨ | | | | ✓ | ✓ | ✓ | ✓ | |
| Column I/O Pin | | ▨ | | | | | | ✓ | ✓ *(1)* |
| LE | | | ▨ | | ✓ | ✓ | ✓ | ✓ | |
| ESB | | | | ▨ | ✓ | ✓ | ✓ | ✓ | |
| Local Interconnect | ✓ | ✓ | ✓ | ✓ | ▨ | | | | |
| MegaLAB Interconnect | | | | | ✓ | ▨ | | | |
| Row FastTrack Interconnect | | | | | | ✓ | ▨ | ✓ | |
| Column FastTrack Interconnect | | | | | | ✓ | ✓ | ▨ | |
| FastRow Interconnect | | | | | ✓ *(1)* | | | | ▨ |

*Note to Table 9:*

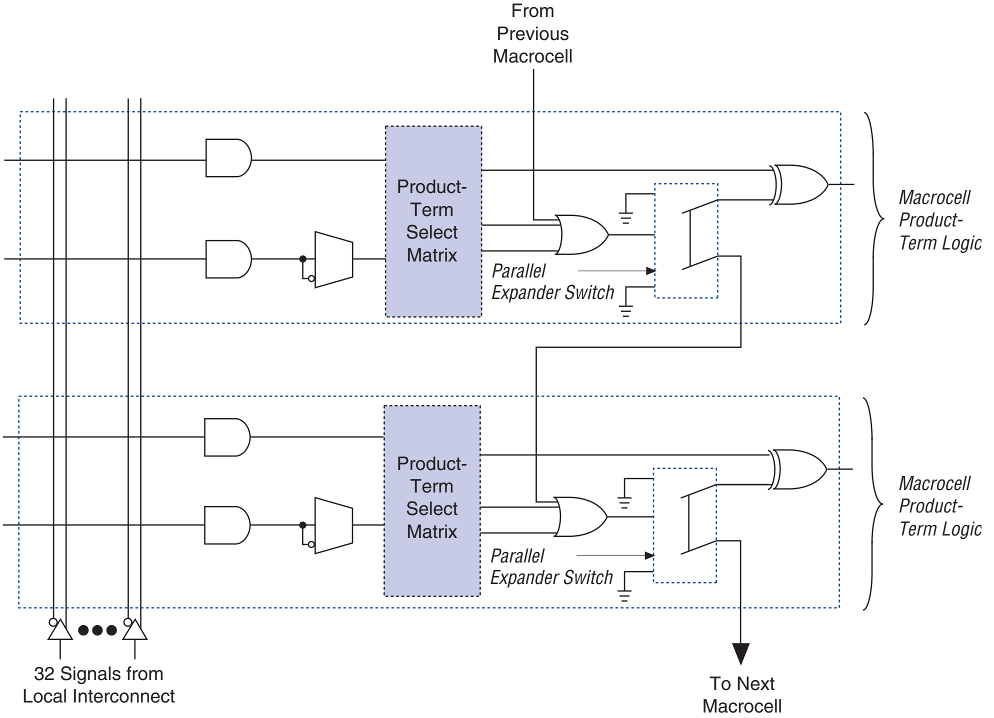
(1) This connection is supported in APEX 20KE devices only.

## Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

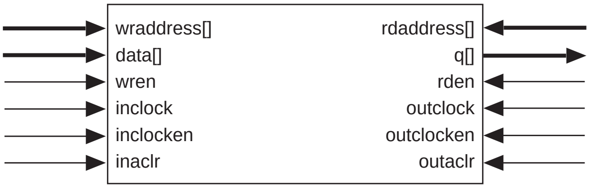
*Figure 16. APEX 20K Parallel Expanders*



## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*



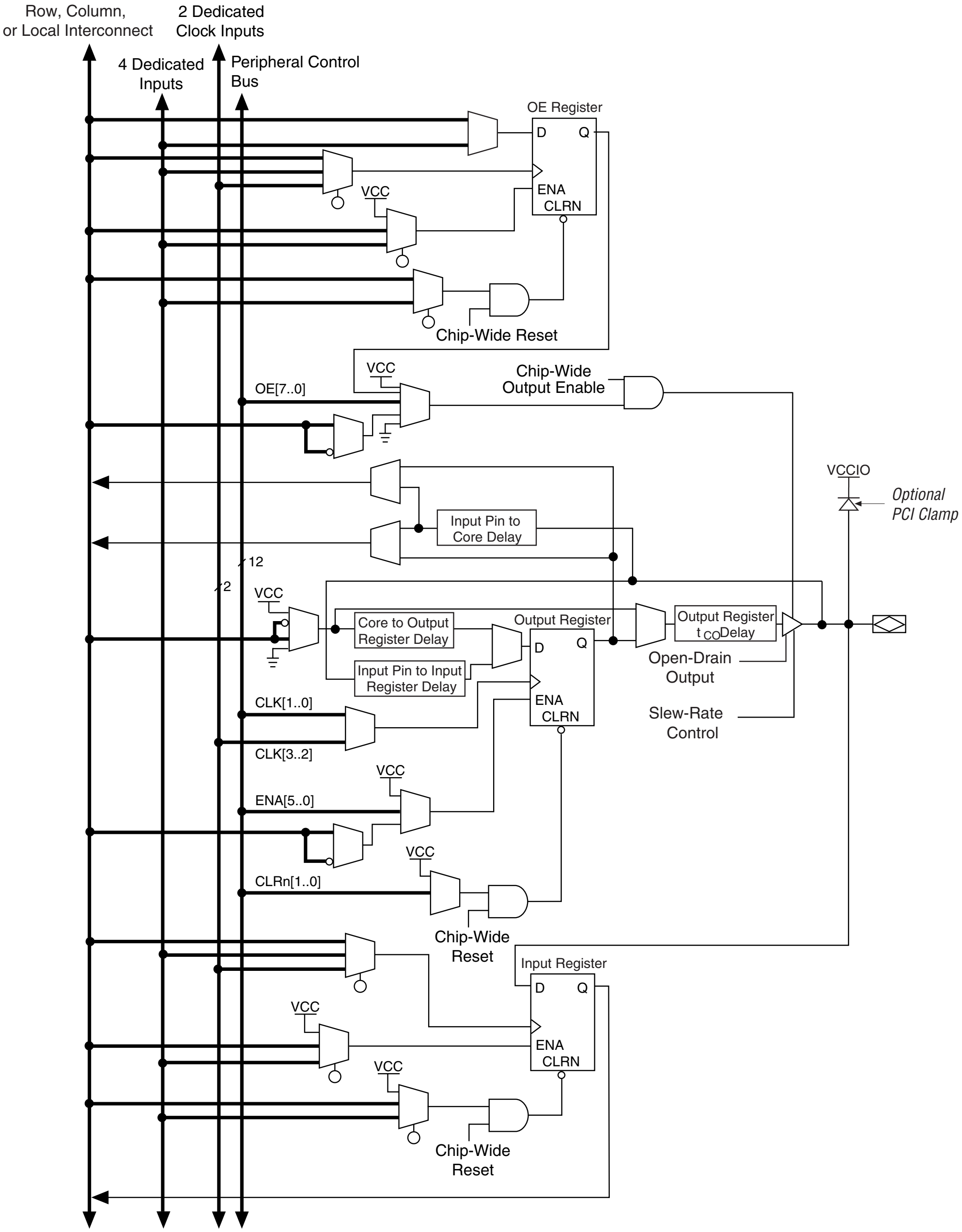
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (`WE`) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the `WE` signal. In contrast, the ESB's synchronous RAM generates its own `WE` signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

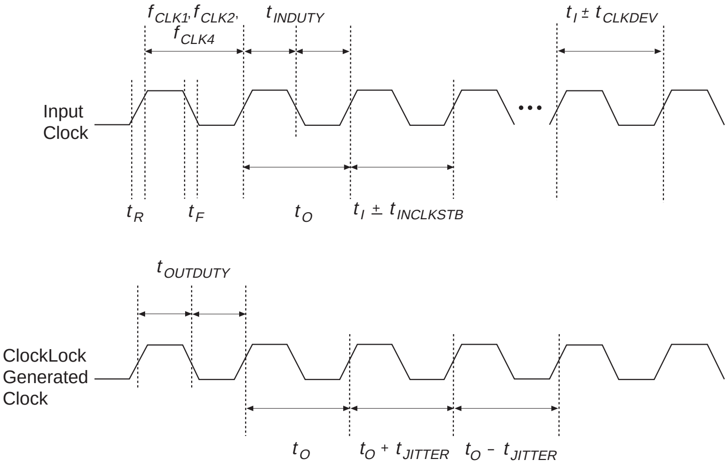
*Figure 25. APEX 20K Bidirectional I/O Registers* *Note (1)*



*Note to Figure 25:*

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

*Figure 30. Specifications for the Incoming & Generated Clocks* *Note (1)*



*Note to Figure 30:*

(1) The tI parameter refers to the nominal input clock period; the tO parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

*Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | 25 | 180 | MHz |
| $f_{CLK1}$ *(1)* | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 180 *(1)* | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 90 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 48 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) *(2)* |  | 25,000 *(3)* | PPM |
| $t_R$ | Input rise time |  | 5 | ns |
| $t_F$ | Input fall time |  | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ClockBoost to acquire lock *(4)* |  | 10 | µs |

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

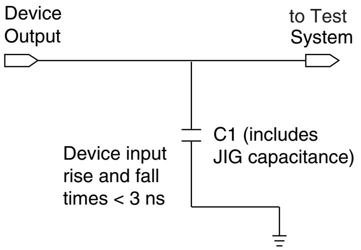
*Table 20. APEX 20K Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K30E | 420 |
| EP20K60E | 624 |
| EP20K100 | 786 |
| EP20K100E | 774 |
| EP20K160E | 984 |
| EP20K200 | 1,176 |
| EP20K200E | 1,164 |
| EP20K300E | 1,266 |
| EP20K400 | 1,536 |
| EP20K400E | 1,506 |
| EP20K600E | 1,806 |
| EP20K1000E | 2,190 |
| EP20K1500E | 1 *(1)* |

***Note to Table 20:***

(1) This device does not support JTAG boundary scan testing.

Figure 32. APEX 20K AC Test Conditions *Note (1)*



*Note to Figure 32:*

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

**Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings** *Notes (1), (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(3)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 28. APEX 20KE Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| | Supply voltage for output buffers, 1.8-V operation | *(3)*, *(4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_I$ | Input voltage | *(5)*, *(6)* | –0.5 | 4.0 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Figure 33. Relationship between $V_{CCIO}$ & $V_{CCINT}$ for 3.3-V PCI Compliance*

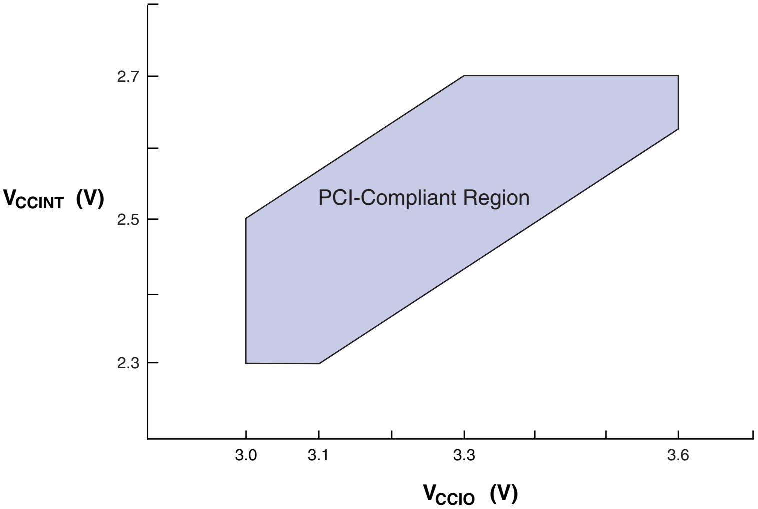
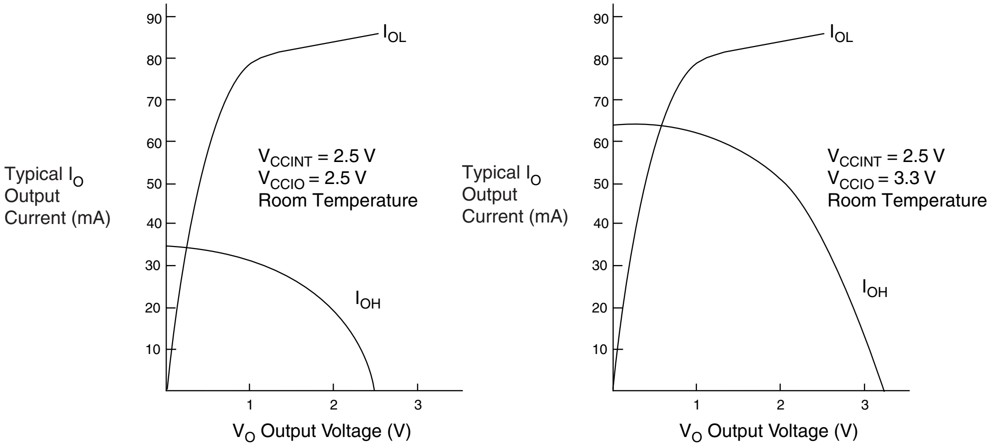


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when `VCCIO` pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

*Figure 34. Output Drive Characteristics of APEX 20K Device Note (1)*



*Note to Figure 34:*

(1) These are transient (AC) currents.

*Table 39. APEX 20KE External Bidirectional Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous Output Enable Register to output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous Output Enable Register output buffer enable delay | C1 = 10 pF |
| $t_{INSUBIDIRPLL}$ | Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{INHBIDIRPLL}$ | Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIRPLL}$ | Clock-to-output delay for bidirectional pins with PLL clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIRPLL}$ | Synchronous Output Enable Register to output buffer disable delay with PLL | C1 = 10 pF |
| $t_{ZXBIDIRPLL}$ | Synchronous Output Enable Register output buffer enable delay with PLL | C1 = 10 pF |

*Note to Tables 38 and 39:*

(1) These timing parameters are sample-tested only.

*Table 52. EP20K30E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CLRP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{PREP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{ESBCH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBCL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBWP}$ | 1.43 | | 2.01 | | 2.97 | | ns |
| $t_{ESBRP}$ | 1.15 | | 1.62 | | 2.39 | | ns |

*Table 53. EP20K30E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.02 | | 2.13 | | 2.24 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{INSUPLL}$ | 2.11 | | 2.23 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |

*Table 54. EP20K30E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.85 | | 1.77 | | 1.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{XZBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{ZXBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{INSUBIDIRPLL}$ | 4.12 | | 4.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |

| Table 60. EP20K60E External Bidirectional Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 | | -2 | | -3 | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.91 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{XZBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{ZXBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{INSUBIDIRPLL}$ | 3.44 | | 3.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |

Tables 61 through 66 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

| Table 61. EP20K100E $f_{MAX}$ LE Timing Microparameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 | | -2 | | -3 | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_H$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.28 | | 0.34 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

### Table 72. EP20K160E External Bidirectional Timing Parameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.86 | | 3.24 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{XZBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{ZXBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{INSUBIDIRPLL}$ | 4.93 | | 5.48 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |

Tables 73 through 78 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

### Table 73. EP20K200E $f_{MAX}$ LE Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_H$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.26 | | 0.31 | | 0.36 | ns |
| $t_{LUT}$ | | 0.70 | | 0.90 | | 1.14 | ns |

### *Table 74. EP20K200E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.68 | | 2.06 | | 2.24 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 2.77 | | 3.18 | ns |
| $t_{ESBAWC}$ | | 3.10 | | 3.86 | | 4.50 | ns |
| $t_{ESBSWC}$ | | 2.90 | | 3.67 | | 4.21 | ns |
| $t_{ESBWASU}$ | 0.55 | | 0.67 | | 0.74 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.83 | | 0.95 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.90 | | 2.09 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.42 | | 1.71 | | 2.01 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.06 | | -0.07 | | 0.05 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.13 | | 0.31 | | ns |
| $t_{ESBRADDRSU}$ | 0.18 | | 0.23 | | 0.39 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.35 | | 1.51 | ns |
| $t_{ESBDATACO2}$ | | 2.19 | | 2.75 | | 3.22 | ns |
| $t_{ESBDD}$ | | 2.75 | | 3.41 | | 4.03 | ns |
| $t_{PD}$ | | 1.58 | | 1.97 | | 2.33 | ns |
| $t_{PTERMSU}$ | 1.00 | | 1.22 | | 1.51 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.37 | | 1.09 | ns |

### *Table 75. EP20K200E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.02 | | 1.20 | | 1.41 | ns |
| $t_{F20+}$ | | 1.99 | | 2.23 | | 2.53 | ns |

| *Table 82. EP20K300E Minimum Pulse Width Timing Parameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1** | | **-2** | | **-3** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.19 | | 0.26 | | 0.35 | | ns |
| $t_{PREP}$ | 0.19 | | 0.26 | | 0.35 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.25 | | 1.71 | | 2.28 | | ns |
| $t_{ESBRP}$ | 1.01 | | 1.38 | | 1.84 | | ns |

| *Table 83. EP20K300E External Timing Parameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1** | | **-2** | | **-3** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{INSU}$ | 2.31 | | 2.44 | | 2.57 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| $t_{INSUPLL}$ | 1.76 | | 1.85 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |

| *Table 84. EP20K300E External Bidirectional Timing Parameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1** | | **-2** | | **-3** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.85 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| $t_{XZBIDIR}$ | | 7.59 | | 8.30 | | 9.09 | ns |
| $t_{ZXBIDIR}$ | | 7.59 | | 8.30 | | 9.09 | ns |
| $t_{INSUBIDIRPLL}$ | 2.50 | | 2.76 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.43 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.43 | | - | ns |

Tables 85 through 90 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

*Table 85. EP20K400E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{H}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{CO}$ | | 0.25 | | 0.29 | | 0.32 | ns |
| $t_{LUT}$ | | 0.70 | | 0.83 | | 1.01 | ns |

**Table 98. EP20K1000E $f_{MAX}$ ESB Timing Microparameters**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.78 | | 2.02 | | 1.95 | ns |
| $t_{ESBSRC}$ | | 2.52 | | 2.91 | | 3.14 | ns |
| $t_{ESBAWC}$ | | 3.52 | | 4.11 | | 4.40 | ns |
| $t_{ESBSWC}$ | | 3.23 | | 3.84 | | 4.16 | ns |
| $t_{ESBWASU}$ | 0.62 | | 0.67 | | 0.61 | | ns |
| $t_{ESBWAH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.77 | | 0.79 | | 0.81 | | ns |
| $t_{ESBWDH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.74 | | 1.92 | | 1.85 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.01 | | 0.23 | | ns |
| $t_{ESBWESU}$ | 2.07 | | 2.28 | | 2.41 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.25 | | 0.27 | | 0.29 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.04 | | 0.11 | | ns |
| $t_{ESBRADDRSU}$ | 0.14 | | 0.11 | | 0.16 | | ns |
| $t_{ESBDATACO1}$ | | 1.29 | | 1.50 | | 1.63 | ns |
| $t_{ESBDATACO2}$ | | 2.55 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.12 | | 3.57 | | 3.85 | ns |
| $t_{PD}$ | | 1.84 | | 2.13 | | 2.32 | ns |
| $t_{PTERMSU}$ | 1.08 | | 1.19 | | 1.32 | | ns |
| $t_{PTERMCO}$ | | 1.31 | | 1.53 | | 1.66 | ns |