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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

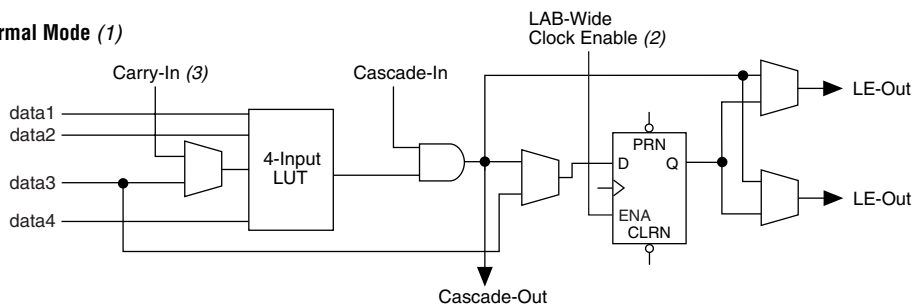
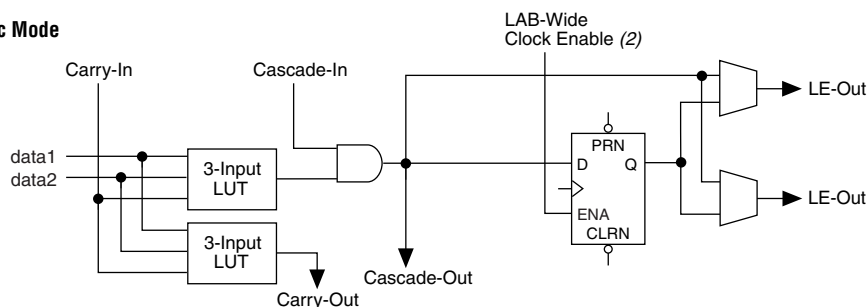
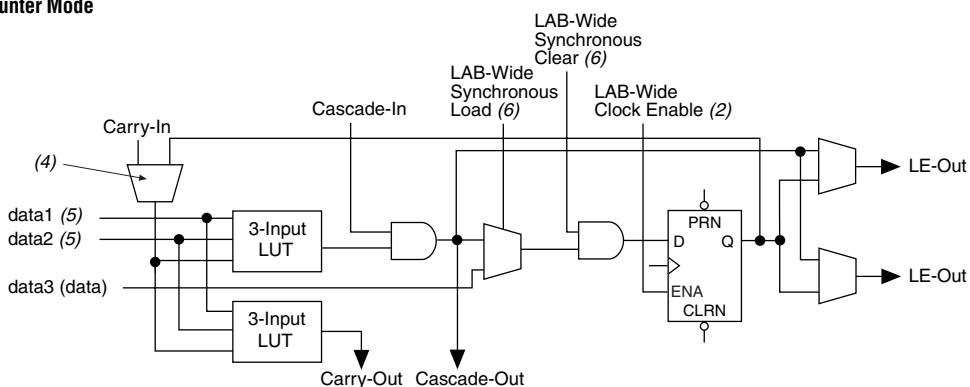
#### Details

Product Status	Obsolete
Number of LABs/CLBs	5184
Number of Logic Elements/Cells	51840
Total RAM Bits	442368
Number of I/O	808
Number of Gates	2392000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k1500efc1020-1x">https://www.e-xfl.com/product-detail/intel/ep20k1500efc1020-1x</a>

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock<sup>®</sup> feature reducing clock delay and skew
  - ClockBoost<sup>®</sup> feature providing clock multiplication and division
  - ClockShift<sup>™</sup> programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ( $t_{CO} + t_{SU}$ ) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - Programmable clamp to  $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack<sup>®</sup> Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
  - FineLine BGA<sup>®</sup> packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera<sup>®</sup> Quartus<sup>®</sup> II development system for

**Table 8. Comparison of APEX 20K & APEX 20KE Features**

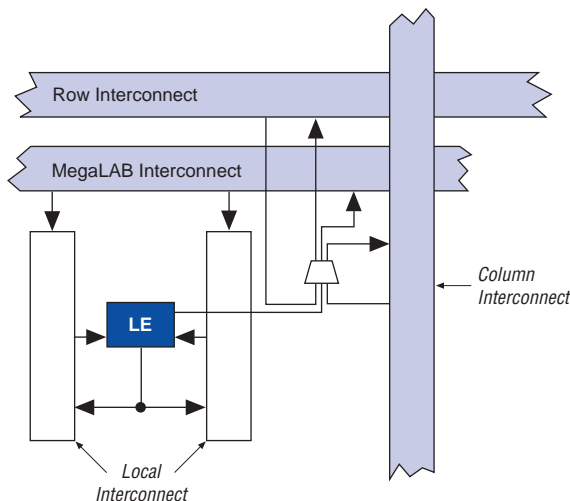
Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
SignalTap logic analysis	Full support	Full support
32/64-Bit, 33-MHz PCI	Full compliance in -1, -2 speed grades	Full compliance in -1, -2 speed grades
32/64-Bit, 66-MHz PCI	-	Full compliance in -1 speed grade
MultiVolt I/O	2.5-V or 3.3-V $V_{CCIO}$ $V_{CCIO}$ selected for device Certain devices are 5.0-V tolerant	1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$ $V_{CCIO}$ selected block-by-block 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction 2× and 4× clock multiplication	Clock delay reduction $m/(n \times v)$ or $m/(n \times k)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVTTL True-LVDS and LVPECL data pins (in EP20K300E and larger devices) LVDS and LVPECL signaling (in all BGA and FineLine BGA devices) LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

**Figure 8. APEX 20K LE Operating Modes****Normal Mode (1)****Arithmetic Mode****Counter Mode****Notes to Figure 8:**

- (1) LEs in normal mode support register packing.
- (2) There are two LAB-wide clock enables per LAB.
- (3) When using the carry-in in normal mode, the packed register feature is unavailable.
- (4) A register feedback multiplexer is available on LE1 of each LAB.
- (5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
- (6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

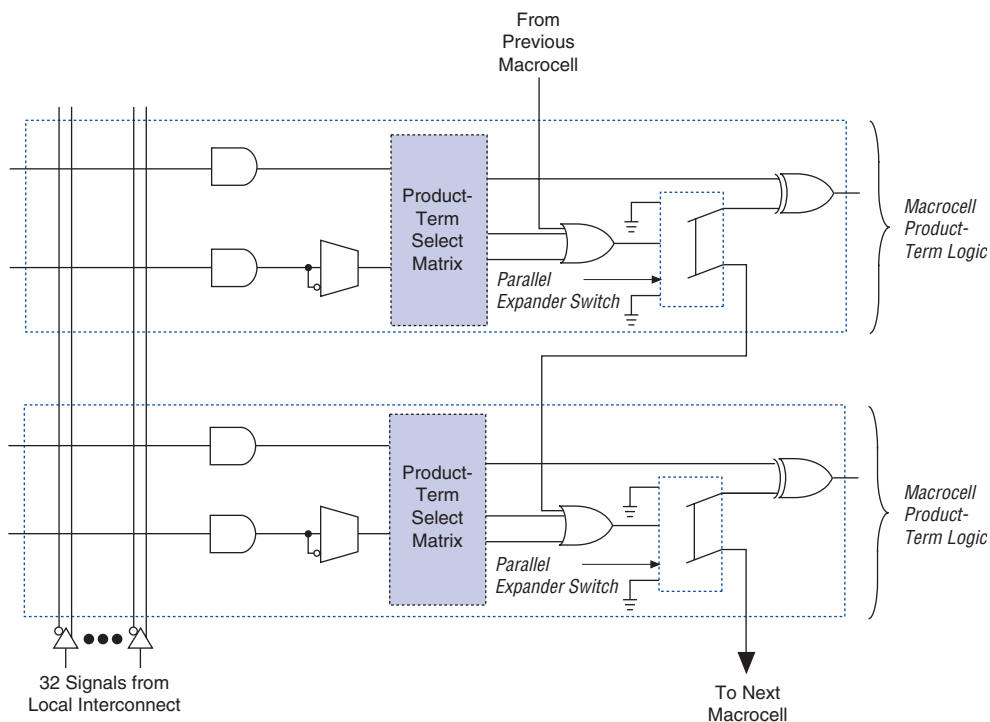
Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

**Figure 11. Driving the FastTrack Interconnect**



APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABs in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

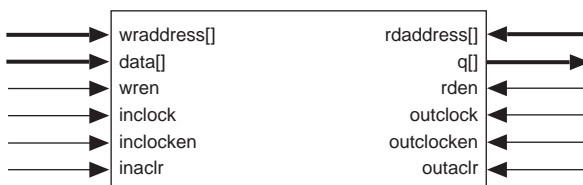
**Figure 16. APEX 20K Parallel Expanders**

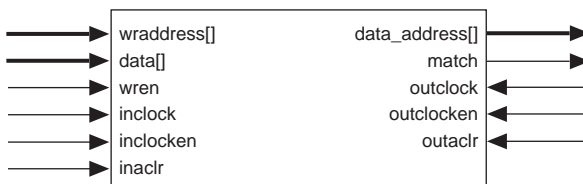


## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

**Figure 17. ESB Block Diagram**



**Figure 23. APEX 20KE CAM Block Diagram**

CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing “don’t care” bits into words of the memory. The “don’t-care” bit can be used as a mask for CAM comparisons; any bit set to “don’t-care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t-care” bits are used, a third clock cycle is required.

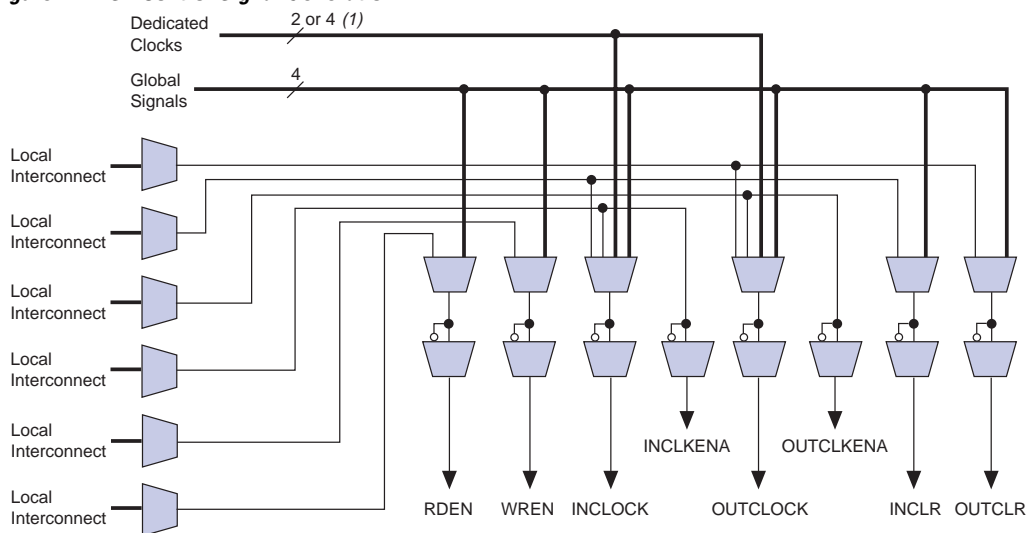


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. [Figure 24](#) shows the ESB control signal generation logic.

**Figure 24. ESB Control Signal Generation**



**Note to Figure 24:**

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.



## Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

## Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

<b>Table 10. APEX 20K Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register $t_{CO}$ delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

**Table 11** describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

<b>Table 11. APEX 20KE Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register $t_{CO}$ Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. **Figure 26** shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

**Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions** *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
$V_I$	Input voltage	(3), (6)	-0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)** *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (9)		5.75	V
$V_{IL}$	Low-level input voltage		-0.5		$0.8, 0.3 \times V_{CCIO}$ (9)	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (10)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (10)	1.7			V

Figure 33. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

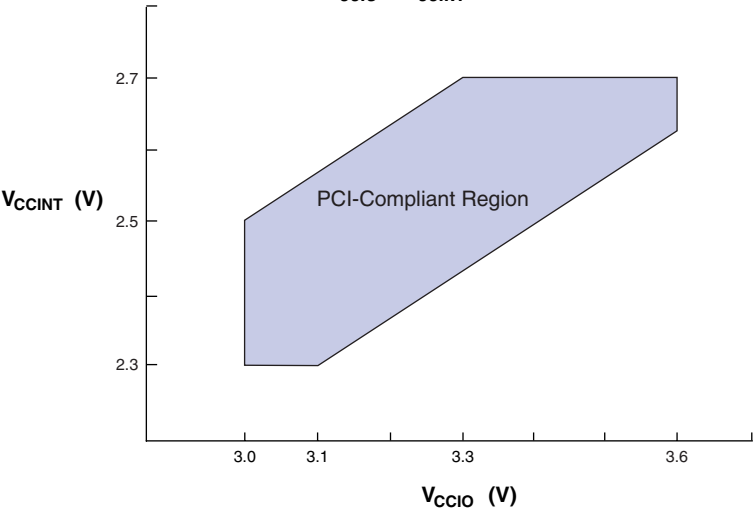
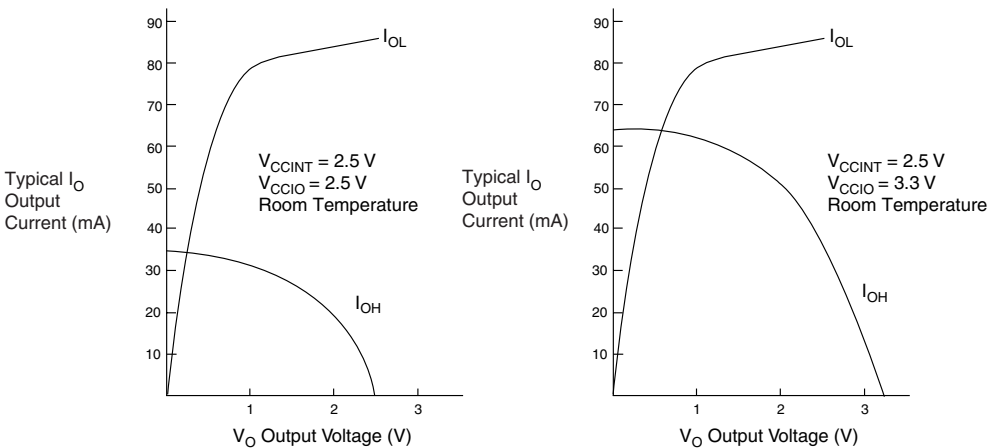


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when  $V_{CCIO}$  pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

Figure 34. Output Drive Characteristics of APEX 20K Device *Note (1)*

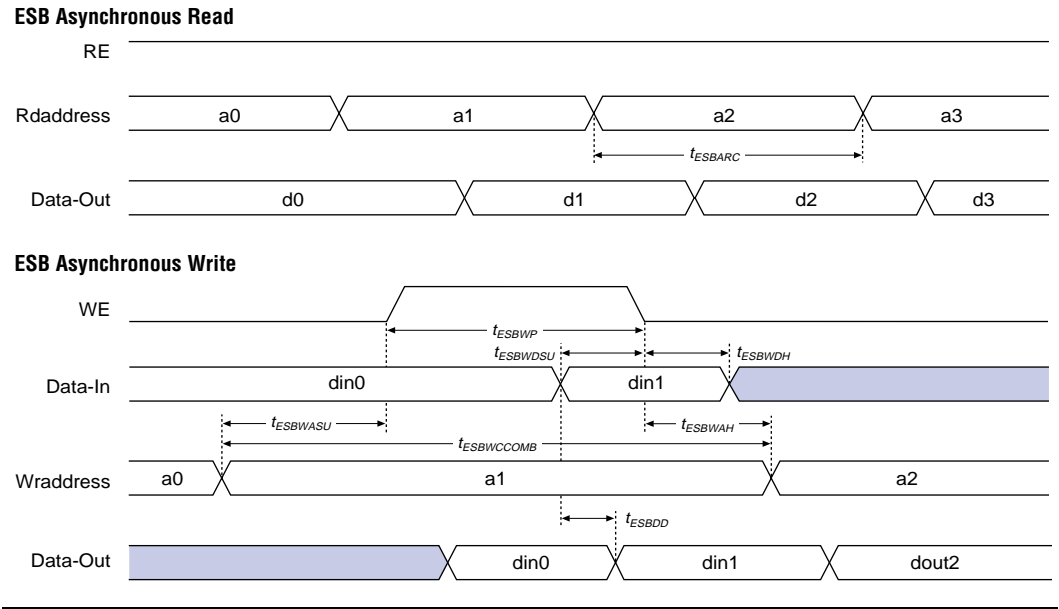


*Note to Figure 34:*

(1) These are transient (AC) currents.

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms



Note to [Tables 32 and 33](#):

(1) These timing parameters are sample-tested only.

[Tables 34 through 37](#) show APEX 20KE LE, ESB, routing, and functional timing microparameters for the  $f_{MAX}$  timing model.

**Table 34. APEX 20KE LE Timing Microparameters**

Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LUT delay for data-in to data-out

**Table 35. APEX 20KE ESB Timing Microparameters**

Symbol	Parameter
$t_{ESBARC}$	ESB Asynchronous read cycle time
$t_{ESBSRC}$	ESB Synchronous read cycle time
$t_{ESBAWC}$	ESB Asynchronous write cycle time
$t_{ESBSWC}$	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
$t_{ESBWAH}$	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
$t_{ESBWDH}$	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
$t_{ESBRAH}$	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBWEH}$	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

Tables 40 through 42 show the  $f_{\text{MAX}}$  timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 40. EP20K100  $f_{\text{MAX}}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.5		0.6		0.8		ns
$t_{\text{H}}$	0.7		0.8		1.0		ns
$t_{\text{CO}}$		0.3		0.4		0.5	ns
$t_{\text{LUT}}$		0.8		1.0		1.3	ns
$t_{\text{ESBRC}}$		1.7		2.1		2.4	ns
$t_{\text{ESBWC}}$		5.7		6.9		8.1	ns
$t_{\text{ESBWESU}}$	3.3		3.9		4.6		ns
$t_{\text{ESBDATASU}}$	2.2		2.7		3.1		ns
$t_{\text{ESBDATAH}}$	0.6		0.8		0.9		ns
$t_{\text{ESBADDRSU}}$	2.4		2.9		3.3		ns
$t_{\text{ESBDATACO1}}$		1.3		1.6		1.8	ns
$t_{\text{ESBDATACO2}}$		2.6		3.1		3.6	ns
$t_{\text{ESBDD}}$		2.5		3.3		3.6	ns
$t_{\text{PD}}$		2.5		3.0		3.6	ns
$t_{\text{PTERMSU}}$	2.3		2.6		3.2		ns
$t_{\text{PTERMCO}}$		1.5		1.8		2.1	ns
$t_{\text{F1-4}}$		0.5		0.6		0.7	ns
$t_{\text{F5-20}}$		1.6		1.7		1.8	ns
$t_{\text{F20+}}$		2.2		2.2		2.3	ns
$t_{\text{CH}}$	2.0		2.5		3.0		ns
$t_{\text{CL}}$	2.0		2.5		3.0		ns
$t_{\text{CLRP}}$	0.3		0.4		0.4		ns
$t_{\text{PREP}}$	0.5		0.5		0.5		ns
$t_{\text{ESBCH}}$	2.0		2.5		3.0		ns
$t_{\text{ESBCL}}$	2.0		2.5		3.0		ns
$t_{\text{ESBWP}}$	1.6		1.9		2.2		ns
$t_{\text{ESBRP}}$	1.0		1.3		1.4		ns



**Table 64. EP20K100E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	2.00		2.00		2.00		ns
t <sub>CL</sub>	2.00		2.00		2.00		ns
t <sub>CLRP</sub>	0.20		0.20		0.20		ns
t <sub>PREP</sub>	0.20		0.20		0.20		ns
t <sub>ESBCH</sub>	2.00		2.00		2.00		ns
t <sub>ESBCL</sub>	2.00		2.00		2.00		ns
t <sub>ESBWP</sub>	1.29		1.53		1.66		ns
t <sub>ESBRP</sub>	1.11		1.29		1.41		ns

**Table 65. EP20K100E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.23		2.32		2.43		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	4.86	2.00	5.35	2.00	5.84	ns
t <sub>INSUPLL</sub>	1.58		1.66		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.96	0.50	3.29	-	-	ns

**Table 66. EP20K100E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	2.74		2.96		3.19		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	4.86	2.00	5.35	2.00	5.84	ns
t <sub>XZBIDIR</sub>		5.00		5.48		5.89	ns
t <sub>ZXBIDIR</sub>		5.00		5.48		5.89	ns
t <sub>INSUBIDIRPLL</sub>	4.64		5.03		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.96	0.50	3.29	-	-	ns
t <sub>XZBIDIRPLL</sub>		3.10		3.42		-	ns
t <sub>ZXBIDIRPLL</sub>		3.10		3.42		-	ns

**Table 80. EP20K300E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.79		2.44		3.25	ns
$t_{ESBSRC}$		2.40		3.12		4.01	ns
$t_{ESBAWC}$		3.41		4.65		6.20	ns
$t_{ESBSWC}$		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
$t_{ESBDD}$		3.41		4.65		6.20	ns
$t_{PD}$		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

**Table 81. EP20K300E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.24		0.26	ns
$t_{F5-20}$		1.33		1.43		1.58	ns
$t_{F20+}$		3.63		3.93		4.35	ns

**Table 102. EP20K1000E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.22		3.33		3.51		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{\text{XZBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{ZXBIDIR}}$		6.31		7.09		7.76	ns
$t_{\text{INSUBIDIRPLL}}$	3.25		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.25	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		2.81		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		2.81		3.80			ns

Tables 103 through 108 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

**Table 103. EP20K1500E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.32		0.33	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns

**Table 106. EP20K1500E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.25		1.43		1.67		ns
t <sub>CL</sub>	1.25		1.43		1.67		ns
t <sub>CLRP</sub>	0.20		0.20		0.20		ns
t <sub>PREP</sub>	0.20		0.20		0.20		ns
t <sub>ESBCH</sub>	1.25		1.43		1.67		ns
t <sub>ESBCL</sub>	1.25		1.43		1.67		ns
t <sub>ESBWP</sub>	1.28		1.51		1.65		ns
t <sub>ESBRP</sub>	1.11		1.29		1.41		ns

**Table 107. EP20K1500E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	3.09		3.30		3.58		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	6.18	2.00	6.81	2.00	7.36	ns
t <sub>INSUPLL</sub>	1.94		2.08		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.67	0.50	2.99	-	-	ns

**Table 108. EP20K1500E External Bidirectional Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.47		3.68		3.99		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{\text{XZBIDIR}}$		6.91		7.62		8.38	ns
$t_{\text{ZXBIDIR}}$		6.91		7.62		8.38	ns
$t_{\text{INSUBIDIRPLL}}$	3.05		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.67	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		3.41		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

**Table 109. Selectable I/O Standard Input Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		−0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		−0.24		−0.23		−0.19	ns
SSTL-3 Class I		−0.32		−0.21		−0.47	ns
SSTL-3 Class II		−0.08		0.03		−0.23	ns
SSTL-2 Class I		−0.17		−0.06		−0.32	ns
SSTL-2 Class II		−0.16		−0.05		−0.31	ns
LVDS		−0.12		−0.12		−0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns