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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	5184
Number of Logic Elements/Cells	51840
Total RAM Bits	442368
Number of I/O	-
Number of Gates	2392000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k1500egc984-1

General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an “E” suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). [Table 8](#) compares the features included in APEX 20K and APEX 20KE devices.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

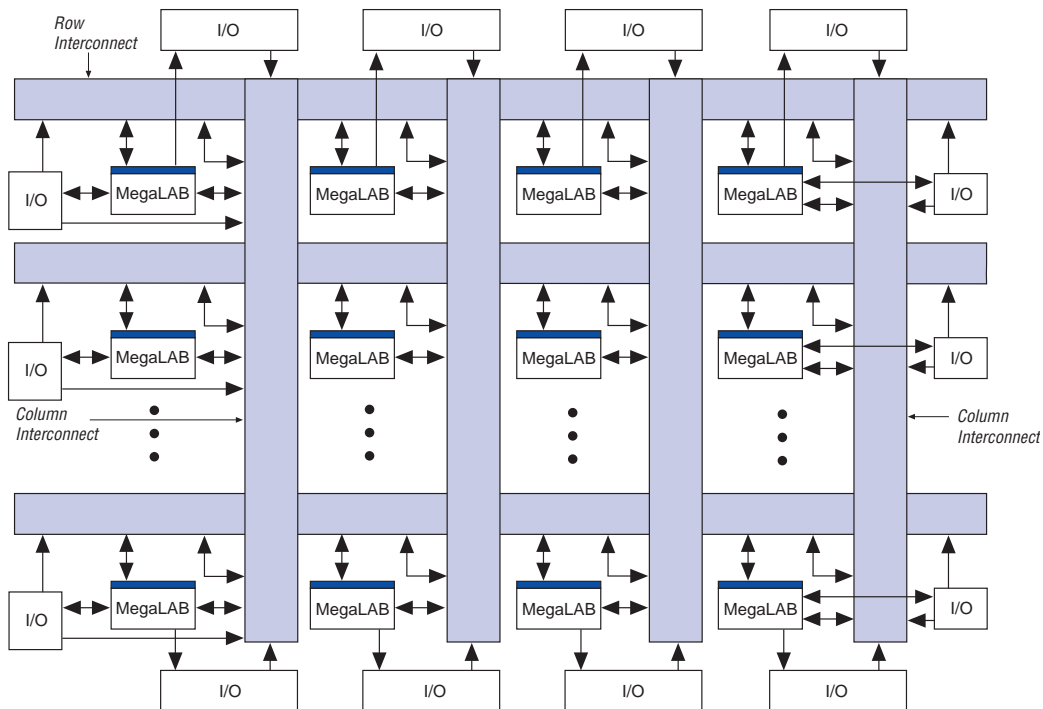
The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

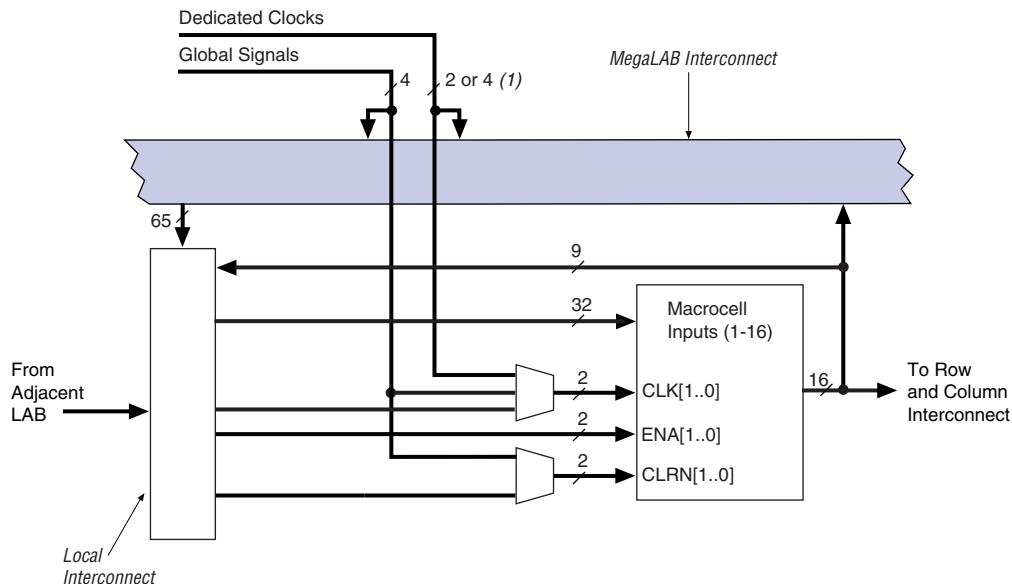
Figure 6 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

Figure 9. APEX 20K Interconnect Structure

A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 13. Product-Term Logic in ESB

Note to Figure 13:

(1) APEX 20KE devices have four dedicated clocks.

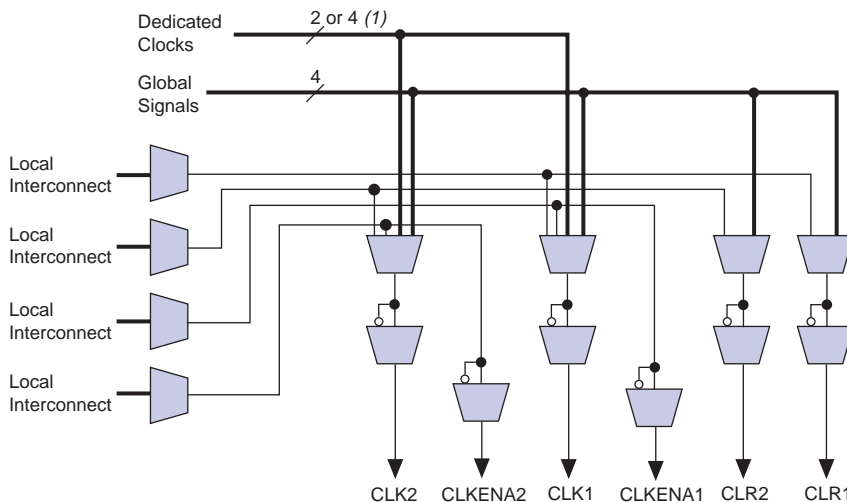
Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Note to Figure 15:

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

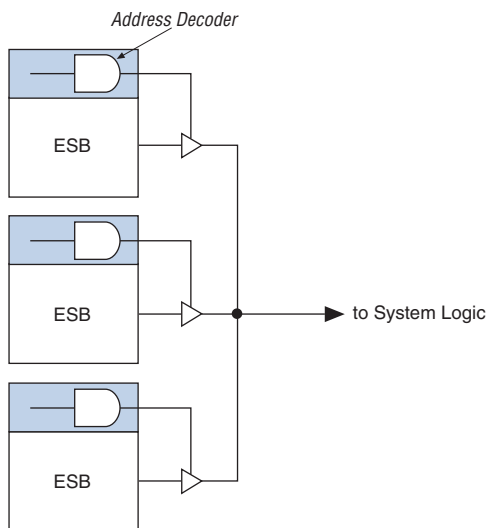
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (*WE*) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the *WE* signal. In contrast, the ESB's synchronous RAM generates its own *WE* signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128×16 , 256×8 , 512×4 , $1,024 \times 2$, or $2,048 \times 1$. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128×16 RAM blocks can be combined to form a 128×32 RAM block, and two 512×4 RAM blocks can be combined to form a 512×8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

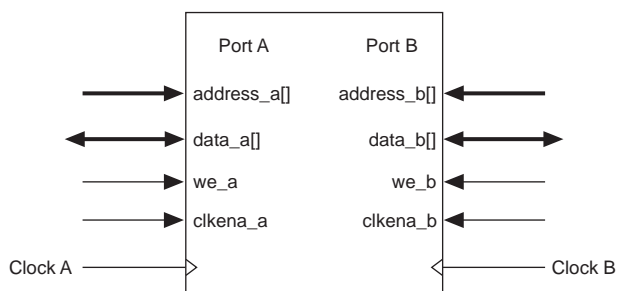
To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).

Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in [Figure 19](#).

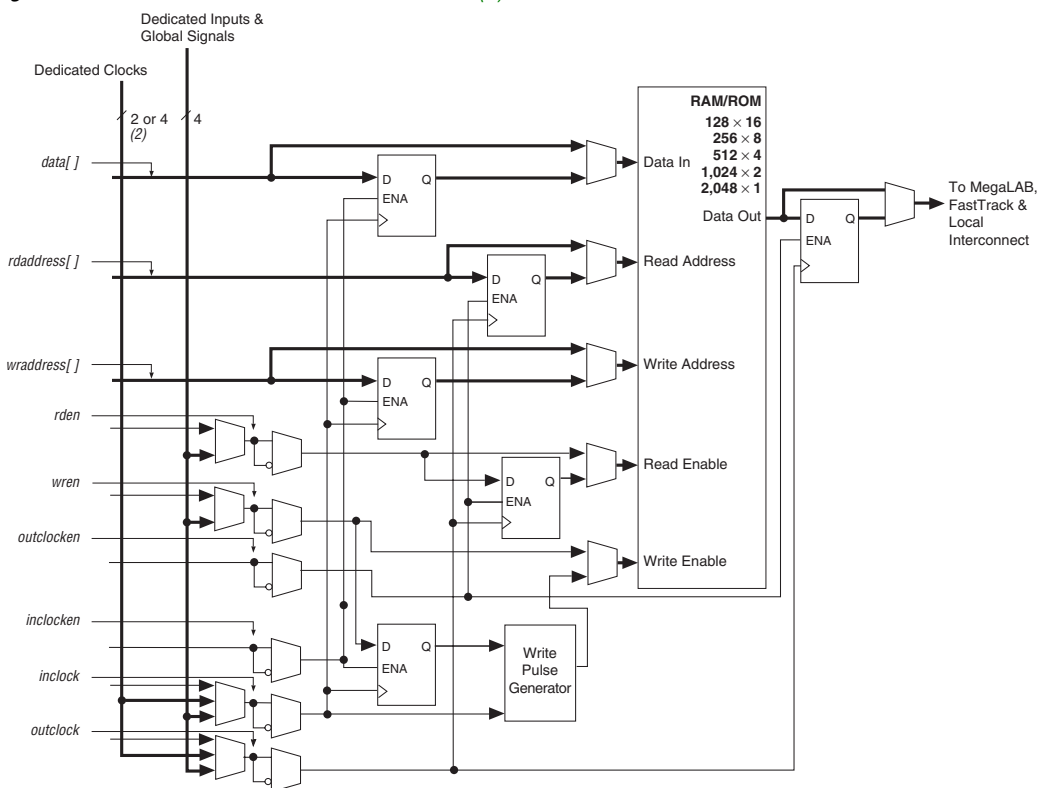
Figure 19. APEX 20K ESB Implementing Dual-Port RAM



Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

Figure 20. ESB in Read/Write Clock Mode *Note (1)*



Notes to Figure 20:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 14. Multiplication Factor Combinations

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where m and k range from 2 to 160, and n and v range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. [Figure 30](#) shows the incoming and generated clock specifications.



For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock (5)		200	ps
t_{INCLKSTB}	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:

- (1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
- (2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
- (4) The jitter specification is measured under long-term observation.
- (5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
t_{OUTDUTY}	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) (1)		25,000 (2)	PPM
t_{R}	Input rise time		5	ns
t_{F}	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock (3)		10	μs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock (4)		200	ps
t_{INCLKSTB}	Input clock stability (measured between adjacent clocks)		50	ps

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. [Tables 20 and 21](#) show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 (1)

Note to [Table 20](#):

- (1) This device does not support JTAG boundary scan testing.

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 12 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (11)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ V}$ (11)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5 \text{ mA DC}$, $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (11)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11)			0.2	V
		$I_{OL} = 1 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11)			0.4	V
		$I_{OL} = 2 \text{ mA DC}$, $V_{CCIO} = 2.30 \text{ V}$ (11)			0.7	V
I_I	Input pin leakage current	$V_I = 5.75 \text{ to } -0.5 \text{ V}$	-10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 5.75 \text{ to } -0.5 \text{ V}$	-10		10	μA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	$V_I = \text{ground}$, no load, no toggling inputs, -1 speed grade (12)		10		mA
		$V_I = \text{ground}$, no load, no toggling inputs, -2, -3 speed grades (12)		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0 \text{ V}$ (13)	20		50	W
		$V_{CCIO} = 2.375 \text{ V}$ (13)	30		80	W

Table 36. APEX 20KE Routing Timing Microparameters *Note (1)*

Symbol	Parameter
t_{F1-4}	Fanout delay using Local Interconnect
t_{F5-20}	Fanout delay estimate using MegaLab Interconnect
t_{F20+}	Fanout delay estimate using FastTrack Interconnect

Note to Table 36:

- (1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 37. APEX 20KE Functional Timing Microparameters

Symbol	Parameter
TCH	Minimum clock high time from clock pin
TCL	Minimum clock low time from clock pin
TCLRP	LE clear Pulse Width
TPREP	LE preset pulse width
TESBCH	Clock high time for ESB
TESBCL	Clock low time for ESB
TESBWP	Write pulse width
TESBRP	Read pulse width

Tables 38 and 39 describe the APEX 20KE external timing parameters.

Table 38. APEX 20KE External Timing Parameters *Note (1)*

Symbol	Clock Parameter	Conditions
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF

Tables 55 through 60 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

Table 55. EP20K60E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.17		0.15		0.16		ns
t_H	0.32		0.33		0.39		ns
t_{CO}		0.29		0.40		0.60	ns
t_{LUT}		0.77		1.07		1.59	ns

Table 74. EP20K200E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.68		2.06		2.24	ns
t_{ESBSRC}		2.27		2.77		3.18	ns
t_{ESBAWC}		3.10		3.86		4.50	ns
t_{ESBSWC}		2.90		3.67		4.21	ns
$t_{ESBWASU}$	0.55		0.67		0.74		ns
t_{ESBWAH}	0.36		0.46		0.48		ns
$t_{ESBWDSU}$	0.69		0.83		0.95		ns
t_{ESBWDH}	0.36		0.46		0.48		ns
$t_{ESBRASU}$	1.61		1.90		2.09		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.42		1.71		2.01		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.06		-0.07		0.05		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.13		0.31		ns
$t_{ESBRADDRSU}$	0.18		0.23		0.39		ns
$t_{ESBDATAO1}$		1.09		1.35		1.51	ns
$t_{ESBDATAO2}$		2.19		2.75		3.22	ns
t_{ESBDD}		2.75		3.41		4.03	ns
t_{PD}		1.58		1.97		2.33	ns
$t_{PTERMSU}$	1.00		1.22		1.51		ns
$t_{PTERMCO}$		1.10		1.37		1.09	ns

Table 75. EP20K200E t_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.27		0.29	ns
t_{F5-20}		1.02		1.20		1.41	ns
t_{F20+}		1.99		2.23		2.53	ns

Table 78. EP20K200E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.81		3.19		3.54		ns
t_{INHBIDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
t_{XZBIDIR}		7.51		8.32		8.67	ns
t_{ZXBIDIR}		7.51		8.32		8.67	ns
$t_{\text{INSUBIDIRPLL}}$	3.30		3.64		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.40		6.05		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.40		6.05		-	ns

Tables 79 through 84 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

Table 79. EP20K300E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.17		0.18		ns
t_{H}	0.31		0.33		0.38		ns
t_{CO}		0.28		0.38		0.51	ns
t_{LUT}		0.79		1.07		1.43	ns

Table 104. EP20K1500E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATAO1}$		1.29		1.50		1.63	ns
$t_{ESBDATAO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 105. EP20K1500E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.28		0.28		0.28	ns
t_{F5-20}		1.36		1.50		1.62	ns
t_{F20+}		4.43		4.48		5.07	ns

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.25		1.43		1.67		ns
t _{CL}	1.25		1.43		1.67		ns
t _{CLRP}	0.20		0.20		0.20		ns
t _{PREP}	0.20		0.20		0.20		ns
t _{ESBCH}	1.25		1.43		1.67		ns
t _{ESBCL}	1.25		1.43		1.67		ns
t _{ESBWP}	1.28		1.51		1.65		ns
t _{ESBRP}	1.11		1.29		1.41		ns

Table 107. EP20K1500E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	3.09		3.30		3.58		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	6.18	2.00	6.81	2.00	7.36	ns
t _{INSUPLL}	1.94		2.08		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.67	0.50	2.99	-	-	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.47		3.68		3.99		ns
t_{INHBIDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
t_{XZBIDIR}		6.91		7.62		8.38	ns
t_{ZXBIDIR}		6.91		7.62		8.38	ns
$t_{\text{INSUBIDIRPLL}}$	3.05		3.26				ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00				ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	2.67	0.50	2.99			ns
$t_{\text{XZBIDIRPLL}}$		3.41		3.80			ns
$t_{\text{ZXBIDIRPLL}}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		-0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		-0.24		-0.23		-0.19	ns
SSTL-3 Class I		-0.32		-0.21		-0.47	ns
SSTL-3 Class II		-0.08		0.03		-0.23	ns
SSTL-2 Class I		-0.17		-0.06		-0.32	ns
SSTL-2 Class II		-0.16		-0.05		-0.31	ns
LVDS		-0.12		-0.12		-0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns