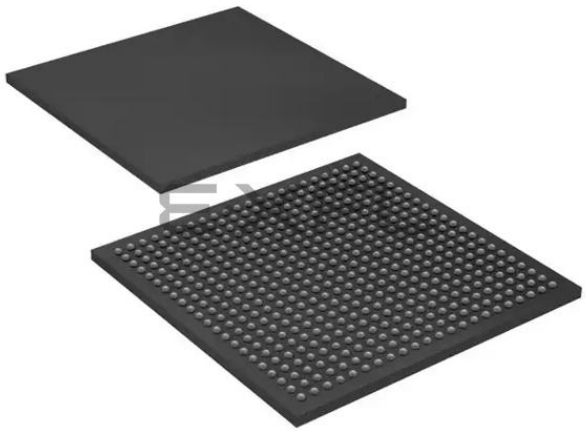

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	640
Number of Logic Elements/Cells	6400
Total RAM Bits	81920
Number of I/O	316
Number of Gates	404000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k160efc484-1x

Table 2. Additional APEX 20K Device Features *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

Note to Tables 1 and 2:
(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

Table 3. APEX 20K Supply Voltages

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage (V_{CCINT})	2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)*

Note to Table 3:
(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock® feature reducing clock delay and skew
  - ClockBoost® feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance (t_{CO} + t_{SU}) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - Programmable clamp to V_{CCIO}
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
  - FineLine BGA® packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus® II development system for

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS)

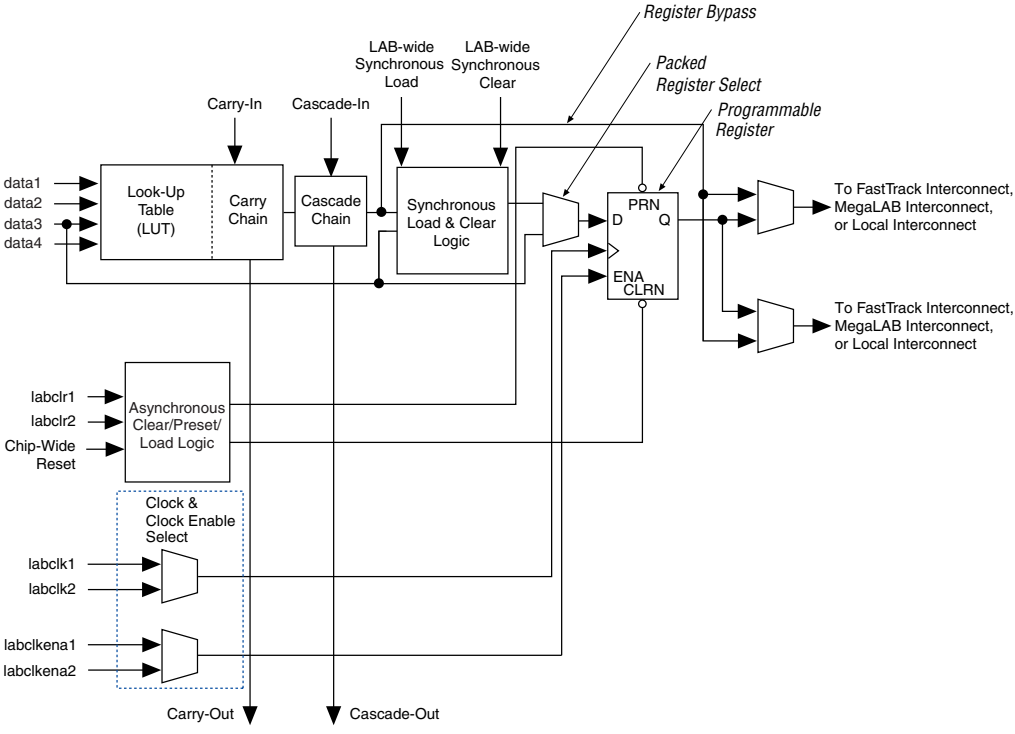
Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

Logic Element

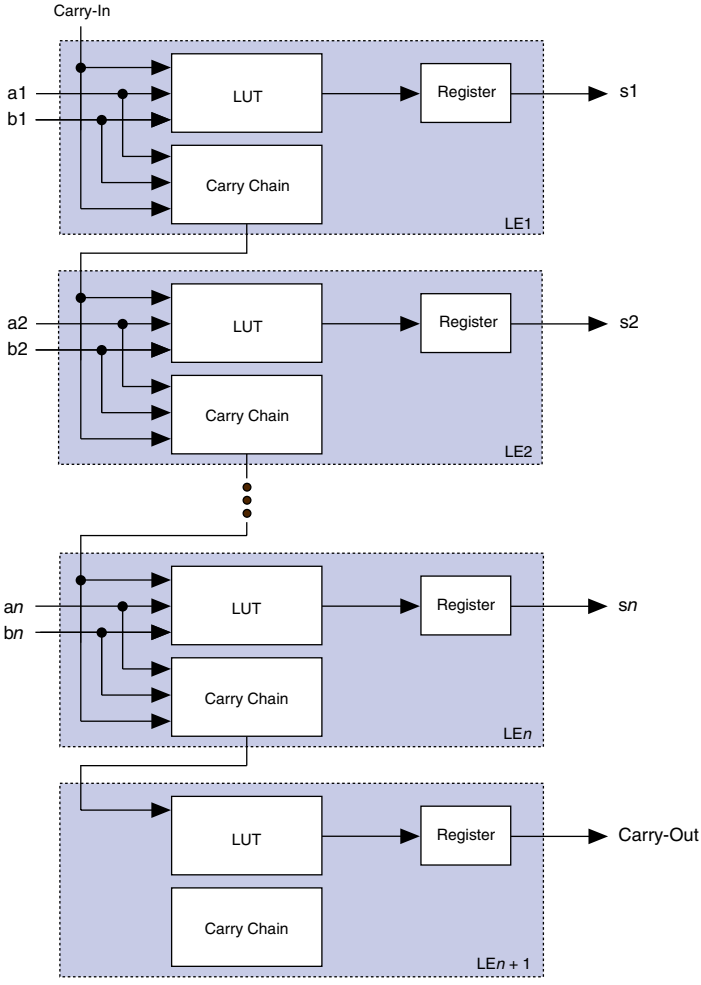
The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Figure 6. APEX 20K Carry Chain



Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain

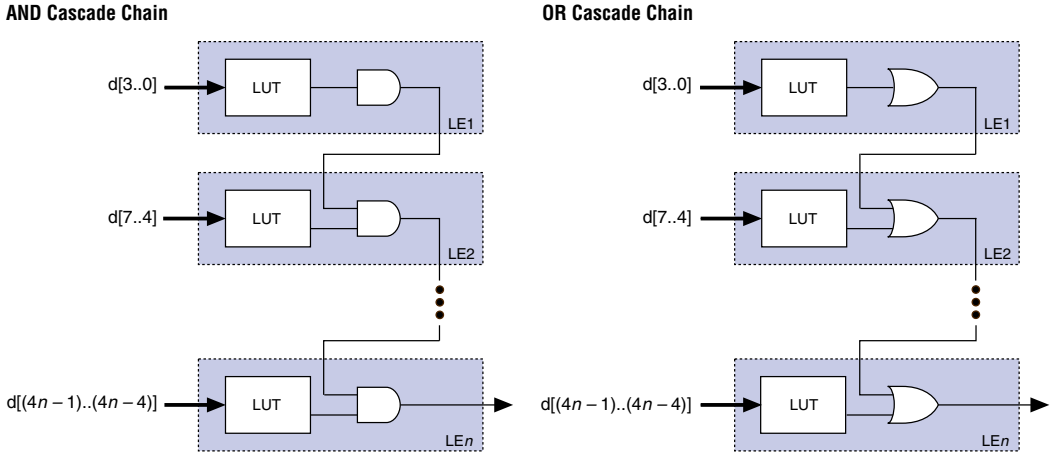
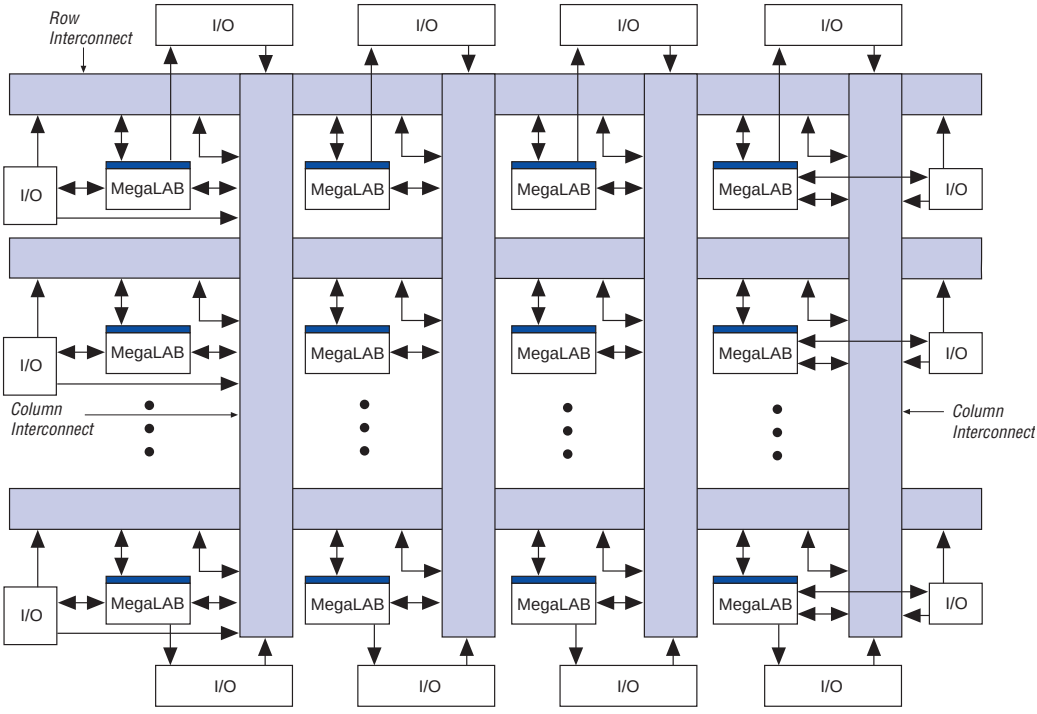


Figure 9. APEX 20K Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 12. APEX 20KE FastRow Interconnect

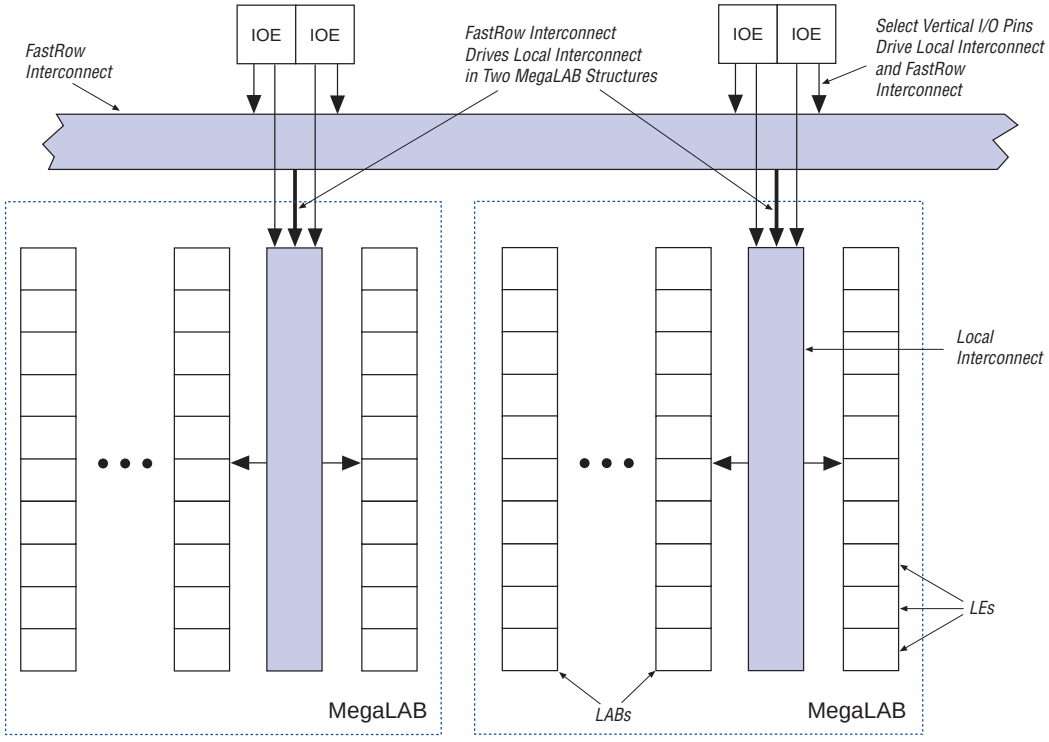
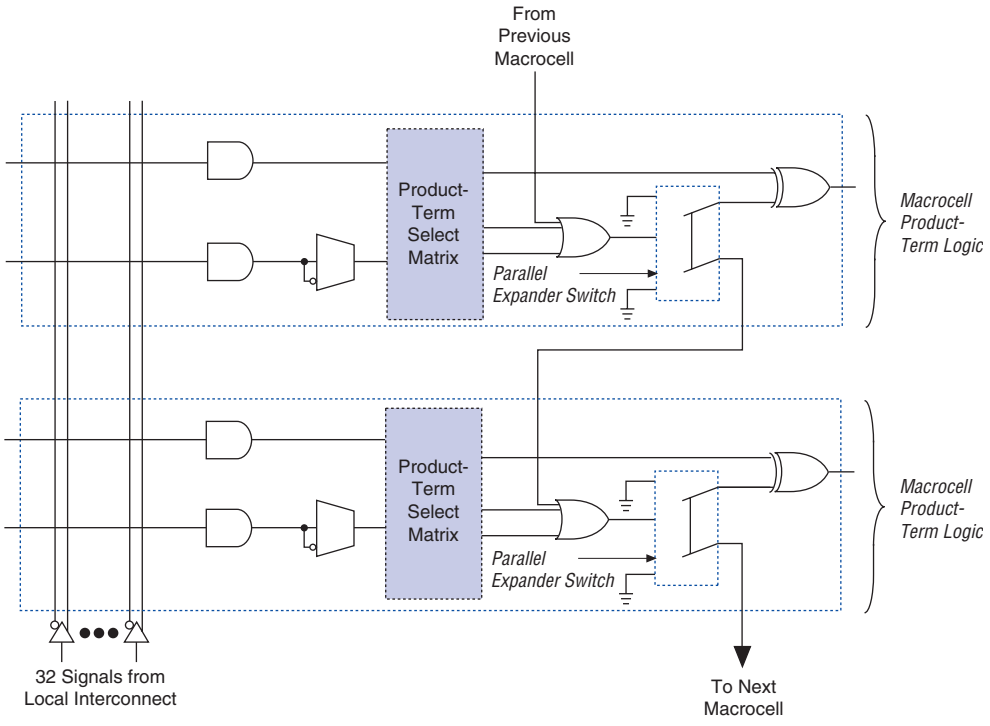


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

Figure 16. APEX 20K Parallel Expanders



Embedded System Block

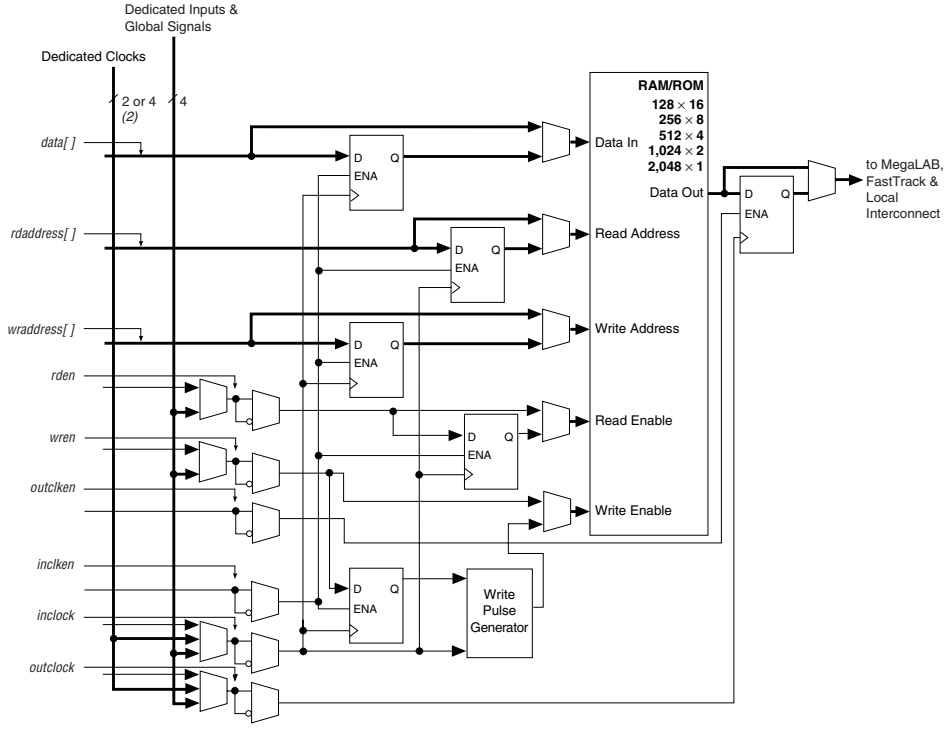
The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

Figure 17. ESB Block Diagram

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode *Note (1)*



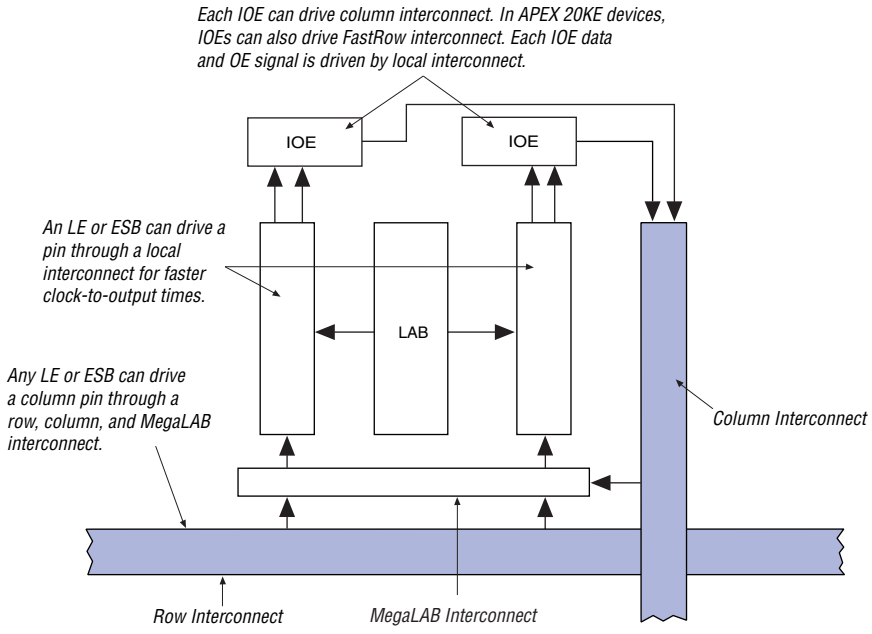
Notes to Figure 21:
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Notes to Table 16:

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus II software, designers must specify the input frequency. The Quartus II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.

(4) The t_{JITTER} specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

Table 17. APEX 20KE ClockLock & ClockBoost Parameters *Note (1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
$t_{INJITTER}$	Input jitter peak-to-peak				2% of input period	peak-to-peak
$t_{OUTJITTER}$	Jitter on ClockLock or ClockBoost-generated clock				0.35% of output period	RMS
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		45		55	%
t_{LOCK} *(2), (3)*	Time required for ClockLock or ClockBoost to acquire lock				40	µs

Table 18. APEX 20KE Clock Input & Output Parameters (Part 2 of 2) Note (1)

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f_{IN}	Input clock frequency	3.3-V LVTTL	1.5	290	1.5	257	MHz
		2.5-V LVTTL	1.5	281	1.5	250	MHz
		1.8-V LVTTL	1.5	272	1.5	243	MHz
		GTL+	1.5	303	1.5	261	MHz
		SSTL-2 Class I	1.5	291	1.5	253	MHz
		SSTL-2 Class II	1.5	291	1.5	253	MHz
		SSTL-3 Class I	1.5	300	1.5	260	MHz
		SSTL-3 Class II	1.5	300	1.5	260	MHz
		LVDS	1.5	420	1.5	350	MHz

Notes to Tables 17 and 18:

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ð f_{VCO} ð 840 MHz for LVDS mode.

SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

Table 30. APEX 20KE Device Capacitance *Note (15)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 27 through 30:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

Vin	Max. Duty Cycle
4.0V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the V_{IH}, V_{IL}, V_{OH}, V_{OL}, and I_I parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance on APEX 20K devices.

Table 39. APEX 20KE External Bidirectional Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{XZBIDIRPLL}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{ZXBIDIRPLL}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

Note to Tables 38 and 39:
(1) These timing parameters are sample-tested only.

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	2.3		2.8		3.2		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	2.3		2.8		3.2		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.0		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.9		2.3		2.6		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t_{INSU} (2)	1.1		1.2		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	2.7	0.5	3.1	–	–	ns

Table 46. EP20K200 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.9		2.3		2.6		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{XZBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{ZXBIDIR}$ (1)		5.0		5.9		6.9	ns
$t_{INSUBIDIR}$ (2)	1.1		1.2		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR}$ (2)		4.3		5.0		–	ns
$t_{ZXBIDIR}$ (2)		4.3		5.0		–	ns

Table 47. EP20K400 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU} (1)	1.4		1.8		2.0		ns
t_{INH} (1)	0.0		0.0		0.0		ns
t_{OUTCO} (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
t_{INSU} (2)	0.4		1.0		–		ns
t_{INH} (2)	0.0		0.0		–		ns
t_{OUTCO} (2)	0.5	3.1	0.5	4.1	–	–	ns

Table 48. EP20K400 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (1)	1.4		1.8		2.0		ns
$t_{INHBIDIR}$ (1)	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$ (1)	2.0	4.9	2.0	6.1	2.0	7.0	ns
$t_{XZBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{ZXBIDIR}$ (1)		7.3		8.9		10.3	ns
$t_{INSUBIDIR}$ (2)	0.5		1.0		–		ns
$t_{INHBIDIR}$ (2)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (2)	0.5	3.1	0.5	4.1	–	–	ns
$t_{XZBIDIR}$ (2)		6.2		7.6		–	ns
$t_{ZXBIDIR}$ (2)		6.2		7.6		–	ns

Table 52. EP20K30E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	0.55		0.78		1.15		ns
t_{CL}	0.55		0.78		1.15		ns
t_{CLRP}	0.22		0.31		0.46		ns
t_{PREP}	0.22		0.31		0.46		ns
t_{ESBCH}	0.55		0.78		1.15		ns
t_{ESBCL}	0.55		0.78		1.15		ns
t_{ESBWP}	1.43		2.01		2.97		ns
t_{ESBRP}	1.15		1.62		2.39		ns

Table 53. EP20K30E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.02		2.13		2.24		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{INSUPLL}$	2.11		2.23		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.88	-	-	ns

Table 54. EP20K30E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.85		1.77		1.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{XZBIDIR}$		7.48		8.46		9.83	ns
$t_{ZXBIDIR}$		7.48		8.46		9.83	ns
$t_{INSUBIDIRPLL}$	4.12		4.24		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.60	0.50	2.88	-	-	ns
$t_{XZBIDIRPLL}$		5.21		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.21		5.99		-	ns

Table 102. EP20K1000E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.22		3.33		3.51		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{XZBIDIR}$		6.31		7.09		7.76	ns
$t_{ZXBIDIR}$		6.31		7.09		7.76	ns
$t_{INSUBIDIRPLL}$	3.25		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.25	0.50	2.99			ns
$t_{XZBIDIRPLL}$		2.81		3.80			ns
$t_{ZXBIDIRPLL}$		2.81		3.80			ns

Tables 103 through 108 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

Table 103. EP20K1500E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.32		0.33	ns
t_{LUT}		0.80		0.95		1.13	ns

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.