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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

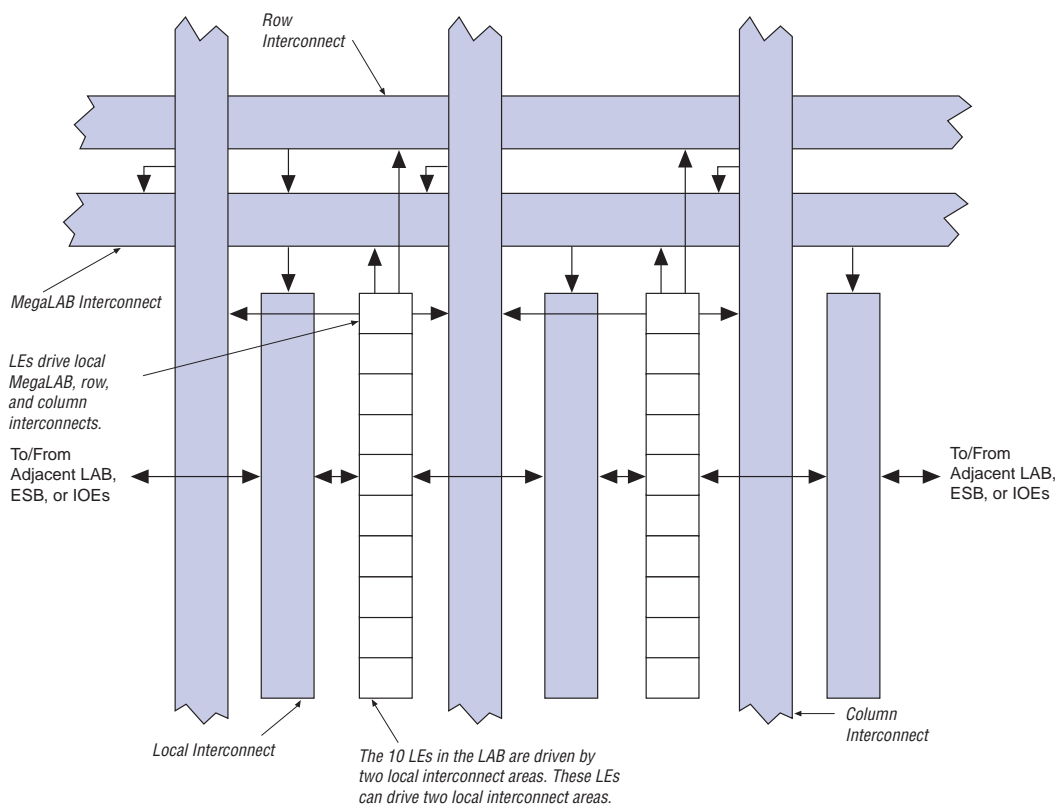
Product Status	Obsolete
Number of LABs/CLBs	640
Number of Logic Elements/Cells	6400
Total RAM Bits	81920
Number of I/O	316
Number of Gates	404000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k160efc484-1xb">https://www.e-xfl.com/product-detail/intel/ep20k160efc484-1xb</a>

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 3. LAB Structure**



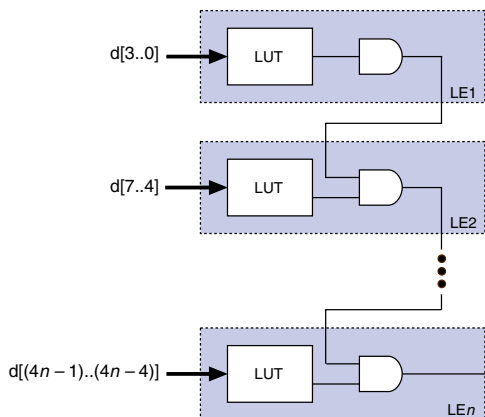
## Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

**Figure 7. APEX 20K Cascade Chain**

**AND Cascade Chain**



**OR Cascade Chain**

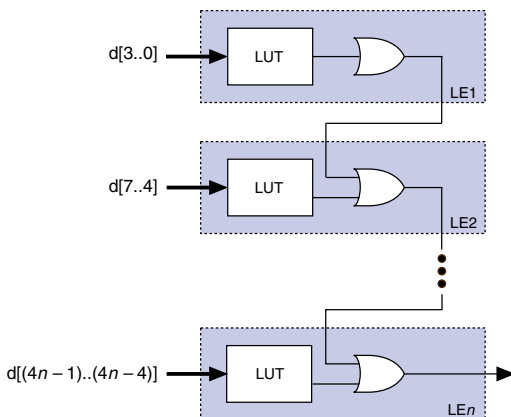


Figure 10. FastTrack Connection to Local Interconnect

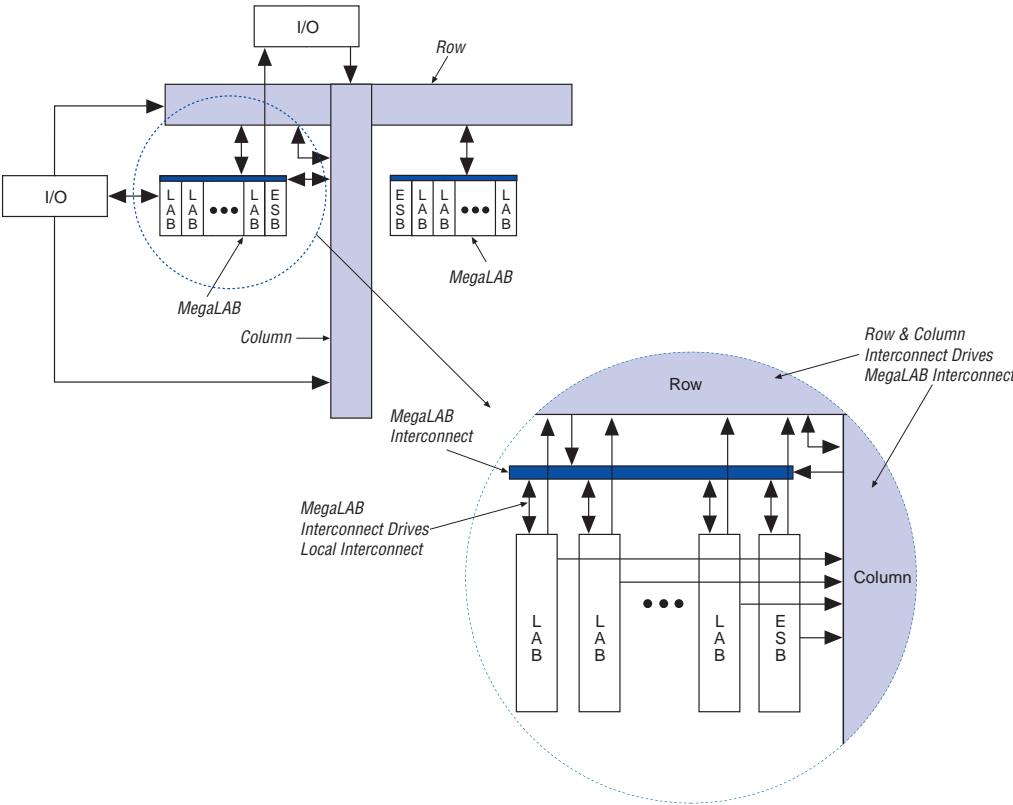


Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

<b>Table 10. APEX 20K Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input pin to core delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Core to output register delay	Decrease input delay to output register
Output register $t_{CO}$ delay	Increase delay to output pin

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

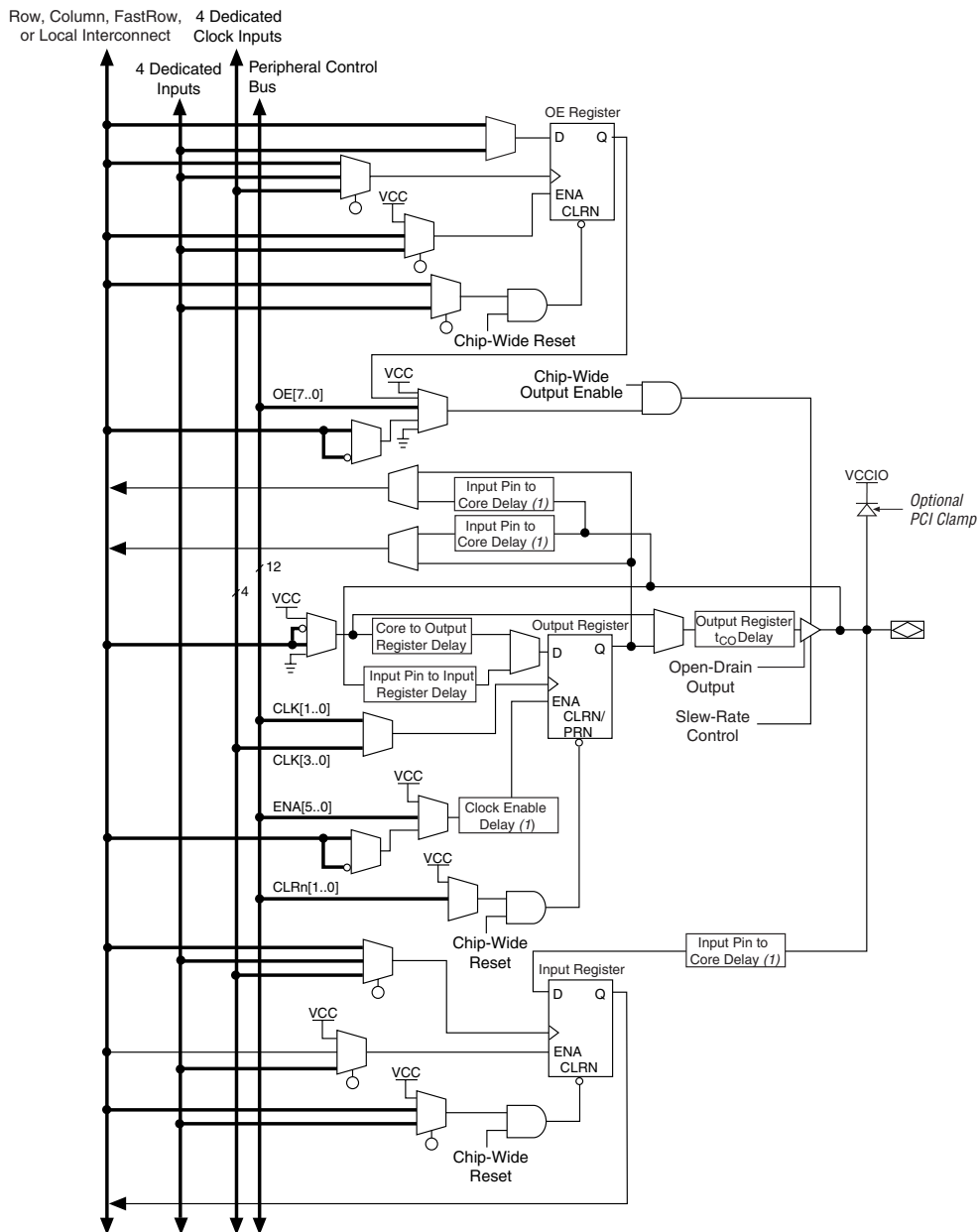
APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

**Table 11** describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

<b>Table 11. APEX 20KE Programmable Delay Chains</b>	
<b>Programmable Delays</b>	<b>Quartus II Logic Option</b>
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register $t_{CO}$ Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. **Figure 26** shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

**Figure 26. APEX 20KE Bidirectional I/O Registers** Notes (1), (2)

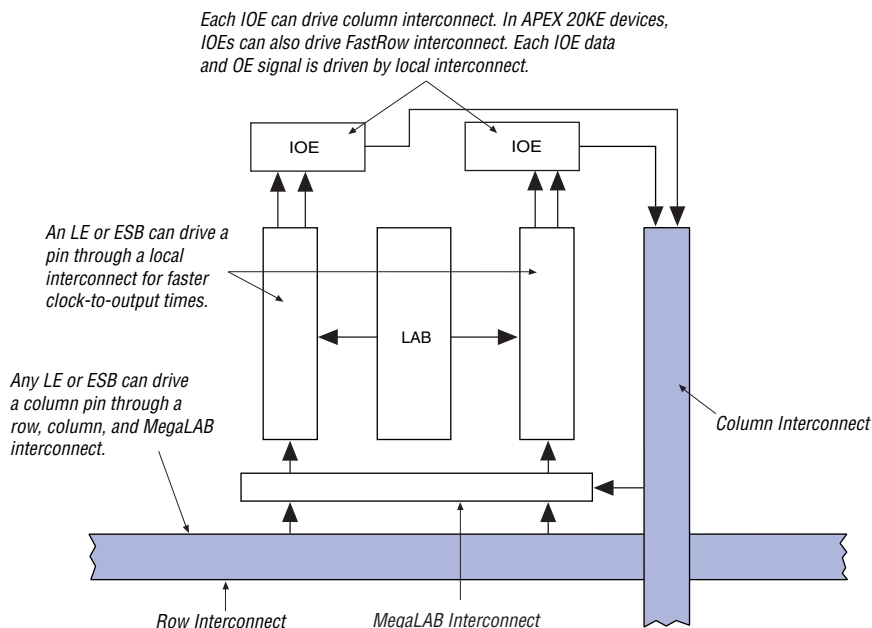


**Notes to Figure 26:**

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Figure 28 shows how a column IOE connects to the interconnect.

**Figure 28. Column IOE Connection to the Interconnect**



## Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.



## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

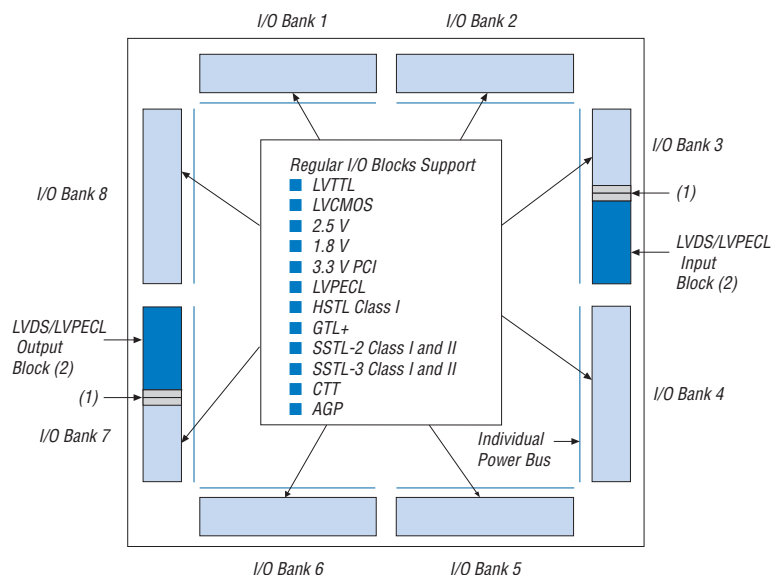


For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate  $V_{REF}$  level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. [Figure 29](#) shows the arrangement of the APEX 20KE I/O banks.

**Figure 29. APEX 20KE I/O Banks**

**Notes to Figure 29:**

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with  $V_{CCIO}$  set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the  $V_{CCIO}$  and  $V_{CCINT}$  power supplies may be powered in any order.



For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

## MultiVolt I/O Interface

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V VCCINT level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

<b>Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support</b>						
<b>V<sub>CCIO</sub> (V)</b>	<b>Input Signals (V)</b>			<b>Output Signals (V)</b>		
	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>	<b>2.5</b>	<b>3.3</b>	<b>5.0</b>
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

**Notes to Table 12:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V<sub>CCIO</sub>.
- (2) When V<sub>CCIO</sub> = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V<sub>IH</sub> of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I<sub>OL</sub> current specification should be considered when selecting a pull-up resistor.

**Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}$ (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
$f_{CLOCK0}$	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
$f_{CLOCK1}$	clock1 PLL output frequency for internal use		20	335	20	200	MHz
$f_{CLOCK0\_EXT}$	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
$f_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

<b>Table 22. APEX 20K JTAG Timing Parameters &amp; Values</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

**Table 26. APEX 20K 5.0-V Tolerant Device Capacitance** *Notes (2), (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 23 through 26:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) All APEX 20K devices are 5.0-V tolerant.
- (3) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{C}$ ,  $V_{CCINT} = 2.5\text{ V}$ , and  $V_{CCIO} = 2.5$  or  $3.3\text{ V}$ .
- (8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
- (9) The APEX 20K input buffers are compatible with  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVC MOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant when  $V_{CCIO}$  and  $V_{CCINT}$  meet the relationship shown in Figure 33 on page 68.
- (10) The  $I_{OH}$  parameter refers to high-level TTL, PCI or CMOS output current.
- (11) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (12) This value is specified for normal device operation. The value may vary during power-up.
- (13) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

**Table 27. APEX 20KE Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage	With respect to ground (2)	$-0.5$	2.5	V
$V_{CCIO}$			$-0.5$	4.6	V
$V_I$			$-0.5$	4.6	V
$I_{OUT}$	DC output current, per pin		$-25$	25	mA
$T_{STG}$	Storage temperature	No bias	$-65$	150	$^\circ\text{C}$
$T_{AMB}$	Ambient temperature	Under bias	$-65$	135	$^\circ\text{C}$
$T_J$	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	$^\circ\text{C}$
		Ceramic PGA packages, under bias		150	$^\circ\text{C}$

Notes to **Tables 43 through 48**:

- (1) This parameter is measured without using ClockLock or ClockBoost circuits.
- (2) This parameter is measured using ClockLock or ClockBoost circuits.

**Tables 49 through 54** describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K30E APEX 20KE devices.

<b>Table 49. EP20K30E <math>f_{MAX}</math> LE Timing Microparameters</b>							
<b>Symbol</b>	<b>-1</b>		<b>-2</b>		<b>-3</b>		<b>Unit</b>
	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
$t_{SU}$	0.01		0.02		0.02		ns
$t_H$	0.11		0.16		0.23		ns
$t_{CO}$		0.32		0.45		0.67	ns
$t_{LUT}$		0.85		1.20		1.77	ns

**Table 57. EP20K60E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns



**Table 60. EP20K60E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.77		2.91		3.11		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{\text{XZBIDIR}}$		6.47		7.44		8.65	ns
$t_{\text{ZXBIDIR}}$		6.47		7.44		8.65	ns
$t_{\text{INSUBIDIRPLL}}$	3.44		3.24		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.37	0.50	3.69	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.00		5.82		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.00		5.82		-	ns

Tables 61 through 66 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

**Table 61. EP20K100E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.25		0.25		0.25		ns
$t_{\text{H}}$	0.25		0.25		0.25		ns
$t_{\text{CO}}$		0.28		0.28		0.34	ns
$t_{\text{LUT}}$		0.80		0.95		1.13	ns

**Table 76. EP20K200E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.36		2.44		2.65		ns
t <sub>CL</sub>	1.36		2.44		2.65		ns
t <sub>CLRP</sub>	0.18		0.19		0.21		ns
t <sub>PREP</sub>	0.18		0.19		0.21		ns
t <sub>ESBCH</sub>	1.36		2.44		2.65		ns
t <sub>ESBCL</sub>	1.36		2.44		2.65		ns
t <sub>ESBWP</sub>	1.18		1.48		1.76		ns
t <sub>ESBRP</sub>	0.95		1.17		1.41		ns

**Table 77. EP20K200E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.24		2.35		2.47		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	5.12	2.00	5.62	2.00	6.11	ns
t <sub>INSUPLL</sub>	2.13		2.07		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	3.01	0.50	3.36	-	-	ns

**Table 86. EP20K400E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		1.91		1.99	ns
$t_{ESBSRC}$		2.30		2.66		2.93	ns
$t_{ESBAWC}$		3.09		3.58		3.99	ns
$t_{ESBSWC}$		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
$t_{ESBWAH}$	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
$t_{ESBWDH}$	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
$t_{ESBDD}$		2.73		3.17		3.58	ns
$t_{PD}$		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns

**Table 87. EP20K400E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.25		0.25		0.26	ns
$t_{F5-20}$		1.01		1.12		1.25	ns
$t_{F20+}$		3.71		3.92		4.17	ns

**Table 88. EP20K400E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.36		2.22		2.35		ns
$t_{CL}$	1.36		2.26		2.35		ns
$t_{CLRP}$	0.18		0.18		0.19		ns
$t_{PREP}$	0.18		0.18		0.19		ns
$t_{ESBCH}$	1.36		2.26		2.35		ns
$t_{ESBCL}$	1.36		2.26		2.35		ns
$t_{ESBWP}$	1.17		1.38		1.56		ns
$t_{ESBRP}$	0.94		1.09		1.25		ns

**Table 89. EP20K400E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.51		2.64		2.77		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

**Table 92. EP20K600E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		2.39		3.11	ns
$t_{ESBSRC}$		2.27		3.07		3.86	ns
$t_{ESBAWC}$		3.19		4.56		5.93	ns
$t_{ESBSWC}$		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATAO1}$		1.01		1.19		1.37	ns
$t_{ESBDATAO2}$		2.18		3.12		4.05	ns
$t_{ESBDD}$		3.19		4.56		5.93	ns
$t_{PD}$		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

**Table 93. EP20K600E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.22		0.25		0.26	ns
$t_{F5-20}$		1.26		1.39		1.52	ns
$t_{F20+}$		3.51		3.88		4.26	ns