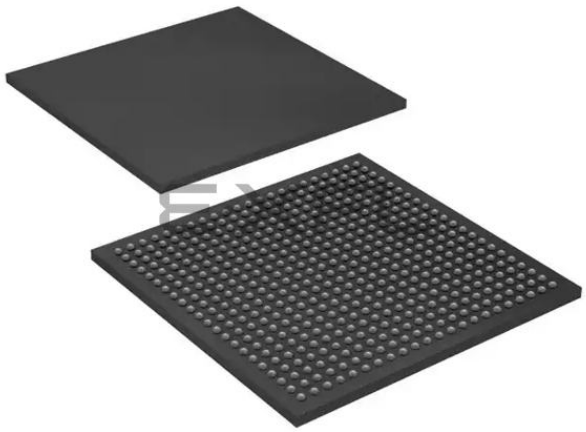

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	640
Number of Logic Elements/Cells	6400
Total RAM Bits	81920
Number of I/O	316
Number of Gates	404000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k160efc484-3

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS)

Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

Table 5. APEX 20K FineLine BGA Package Options & I/O Count *Notes (1), (2)*

Device	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
EP20K30E	93	128			
EP20K60E	93	196			
EP20K100		252			
EP20K100E	93	246			
EP20K160E			316		
EP20K200			382		
EP20K200E			376	376	
EP20K300E				408	
EP20K400				502 *(3)*	
EP20K400E				488 *(3)*	
EP20K600E				508 *(3)*	588
EP20K1000E				508 *(3)*	708
EP20K1500E					808

Notes to Tables 4 and 5:

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

Table 6. APEX 20K QFP, BGA & PGA Package Sizes

Feature	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
Pitch (mm)	0.50	0.50	0.50	1.27	1.27	–
Area (mm^2)	484	924	1,218	1,225	2,025	3,906
Length × Width (mm × mm)	22 × 22	30.4 × 30.4	34.9 × 34.9	35 × 35	45 × 45	62.5 × 62.5

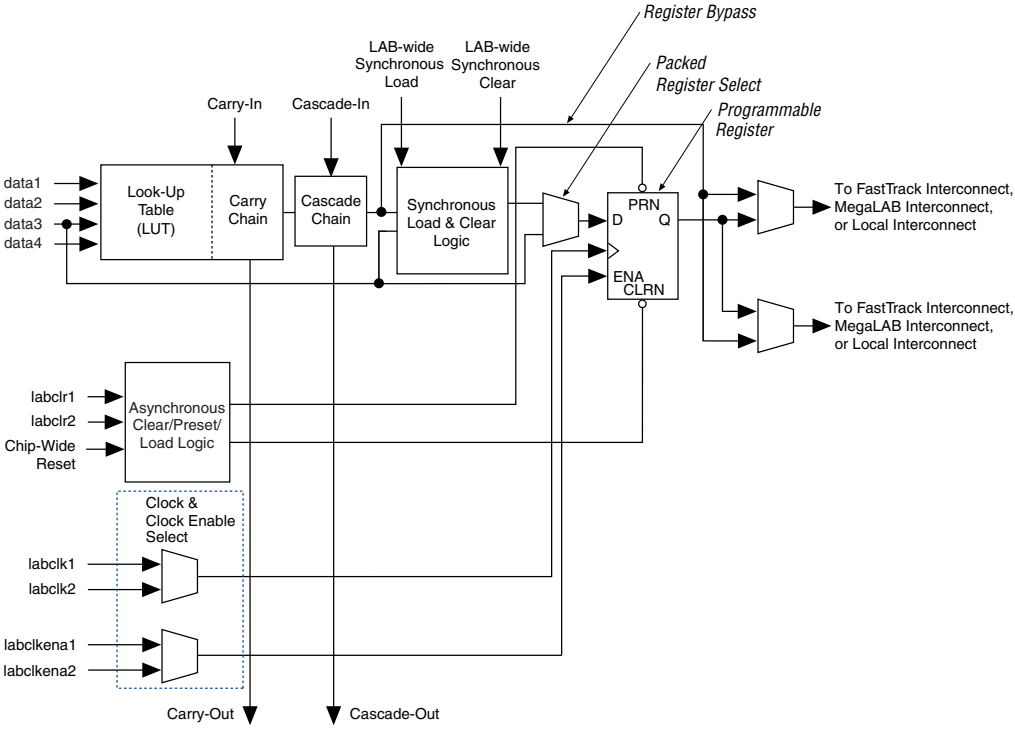
Table 7. APEX 20K FineLine BGA Package Sizes

Feature	144 Pin	324 Pin	484 Pin	672 Pin	1,020 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	169	361	529	729	1,089
Length × Width (mm × mm)	13 × 13	19 × 19	23 × 23	27 × 27	33 × 33

Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

Figure 5. APEX 20K Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Figure 10. FastTrack Connection to Local Interconnect

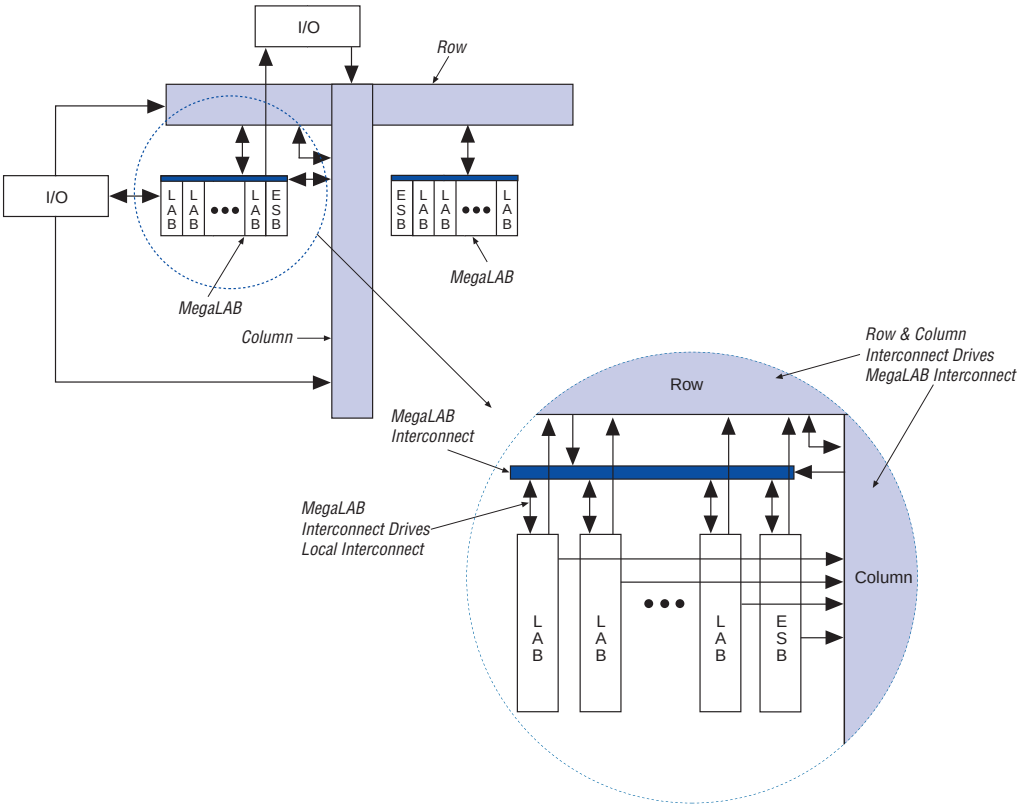
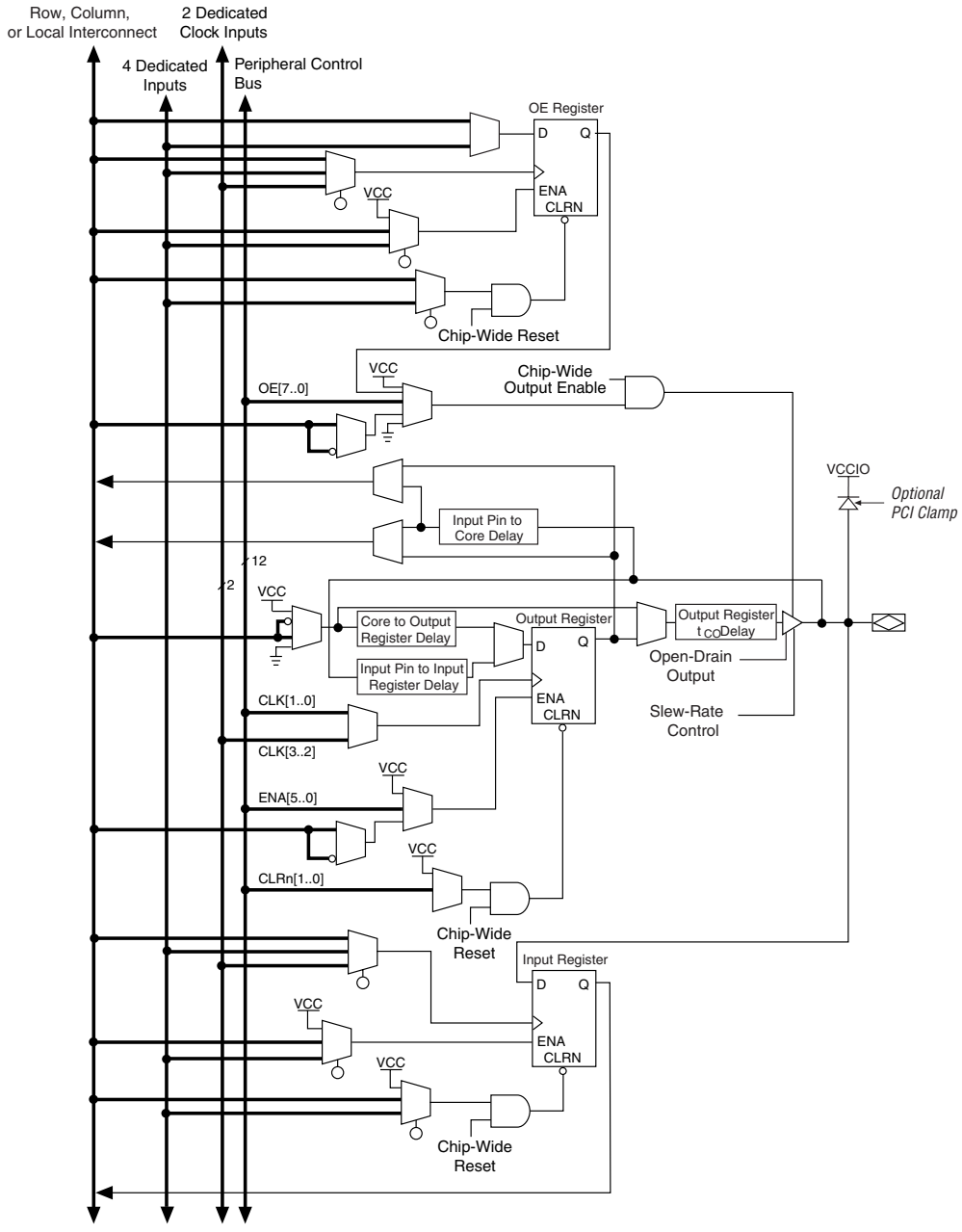


Figure 25. APEX 20K Bidirectional I/O Registers *Note (1)*



Note to Figure 25:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 *(1)*

Note to Table 20:
(1) This device does not support JTAG boundary scan testing.

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

Table 30. APEX 20KE Device Capacitance *Note (15)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 27 through 30:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

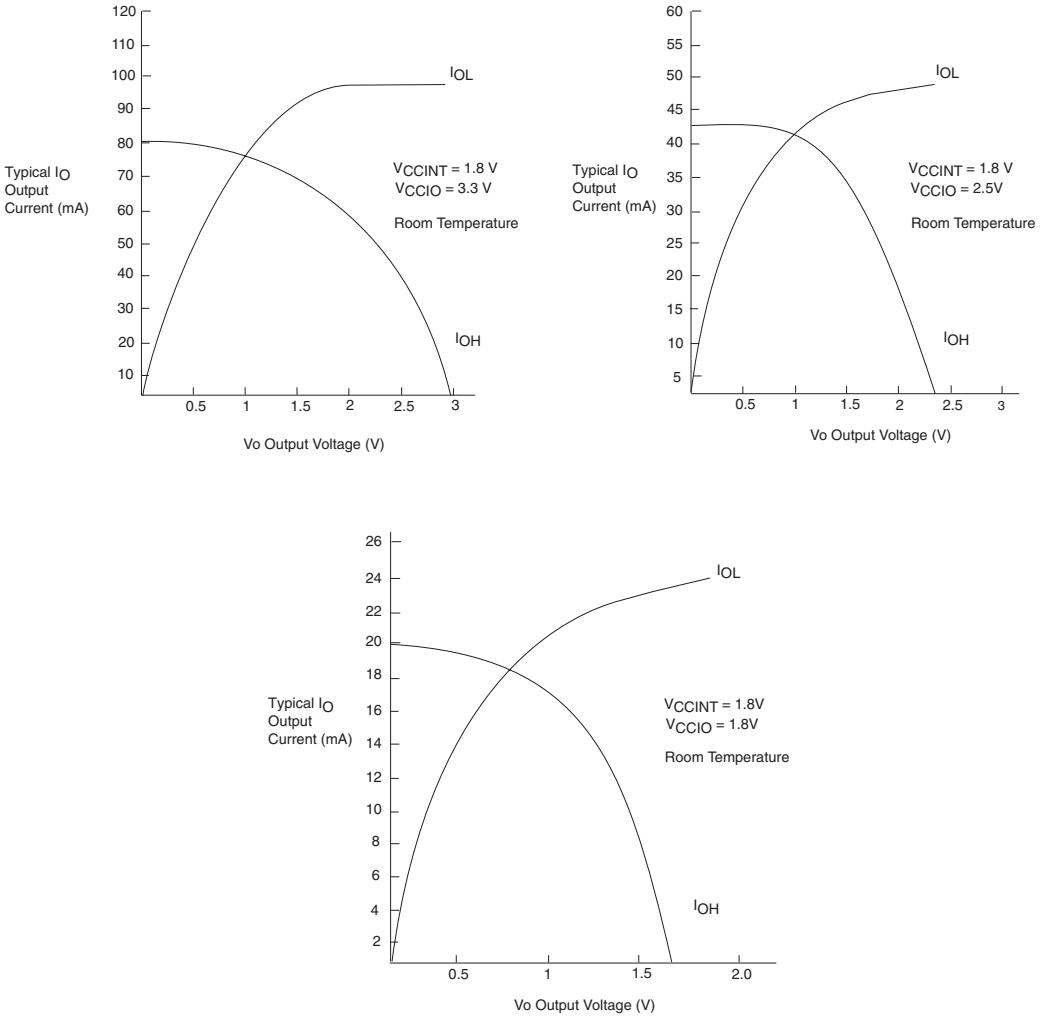
Vin	Max. Duty Cycle
4.0V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the V_{IH}, V_{IL}, V_{OH}, V_{OL}, and I_I parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance on APEX 20K devices.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices *Note (1)*



Note to Figure 35:
(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Table 39. APEX 20KE External Bidirectional Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
$t_{INSUBIDIR}$	Setup time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at LAB adjacent Input Register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE output register	C1 = 10 pF
$t_{XZBIDIR}$	Synchronous Output Enable Register to output buffer disable delay	C1 = 10 pF
$t_{ZXBIDIR}$	Synchronous Output Enable Register output buffer enable delay	C1 = 10 pF
$t_{INSUBIDIRPLL}$	Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{INHBIDIRPLL}$	Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register	
$t_{OUTCOBIDIRPLL}$	Clock-to-output delay for bidirectional pins with PLL clock at IOE output register	C1 = 10 pF
$t_{XZBIDIRPLL}$	Synchronous Output Enable Register to output buffer disable delay with PLL	C1 = 10 pF
$t_{ZXBIDIRPLL}$	Synchronous Output Enable Register output buffer enable delay with PLL	C1 = 10 pF

Note to Tables 38 and 39:
(1) These timing parameters are sample-tested only.

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
$t_{PTERMSU}$	2.3		2.6		3.2		ns
$t_{PTERMCO}$		1.5		1.8		2.1	ns
t_{F1-4}		0.5		0.6		0.7	ns
t_{F5-20}		1.6		1.7		1.8	ns
t_{F20+}		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 56. EP20K60E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.83		2.57		3.79	ns
t_{ESBSRC}		2.46		3.26		4.61	ns
t_{ESBAWC}		3.50		4.90		7.23	ns
t_{ESBSWC}		3.77		4.90		6.79	ns
$t_{ESBWASU}$	1.59		2.23		3.29		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.75		2.46		3.62		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.76		2.47		3.64		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.68		2.49		3.87		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.08		0.43		1.04		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.29		0.72		1.46		ns
$t_{ESBRADDRSU}$	0.36		0.81		1.58		ns
$t_{ESBDATACO1}$		1.06		1.24		1.55	ns
$t_{ESBDATACO2}$		2.39		3.35		4.94	ns
t_{ESBDD}		3.50		4.90		7.23	ns
t_{PD}		1.72		2.41		3.56	ns
$t_{PTERMSU}$	0.99		1.56		2.55		ns
$t_{PTERMCO}$		1.07		1.26		1.08	ns

Table 64. EP20K100E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	2.00		2.00		2.00		ns
t_{CL}	2.00		2.00		2.00		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	2.00		2.00		2.00		ns
t_{ESBCL}	2.00		2.00		2.00		ns
t_{ESBWP}	1.29		1.53		1.66		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 65. EP20K100E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.23		2.32		2.43		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.86	2.00	5.35	2.00	5.84	ns
$t_{INSUPLL}$	1.58		1.66		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.96	0.50	3.29	-	-	ns

Table 66. EP20K100E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.74		2.96		3.19		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.86	2.00	5.35	2.00	5.84	ns
$t_{XZBIDIR}$		5.00		5.48		5.89	ns
$t_{ZXBIDIR}$		5.00		5.48		5.89	ns
$t_{INSUBIDIRPLL}$	4.64		5.03		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.96	0.50	3.29	-	-	ns
$t_{XZBIDIRPLL}$		3.10		3.42		-	ns
$t_{ZXBIDIRPLL}$		3.10		3.42		-	ns

Table 74. EP20K200E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.68		2.06		2.24	ns
t_{ESBSRC}		2.27		2.77		3.18	ns
t_{ESBAWC}		3.10		3.86		4.50	ns
t_{ESBSWC}		2.90		3.67		4.21	ns
$t_{ESBWASU}$	0.55		0.67		0.74		ns
t_{ESBWAH}	0.36		0.46		0.48		ns
$t_{ESBWDSU}$	0.69		0.83		0.95		ns
t_{ESBWDH}	0.36		0.46		0.48		ns
$t_{ESBRASU}$	1.61		1.90		2.09		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.42		1.71		2.01		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.06		-0.07		0.05		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.13		0.31		ns
$t_{ESBRADDRSU}$	0.18		0.23		0.39		ns
$t_{ESBDATACO1}$		1.09		1.35		1.51	ns
$t_{ESBDATACO2}$		2.19		2.75		3.22	ns
t_{ESBDD}		2.75		3.41		4.03	ns
t_{PD}		1.58		1.97		2.33	ns
$t_{PTERMSU}$	1.00		1.22		1.51		ns
$t_{PTERMCO}$		1.10		1.37		1.09	ns

Table 75. EP20K200E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.27		0.29	ns
t_{F5-20}		1.02		1.20		1.41	ns
t_{F20+}		1.99		2.23		2.53	ns

Table 80. EP20K300E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.79		2.44		3.25	ns
t_{ESBSRC}		2.40		3.12		4.01	ns
t_{ESBAWC}		3.41		4.65		6.20	ns
t_{ESBSWC}		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
t_{ESBDD}		3.41		4.65		6.20	ns
t_{PD}		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

Table 81. EP20K300E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.24		0.26	ns
t_{F5-20}		1.33		1.43		1.58	ns
t_{F20+}		3.63		3.93		4.35	ns

Table 82. EP20K300E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.19		0.26		0.35		ns
t_{PREP}	0.19		0.26		0.35		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.25		1.71		2.28		ns
t_{ESBRP}	1.01		1.38		1.84		ns

Table 83. EP20K300E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.31		2.44		2.57		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.29	2.00	5.82	2.00	6.24	ns
$t_{INSUPLL}$	1.76		1.85		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.65	0.50	2.95	-	-	ns

Table 84. EP20K300E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.77		2.85		3.11		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.29	2.00	5.82	2.00	6.24	ns
$t_{XZBIDIR}$		7.59		8.30		9.09	ns
$t_{ZXBIDIR}$		7.59		8.30		9.09	ns
$t_{INSUBIDIRPLL}$	2.50		2.76		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.65	0.50	2.95	-	-	ns
$t_{XZBIDIRPLL}$		5.00		5.43		-	ns
$t_{ZXBIDIRPLL}$		5.00		5.43		-	ns

Table 87. EP20K400E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.25		0.26	ns
t_{F5-20}		1.01		1.12		1.25	ns
t_{F20+}		3.71		3.92		4.17	ns

Table 88. EP20K400E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.22		2.35		ns
t_{CL}	1.36		2.26		2.35		ns
t_{CLRP}	0.18		0.18		0.19		ns
t_{PREP}	0.18		0.18		0.19		ns
t_{ESBCH}	1.36		2.26		2.35		ns
t_{ESBCL}	1.36		2.26		2.35		ns
t_{ESBWP}	1.17		1.38		1.56		ns
t_{ESBRP}	0.94		1.09		1.25		ns

Table 89. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.51		2.64		2.77		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

Table 99. EP20K1000E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.27		0.27		0.27	ns
t_{F5-20}		1.45		1.63		1.75	ns
t_{F20+}		4.15		4.33		4.97	ns

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 101. EP20K1000E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.70		2.84		2.97		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{INSUPLL}$	1.64		2.09		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns

Table 102. EP20K1000E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.22		3.33		3.51		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{XZBIDIR}$		6.31		7.09		7.76	ns
$t_{ZXBIDIR}$		6.31		7.09		7.76	ns
$t_{INSUBIDIRPLL}$	3.25		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.25	0.50	2.99			ns
$t_{XZBIDIRPLL}$		2.81		3.80			ns
$t_{ZXBIDIRPLL}$		2.81		3.80			ns

Tables 103 through 108 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

Table 103. EP20K1500E f_{MAX} LE Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.32		0.33	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 104. EP20K1500E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 105. EP20K1500E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.28		0.28		0.28	ns
t_{F5-20}		1.36		1.50		1.62	ns
t_{F20+}		4.43		4.48		5.07	ns