# Intel - EP20K160EQC208-2N Datasheet

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 640 |
| Number of Logic Elements/Cells | 6400 |
| Total RAM Bits | 81920 |
| Number of I/O | 143 |
| Number of Gates | 404000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k160eqc208-2n |

### Table 8. Comparison of APEX 20K & APEX 20KE Features

| Feature | APEX 20K Devices | APEX 20KE Devices |
|---|---|---|
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

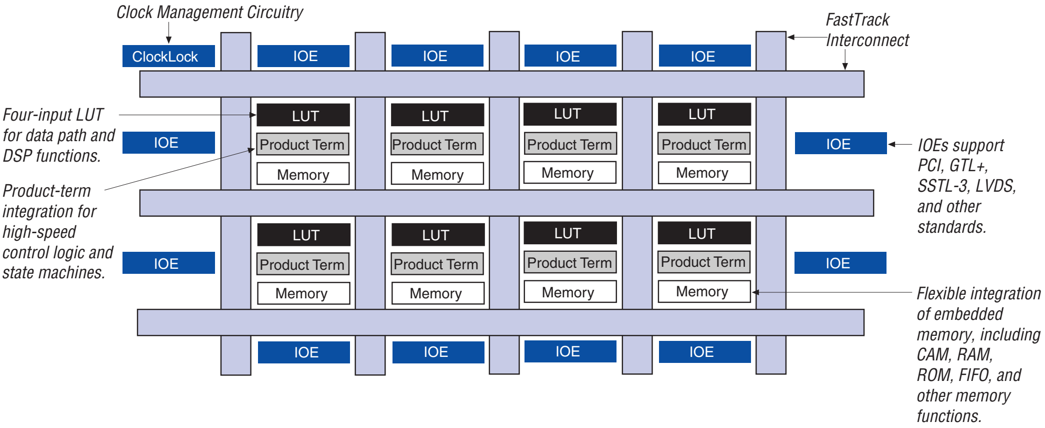
## Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

*Figure 1. APEX 20K Device Block Diagram*

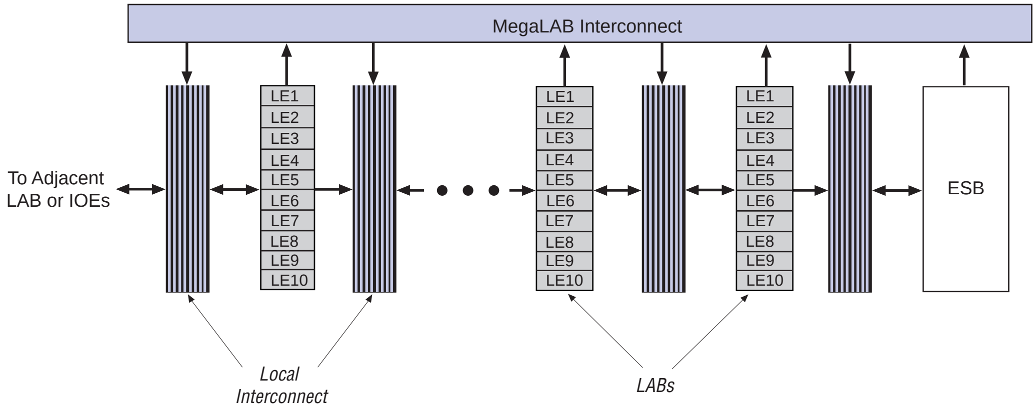


APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

## MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

*Figure 2. MegaLAB Structure*

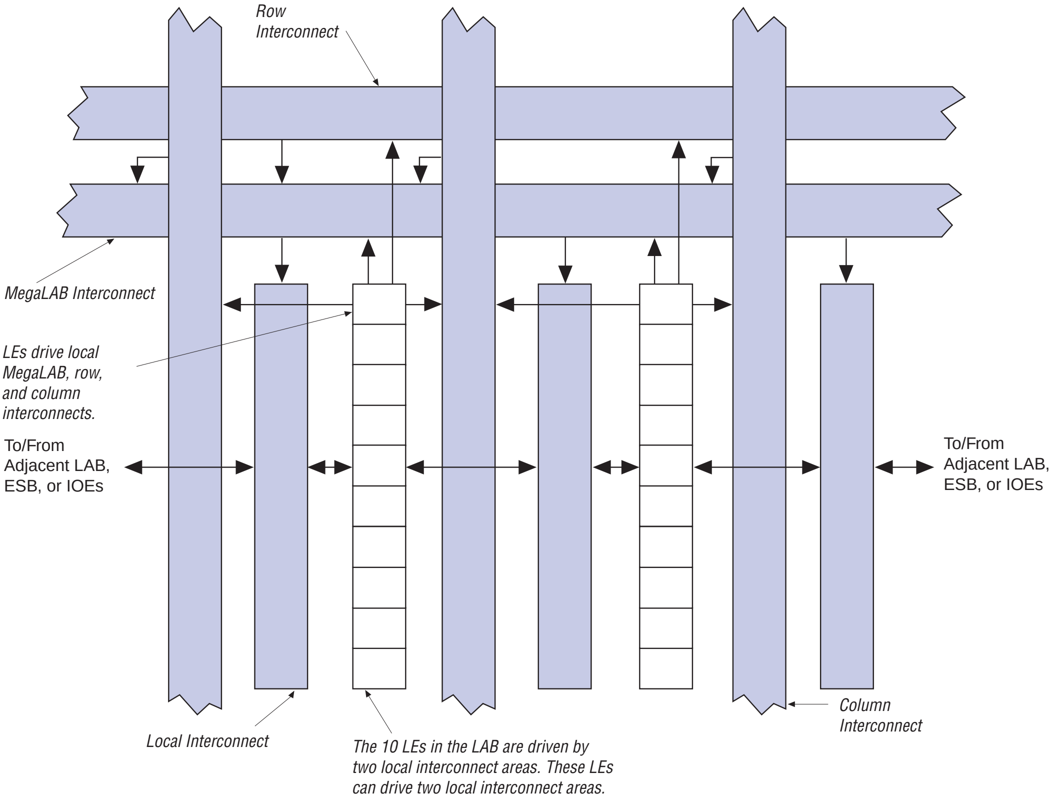


## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

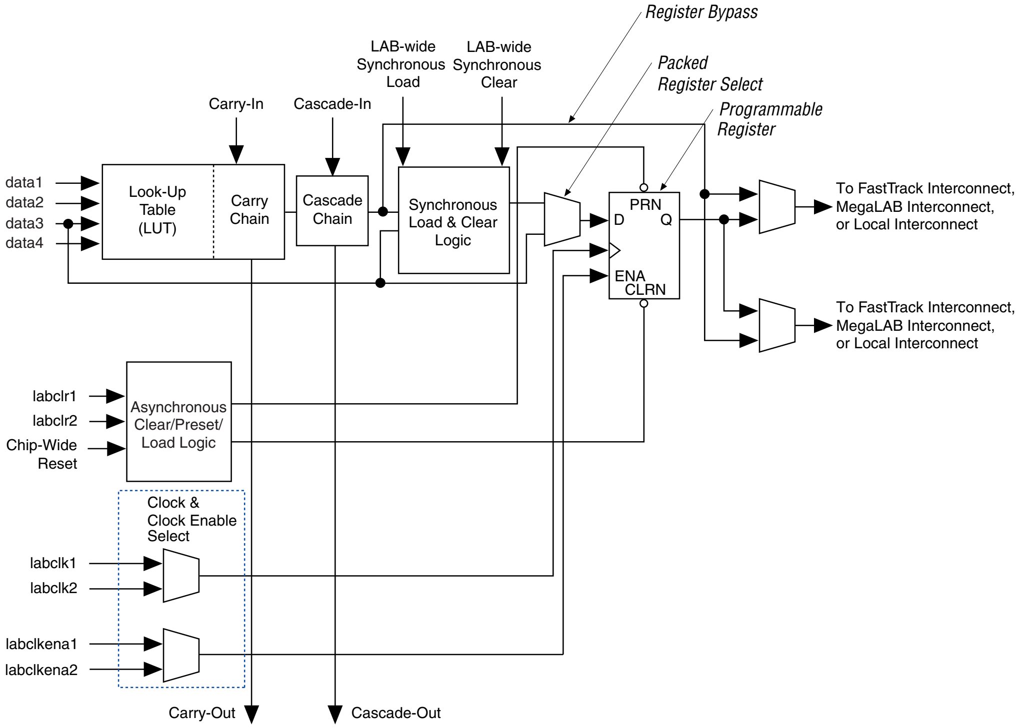
*Figure 3. LAB Structure*



## Logic Element

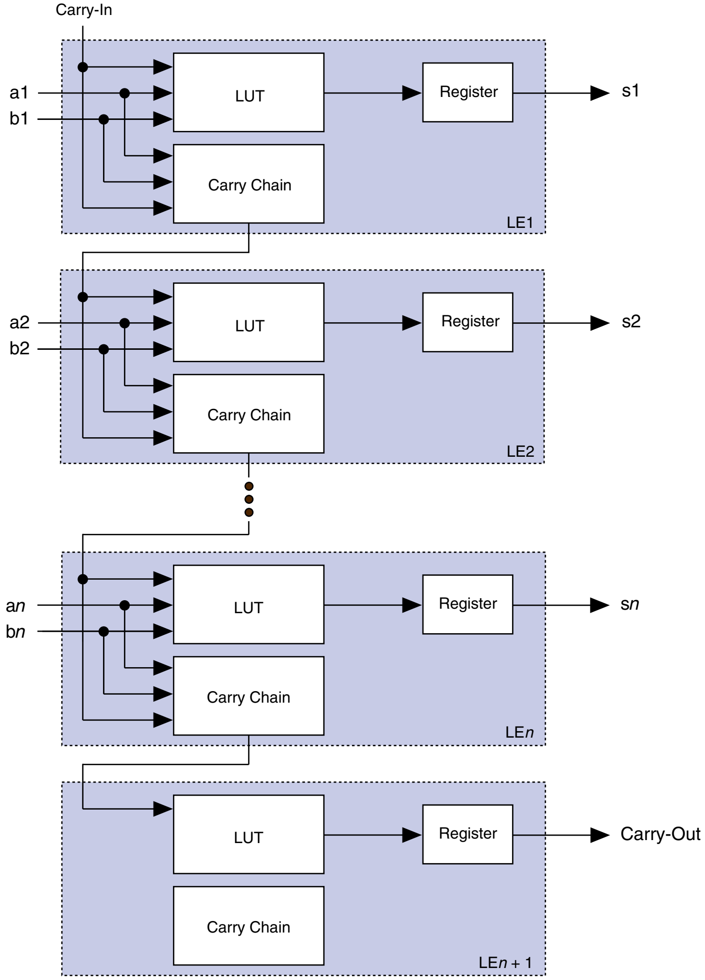
The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

*Figure 5. APEX 20K Logic Element*



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

*Figure 6. APEX 20K Carry Chain*



### Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

### Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE `VCCINT` pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the `VCCIO` pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When `VCCIO` pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

**Table 13. APEX 20KE MultiVolt I/O Support** *Note (1)*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | *(2)* | | | ✓ *(3)* | |

*Notes to Table 13:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

*Table 18. APEX 20KE Clock Input & Output Parameters (Part 2 of 2) Note (1)*

| Symbol | Parameter | I/O Standard | -1X Speed Grade | | -2X Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{IN}$ | Input clock frequency | 3.3-V LVTTL | 1.5 | 290 | 1.5 | 257 | MHz |
| | | 2.5-V LVTTL | 1.5 | 281 | 1.5 | 250 | MHz |
| | | 1.8-V LVTTL | 1.5 | 272 | 1.5 | 243 | MHz |
| | | GTL+ | 1.5 | 303 | 1.5 | 261 | MHz |
| | | SSTL-2 Class I | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-2 Class II | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-3 Class I | 1.5 | 300 | 1.5 | 260 | MHz |
| | | SSTL-3 Class II | 1.5 | 300 | 1.5 | 260 | MHz |
| | | LVDS | 1.5 | 420 | 1.5 | 350 | MHz |

*Notes to Tables 17 and 18:*

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.

(2) The maximum lock time is 40 µs or 2000 input clock cycles, whichever occurs first.

(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.

(4) The PLL VCO operating range is 200 MHz ð $f_{VCO}$ ð 840 MHz for LVDS mode.

## SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

**Table 29. APEX 20KE Device DC Operating Conditions** *Notes (7), (8), (9)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level LVTTL, CMOS, or 3.3-V PCI input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(10)* | | 4.1 | V |
| $V_{IL}$ | Low-level LVTTL, CMOS, or 3.3-V PCI input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(10)* | V |
| $V_{OH}$ | 3.3-V high-level LVTTL output voltage | $I_{OH}$ = –12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | 2.4 | | | V |
| | 3.3-V high-level LVCMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(11)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level LVTTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(12)* | | | 0.4 | V |
| | 3.3-V low-level LVCMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(12)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(12)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 4.1 to –0.5 V *(13)* | –10 | | 10 | μA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 4.1 to –0.5 V *(13)* | –10 | | 10 | μA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(14)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(14)* | 30 | | 80 | kΩ |
| | | $V_{CCIO}$ = 1.71 V *(14)* | 60 | | 150 | kΩ |

☞ For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

**Table 30. APEX 20KE Device Capacitance** *Note (15)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 27 through 30:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

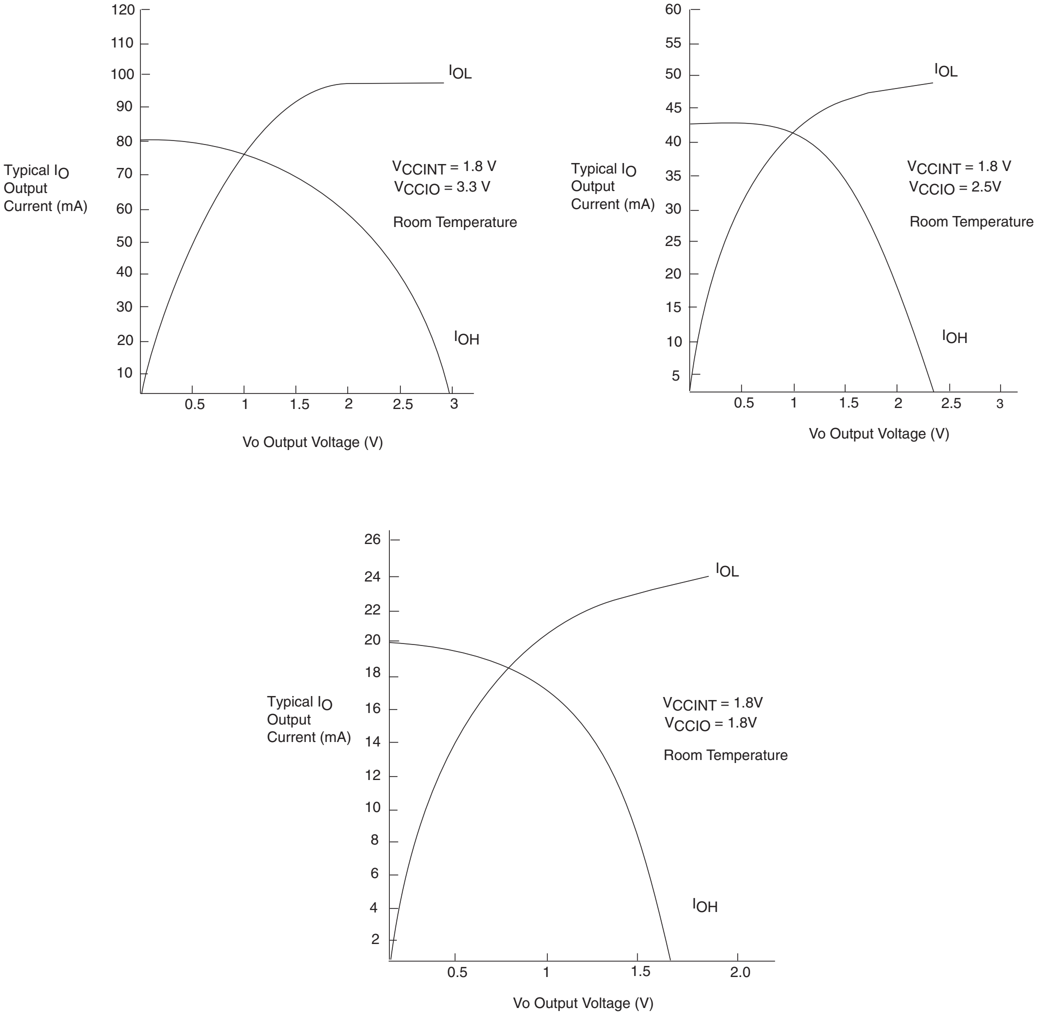
| Vin | Max. Duty Cycle |
|---|---|
| 4.0V | 100% (DC) |
| 4.1 | 90% |
| 4.2 | 50% |
| 4.3 | 30% |
| 4.4 | 17% |
| 4.5 | 10% |

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, and $I_I$ parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

***Figure 35. Output Drive Characteristics of APEX 20KE Devices*** *Note (1)*



***Note to Figure 35:***

(1) These are transient (AC) currents.

## Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Tables 40 through 42 show the $f_{MAX}$ timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 40. EP20K100 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.6 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

### *Table 46. EP20K200 External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(1)* | 1.9 | | 2.3 | | 2.6 | | ns |
| $t_{INHBIDIR}$ *(1)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ *(1)* | 2.0 | 4.6 | 2.0 | 5.6 | 2.0 | 6.8 | ns |
| $t_{XZBIDIR}$ *(1)* | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{ZXBIDIR}$ *(1)* | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{INSUBIDIR}$ *(2)* | 1.1 | | 1.2 | | – | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 0.5 | 2.7 | 0.5 | 3.1 | – | – | ns |
| $t_{XZBIDIR}$ *(2)* | | 4.3 | | 5.0 | | – | ns |
| $t_{ZXBIDIR}$ *(2)* | | 4.3 | | 5.0 | | – | ns |

### *Table 47. EP20K400 External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ *(1)* | 1.4 | | 1.8 | | 2.0 | | ns |
| $t_{INH}$ *(1)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(1)* | 2.0 | 4.9 | 2.0 | 6.1 | 2.0 | 7.0 | ns |
| $t_{INSU}$ *(2)* | 0.4 | | 1.0 | | – | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ *(2)* | 0.5 | 3.1 | 0.5 | 4.1 | – | – | ns |

### *Table 48. EP20K400 External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(1)* | 1.4 | | 1.8 | | 2.0 | | ns |
| $t_{INHBIDIR}$ *(1)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ *(1)* | 2.0 | 4.9 | 2.0 | 6.1 | 2.0 | 7.0 | ns |
| $t_{XZBIDIR}$ *(1)* | | 7.3 | | 8.9 | | 10.3 | ns |
| $t_{ZXBIDIR}$ *(1)* | | 7.3 | | 8.9 | | 10.3 | ns |
| $t_{INSUBIDIR}$ *(2)* | 0.5 | | 1.0 | | – | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 0.5 | 3.1 | 0.5 | 4.1 | – | – | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.2 | | 7.6 | | – | ns |
| $t_{ZXBIDIR}$ *(2)* | | 6.2 | | 7.6 | | – | ns |

| *Table 62. EP20K100E $f_{MAX}$ ESB Timing Microparameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1** | | **-2** | | **-3** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{ESBARC}$ | | 1.61 | | 1.84 | | 1.97 | ns |
| $t_{ESBSRC}$ | | 2.57 | | 2.97 | | 3.20 | ns |
| $t_{ESBAWC}$ | | 0.52 | | 4.09 | | 4.39 | ns |
| $t_{ESBSWC}$ | | 3.17 | | 3.78 | | 4.09 | ns |
| $t_{ESBWASU}$ | 0.56 | | 6.41 | | 0.63 | | ns |
| $t_{ESBWAH}$ | 0.48 | | 0.54 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.71 | | 0.80 | | 0.81 | | ns |
| $t_{ESBWDH}$ | .048 | | 0.54 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.57 | | 1.75 | | 1.87 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.20 | | ns |
| $t_{ESBWESU}$ | 1.54 | | 1.72 | | 1.80 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.16 | | -0.20 | | -0.20 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.12 | | 0.08 | | 0.13 | | ns |
| $t_{ESBRADDRSU}$ | 0.17 | | 0.15 | | 0.19 | | ns |
| $t_{ESBDATACO1}$ | | 1.20 | | 1.39 | | 1.52 | ns |
| $t_{ESBDATACO2}$ | | 2.54 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.06 | | 3.56 | | 3.85 | ns |
| $t_{PD}$ | | 1.73 | | 2.02 | | 2.20 | ns |
| $t_{PTERMSU}$ | 1.11 | | 1.26 | | 1.38 | | ns |
| $t_{PTERMCO}$ | | 1.19 | | 1.40 | | 1.08 | ns |

| *Table 63. EP20K100E $f_{MAX}$ Routing Delays* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1** | | **-2** | | **-3** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.04 | | 1.26 | | 1.52 | ns |
| $t_{F20+}$ | | 1.12 | | 1.36 | | 1.86 | ns |

*Table 68. EP20K160E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.65 | | 2.02 | | 2.11 | ns |
| $t_{ESBSRC}$ | | 2.21 | | 2.70 | | 3.11 | ns |
| $t_{ESBAWC}$ | | 3.04 | | 3.79 | | 4.42 | ns |
| $t_{ESBSWC}$ | | 2.81 | | 3.56 | | 4.10 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.66 | | 0.73 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.45 | | 0.47 | | ns |
| $t_{ESBWDSU}$ | 0.68 | | 0.81 | | 0.94 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.45 | | 0.47 | | ns |
| $t_{ESBRASU}$ | 1.58 | | 1.87 | | 2.06 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.41 | | 1.71 | | 2.00 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.02 | | -0.03 | | 0.09 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.14 | | 0.17 | | 0.35 | | ns |
| $t_{ESBRADDRSU}$ | 0.21 | | 0.27 | | 0.43 | | ns |
| $t_{ESBDATACO1}$ | | 1.04 | | 1.30 | | 1.46 | ns |
| $t_{ESBDATACO2}$ | | 2.15 | | 2.70 | | 3.16 | ns |
| $t_{ESBDD}$ | | 2.69 | | 3.35 | | 3.97 | ns |
| $t_{PD}$ | | 1.55 | | 1.93 | | 2.29 | ns |
| $t_{PTERMSU}$ | 1.01 | | 1.23 | | 1.52 | | ns |
| $t_{PTERMCO}$ | | 1.06 | | 1.32 | | 1.04 | ns |

*Table 69. EP20K160E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.26 | | 0.28 | ns |
| $t_{F5-20}$ | | 1.00 | | 1.18 | | 1.35 | ns |
| $t_{F20+}$ | | 1.95 | | 2.19 | | 2.30 | ns |

*Table 70. EP20K160E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{CL}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{PREP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{ESBCH}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{ESBCL}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{ESBWP}$ | 1.15 | | 1.45 | | 1.73 | | ns |
| $t_{ESBRP}$ | 0.93 | | 1.15 | | 1.38 | | ns |

*Table 71. EP20K160E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.23 | | 2.34 | | 2.47 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{INSUPLL}$ | 2.12 | | 2.07 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |

**Table 90. EP20K400E External Bidirectional Timing Parameters**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.93 | | 3.23 | | 3.44 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.25 | 2.00 | 5.79 | 2.00 | 6.32 | ns |
| $t_{XZBIDIR}$ | | 5.95 | | 6.77 | | 7.12 | ns |
| $t_{ZXBIDIR}$ | | 5.95 | | 6.77 | | 7.12 | ns |
| $t_{INSUBIDIRPLL}$ | 4.31 | | 4.76 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.45 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 2.94 | | 3.43 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 2.94 | | 3.43 | | - | ns |

Tables 91 through 96 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K600E APEX 20KE devices.

**Table 91. EP20K600E $f_{MAX}$ LE Timing Microparameters**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.16 | | 0.17 | | ns |
| $t_{H}$ | 0.29 | | 0.33 | | 0.37 | | ns |
| $t_{CO}$ | | 0.65 | | 0.38 | | 0.49 | ns |
| $t_{LUT}$ | | 0.70 | | 1.00 | | 1.30 | ns |

**Table 99. EP20K1000E $f_{MAX}$ Routing Delays**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.27 | | 0.27 | | 0.27 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.63 | | 1.75 | ns |
| $t_{F20+}$ | | 4.15 | | 4.33 | | 4.97 | ns |

**Table 100. EP20K1000E Minimum Pulse Width Timing Parameters**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

**Table 101. EP20K1000E External Timing Parameters**

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.70 | | 2.84 | | 2.97 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{INSUPLL}$ | 1.64 | | 2.09 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | - | - | ns |

*Table 102. EP20K1000E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 3.22 | | 3.33 | | 3.51 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{XZBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{ZXBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{INSUBIDIRPL}$L | 3.25 | | 3.26 | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | | | ns |
| $t_{XZBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |
| $t_{ZXBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |

Tables 103 through 108 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

*Table 103. EP20K1500E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |