Welcome to E-XFL.COM

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 640 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 143 |
| Number of Gates | - |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k160eqc208-2x |

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock® feature reducing clock delay and skew
  - ClockBoost® feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ($\mathbf{t_{CO}} + \mathbf{t_{SU}}$) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast $t_{CO}$ and $t_{SU}$ times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - Programmable clamp to $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
  - FineLine BGA® packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus® II development system for

| *Table 5. APEX 20K FineLine BGA Package Options & I/O Count* *Notes (1), (2)* | | | | | |
|---|---|---|---|---|---|
| **Device** | **144 Pin** | **324 Pin** | **484 Pin** | **672 Pin** | **1,020 Pin** |
| EP20K30E | 93 | 128 | | | |
| EP20K60E | 93 | 196 | | | |
| EP20K100 | | 252 | | | |
| EP20K100E | 93 | 246 | | | |
| EP20K160E | | | 316 | | |
| EP20K200 | | | 382 | | |
| EP20K200E | | | 376 | 376 | |
| EP20K300E | | | | 408 | |
| EP20K400 | | | | 502 *(3)* | |
| EP20K400E | | | | 488 *(3)* | |
| EP20K600E | | | | 508 *(3)* | 588 |
| EP20K1000E | | | | 508 *(3)* | 708 |
| EP20K1500E | | | | | 808 |

*Notes to Tables 4 and 5:*
(1) I/O counts include dedicated input and clock pins.
(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.
(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

| *Table 6. APEX 20K QFP, BGA & PGA Package Sizes* | | | | | | |
|---|---|---|---|---|---|---|
| **Feature** | **144-Pin TQFP** | **208-Pin QFP** | **240-Pin QFP** | **356-Pin BGA** | **652-Pin BGA** | **655-Pin PGA** |
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.27 | 1.27 | – |
| Area ($mm^2$) | 484 | 924 | 1,218 | 1,225 | 2,025 | 3,906 |
| Length × Width (mm × mm) | 22 × 22 | 30.4 × 30.4 | 34.9 × 34.9 | 35 × 35 | 45 × 45 | 62.5 × 62.5 |

| *Table 7. APEX 20K FineLine BGA Package Sizes* | | | | | |
|---|---|---|---|---|---|
| **Feature** | **144 Pin** | **324 Pin** | **484 Pin** | **672 Pin** | **1,020 Pin** |
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 169 | 361 | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 13 × 13 | 19 × 19 | 23 × 23 | 27 × 27 | 33 × 33 |

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 3. LAB Structure**

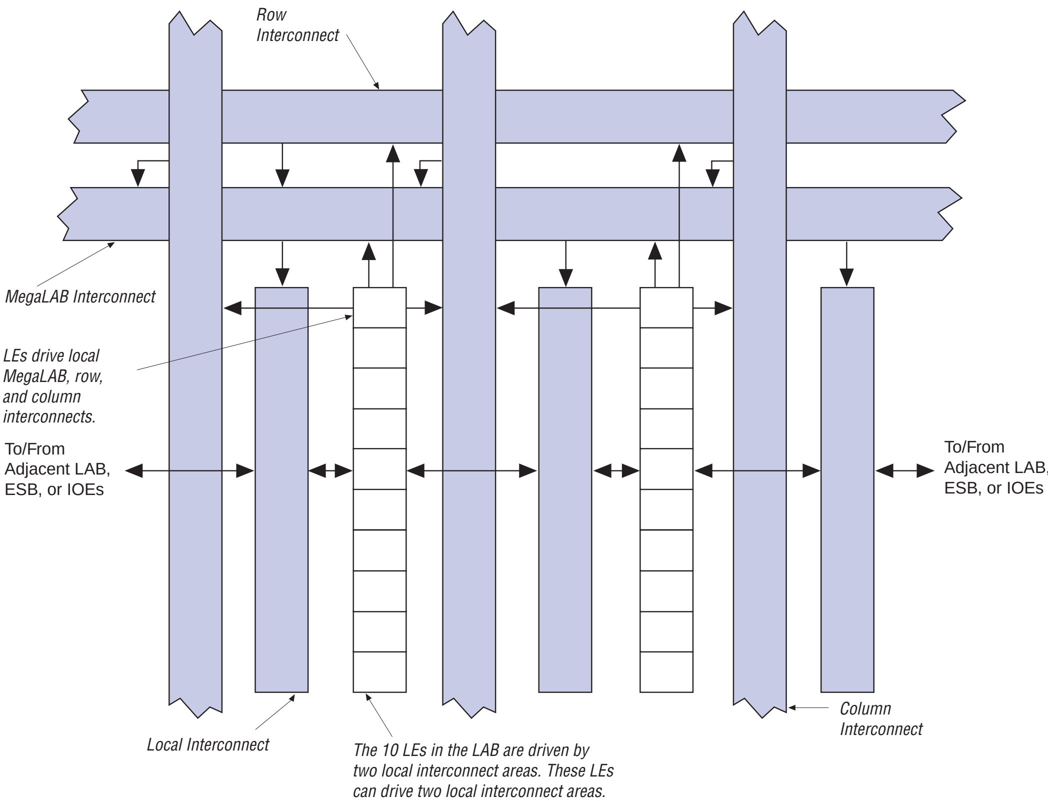


***Figure 10. FastTrack Connection to Local Interconnect***

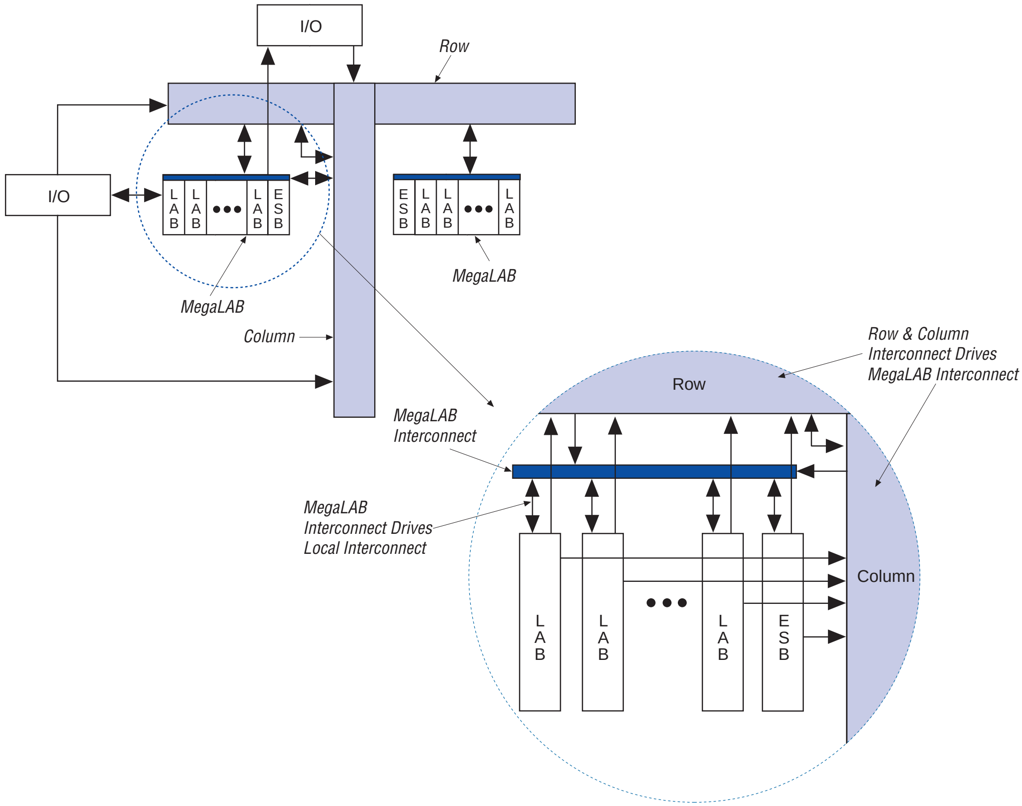
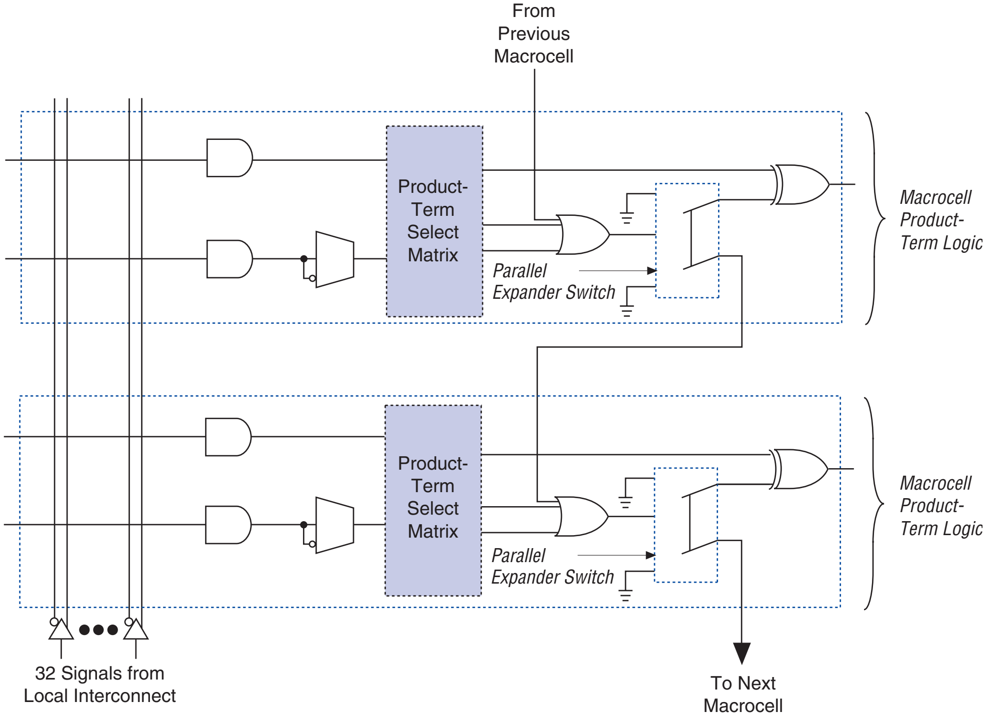


*Figure 16. APEX 20K Parallel Expanders*




## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*

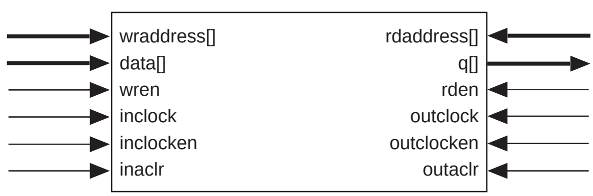
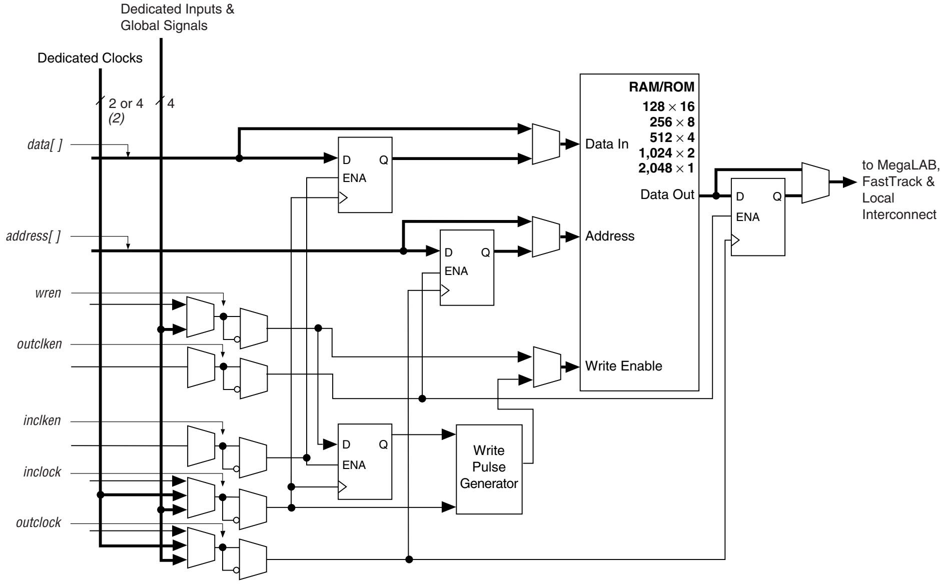


***Figure 22. ESB in Single-Port Mode*** *Note (1)*




*Notes to Figure 22:*

(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

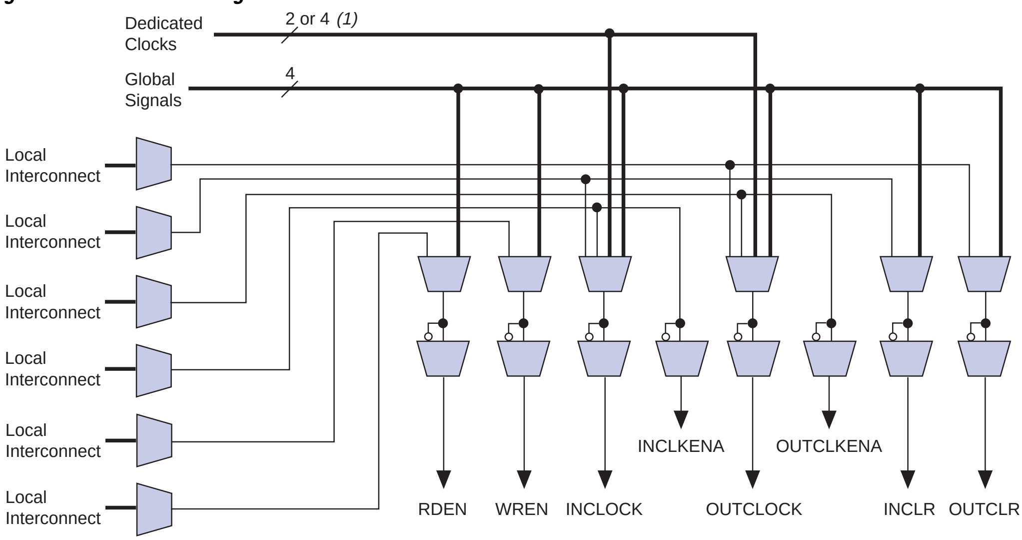
CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

*Figure 24. ESB Control Signal Generation*

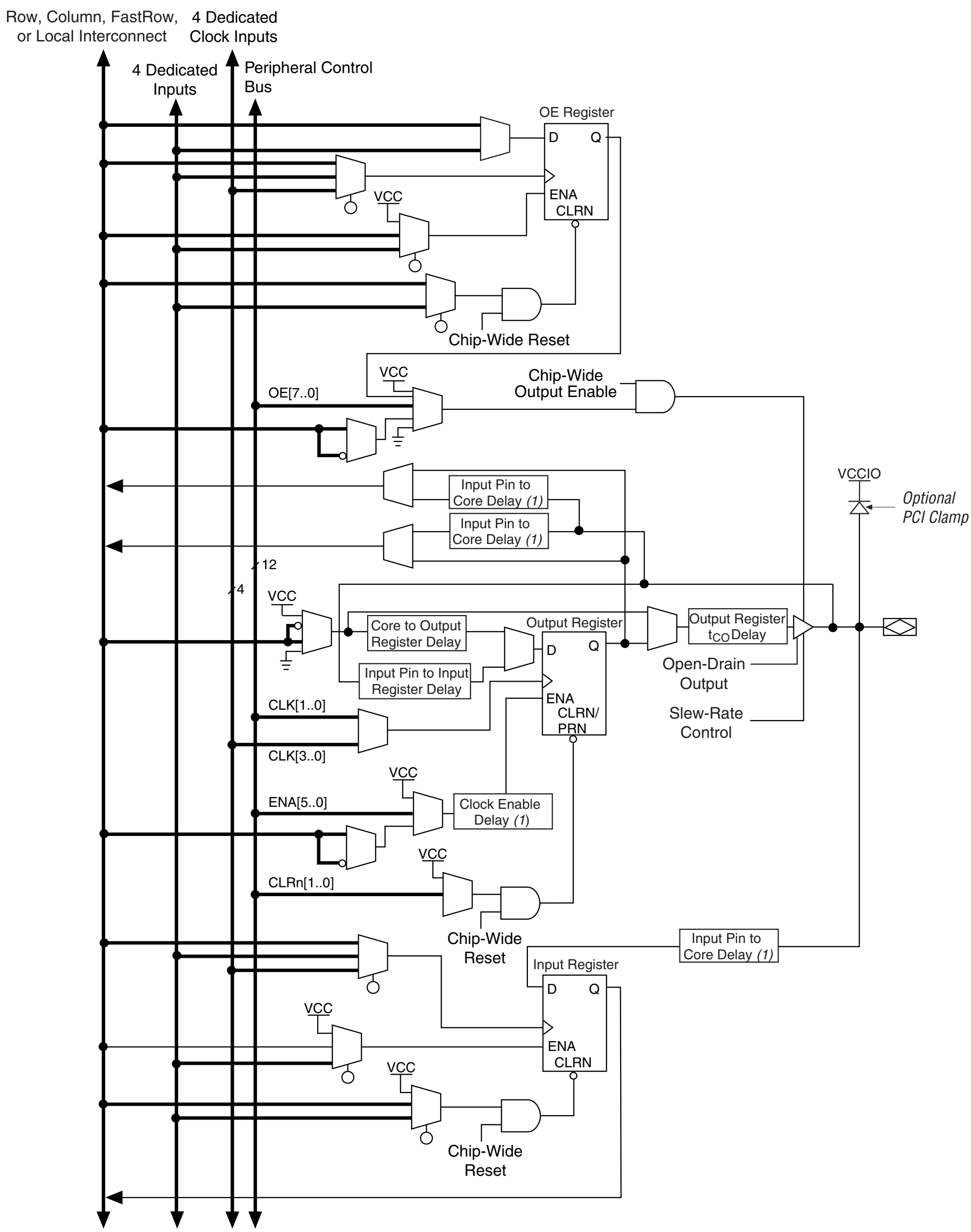



*Note to Figure 24:*

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

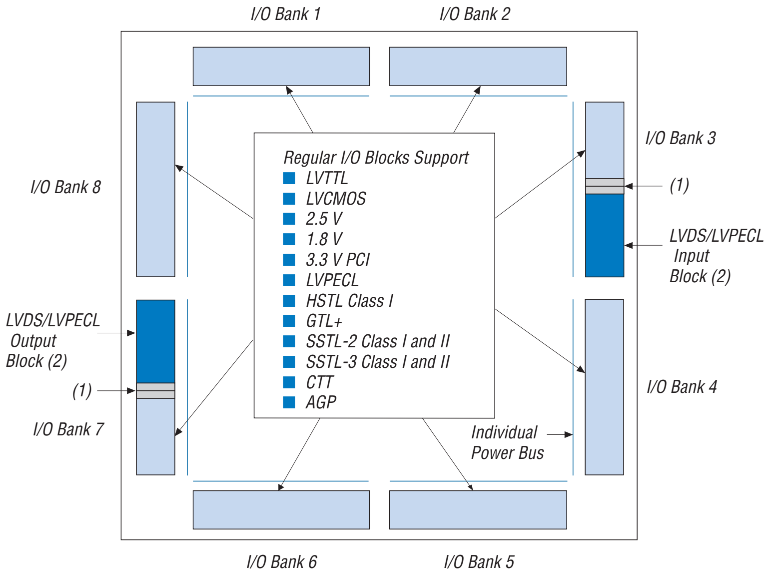
***Figure 26. APEX 20KE Bidirectional I/O Registers*** *Notes (1), (2)*




*Notes to Figure 26:*

(1) This programmable delay has four settings: off and three levels of delay.
(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

***Figure 29. APEX 20KE I/O Banks***




*Notes to Figure 29:*

(1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with $V_{CCIO}$ set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the $V_{CCIO}$ and $V_{CCINT}$ power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

***Table 13. APEX 20KE MultiVolt I/O Support*** *Note (1)*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | *(2)* | | | ✓*(3)* | |

*Notes to Table 13:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

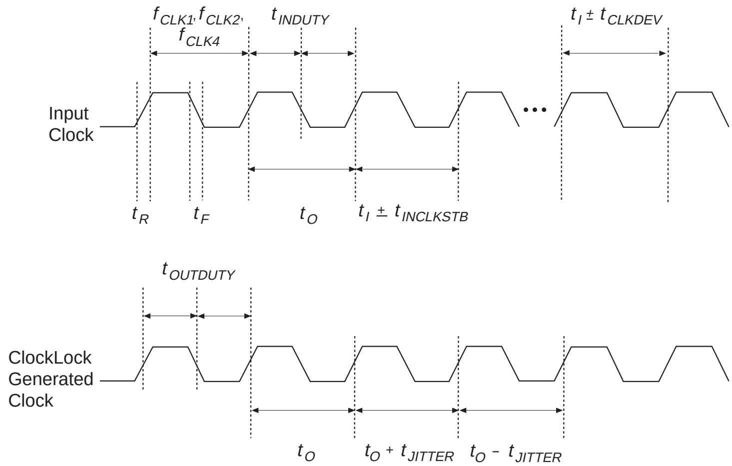
(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

*Figure 30. Specifications for the Incoming & Generated Clocks* *Note (1)*




*Note to Figure 30:*

(1) The tI parameter refers to the nominal input clock period; the tO parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

*Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | 25 | 180 | MHz |
| $f_{CLK1}$ *(1)* | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 180 *(1)* | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 90 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 48 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) *(2)* | | 25,000 *(3)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ClockBoost to acquire lock *(4)* | | 10 | µs |

| Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2) | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $t_{SKEW}$ | Skew delay between related ClockLock/ClockBoost-generated clocks | | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ClockBoost-generated clock *(5)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

*Notes to Table 15:*

(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, $t_{JITTER}$ is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

| Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $f_{OUT}$ | Output frequency | 25 | 170 | MHz |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 170 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 80 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 34 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)* | | 25,000 *(2)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ ClockBoost to acquire lock *(3)* | | 10 | µs |
| $t_{SKEW}$ | Skew delay between related ClockLock/ ClockBoost-generated clock | 500 | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ ClockBoost-generated clock *(4)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

**Table 26. APEX 20K 5.0-V Tolerant Device Capacitance** *Notes (2), (14)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

*Notes to Tables 23 through 26:*

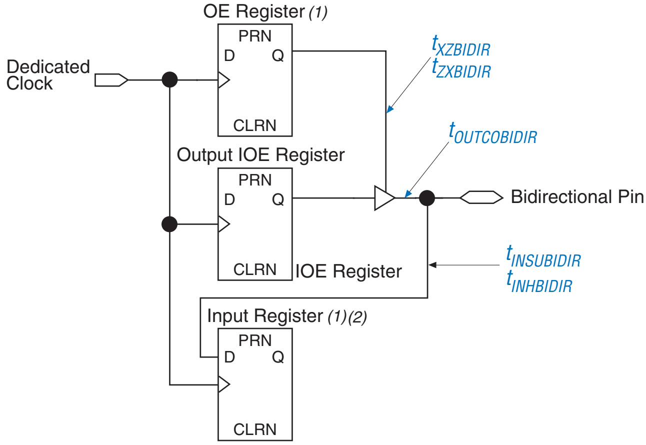
(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$= 25° C, $V_{CCINT}$ = 2.5 V, and $V_{CCIO}$ = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when $V_{CCIO}$ and $V_{CCINT}$ meet the relationship shown in Figure 33 on page 68.
(10) The $I_{OH}$ parameter refers to high-level TTL, PCI or CMOS output current.
(11) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

**Table 27. APEX 20KE Device Absolute Maximum Ratings** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 2.5 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

### *Figure 40. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 40:*

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the $f_{MAX}$ timing parameters shown in Figure 36 on page 68.

**Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 1 of 2)**

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{ESBRC}$ | ESB Asynchronous read cycle time |
| $t_{ESBWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |

Tables 40 through 42 show the $f_{MAX}$ timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 40. EP20K100 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.6 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

*Table 43. EP20K100 External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ *(1)* | 2.3 | | 2.8 | | 3.2 | | ns |
| $t_{INH}$ *(1)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(1)* | 2.0 | 4.5 | 2.0 | 4.9 | 2.0 | 6.6 | ns |
| $t_{INSU}$ *(2)* | 1.1 | | 1.2 | | – | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ *(2)* | 0.5 | 2.7 | 0.5 | 3.1 | – | 4.8 | ns |

*Table 44. EP20K100 External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(1)* | 2.3 | | 2.8 | | 3.2 | | ns |
| $t_{INHBIDIR}$ *(1)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ *(1)* | 2.0 | 4.5 | 2.0 | 4.9 | 2.0 | 6.6 | ns |
| $t_{XZBIDIR}$ *(1)* | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{ZXBIDIR}$ *(1)* | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{INSUBIDIR}$ *(2)* | 1.0 | | 1.2 | | – | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 0.5 | 2.7 | 0.5 | 3.1 | – | – | ns |
| $t_{XZBIDIR}$ *(2)* | | 4.3 | | 5.0 | | – | ns |
| $t_{ZXBIDIR}$ *(2)* | | 4.3 | | 5.0 | | – | ns |

*Table 45. EP20K200 External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ *(1)* | 1.9 | | 2.3 | | 2.6 | | ns |
| $t_{INH}$ *(1)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(1)* | 2.0 | 4.6 | 2.0 | 5.6 | 2.0 | 6.8 | ns |
| $t_{INSU}$ *(2)* | 1.1 | | 1.2 | | – | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ *(2)* | 0.5 | 2.7 | 0.5 | 3.1 | – | – | ns |

Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

Table 51. EP20K30E $f_{MAX}$ Routing Delays

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

| *Table 56. EP20K60E $f_{MAX}$ ESB Timing Microparameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1** | | **-2** | | **-3** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{ESBARC}$ | | 1.83 | | 2.57 | | 3.79 | ns |
| $t_{ESBSRC}$ | | 2.46 | | 3.26 | | 4.61 | ns |
| $t_{ESBAWC}$ | | 3.50 | | 4.90 | | 7.23 | ns |
| $t_{ESBSWC}$ | | 3.77 | | 4.90 | | 6.79 | ns |
| $t_{ESBWASU}$ | 1.59 | | 2.23 | | 3.29 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.75 | | 2.46 | | 3.62 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.76 | | 2.47 | | 3.64 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.68 | | 2.49 | | 3.87 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.08 | | 0.43 | | 1.04 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.29 | | 0.72 | | 1.46 | | ns |
| $t_{ESBRADDRSU}$ | 0.36 | | 0.81 | | 1.58 | | ns |
| $t_{ESBDATACO1}$ | | 1.06 | | 1.24 | | 1.55 | ns |
| $t_{ESBDATACO2}$ | | 2.39 | | 3.35 | | 4.94 | ns |
| $t_{ESBDD}$ | | 3.50 | | 4.90 | | 7.23 | ns |
| $t_{PD}$ | | 1.72 | | 2.41 | | 3.56 | ns |
| $t_{PTERMSU}$ | 0.99 | | 1.56 | | 2.55 | | ns |
| $t_{PTERMCO}$ | | 1.07 | | 1.26 | | 1.08 | ns |

Tables 67 through 72 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

***Table 67. EP20K160E $f_{MAX}$ LE Timing Microparameters***

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.25 | | 0.31 | | 0.35 | ns |
| $t_{LUT}$ | | 0.69 | | 0.88 | | 1.12 | ns |

*Table 80. EP20K300E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.79 | | 2.44 | | 3.25 | ns |
| $t_{ESBSRC}$ | | 2.40 | | 3.12 | | 4.01 | ns |
| $t_{ESBAWC}$ | | 3.41 | | 4.65 | | 6.20 | ns |
| $t_{ESBSWC}$ | | 3.68 | | 4.68 | | 5.93 | ns |
| $t_{ESBWASU}$ | 1.55 | | 2.12 | | 2.83 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.71 | | 2.33 | | 3.11 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.72 | | 2.34 | | 3.13 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.63 | | 2.36 | | 3.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.39 | | 0.80 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.27 | | 0.67 | | 1.17 | | ns |
| $t_{ESBRADDRSU}$ | 0.34 | | 0.75 | | 1.28 | | ns |
| $t_{ESBDATACO1}$ | | 1.03 | | 1.20 | | 1.40 | ns |
| $t_{ESBDATACO2}$ | | 2.33 | | 3.18 | | 4.24 | ns |
| $t_{ESBDD}$ | | 3.41 | | 4.65 | | 6.20 | ns |
| $t_{PD}$ | | 1.68 | | 2.29 | | 3.06 | ns |
| $t_{PTERMSU}$ | 0.96 | | 1.48 | | 2.14 | | ns |
| $t_{PTERMCO}$ | | 1.05 | | 1.22 | | 1.42 | ns |

*Table 81. EP20K300E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.24 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.33 | | 1.43 | | 1.58 | ns |
| $t_{F20+}$ | | 3.63 | | 3.93 | | 4.35 | ns |