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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

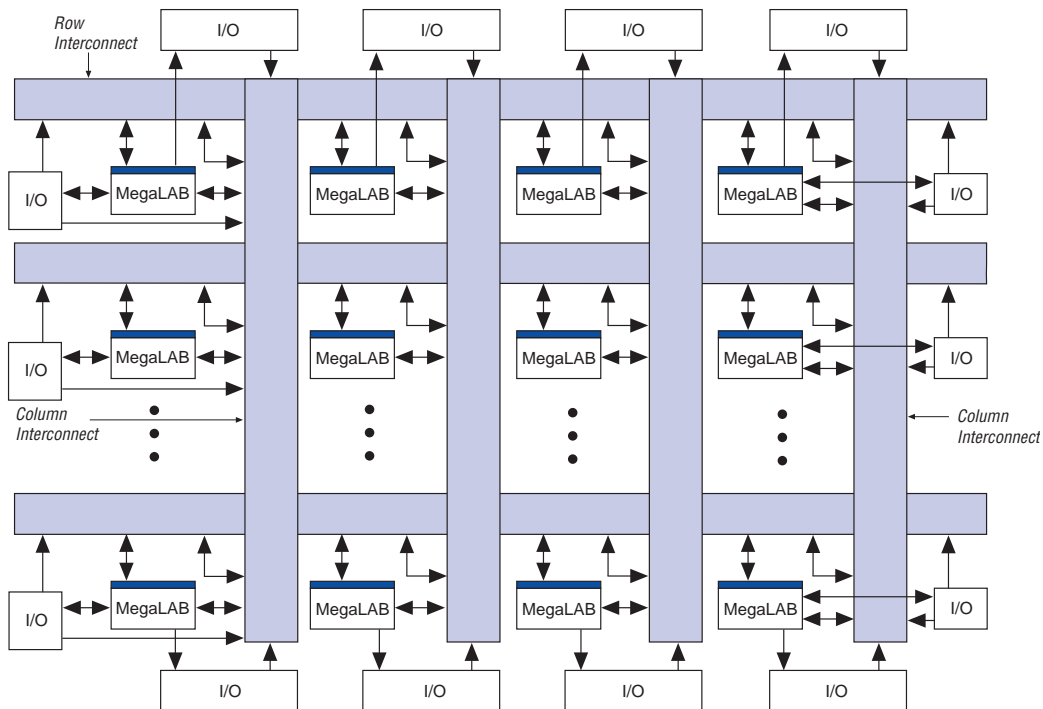
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	640
Number of Logic Elements/Cells	6400
Total RAM Bits	81920
Number of I/O	143
Number of Gates	404000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k160eqi208-3

Table 8. Comparison of APEX 20K & APEX 20KE Features

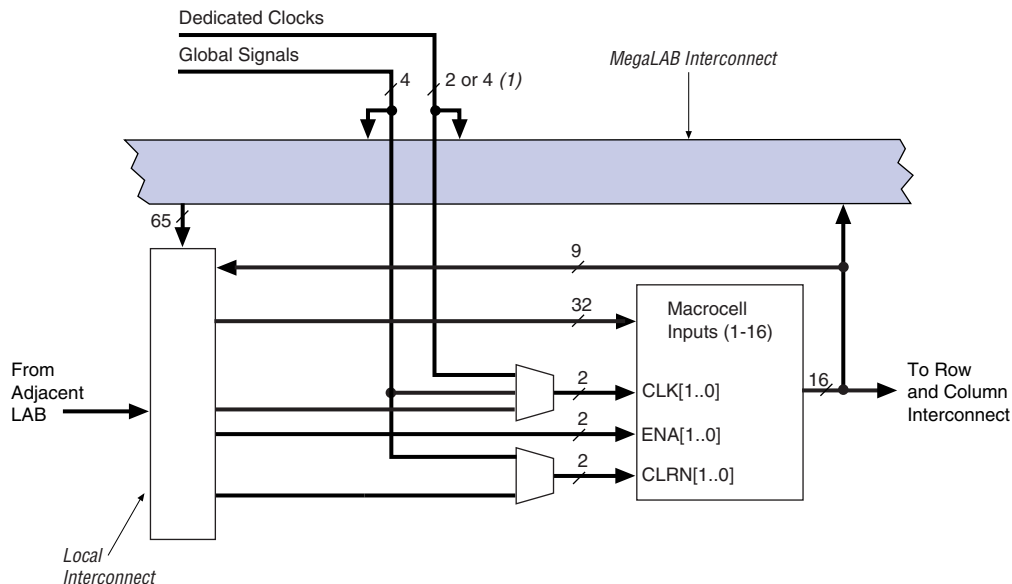
Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
SignalTap logic analysis	Full support	Full support
32/64-Bit, 33-MHz PCI	Full compliance in -1, -2 speed grades	Full compliance in -1, -2 speed grades
32/64-Bit, 66-MHz PCI	-	Full compliance in -1 speed grade
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device Certain devices are 5.0-V tolerant	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction 2× and 4× clock multiplication	Clock delay reduction $m/(n \times v)$ or $m/(n \times k)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVTTL True-LVDS and LVPECL data pins (in EP20K300E and larger devices) LVDS and LVPECL signaling (in all BGA and FineLine BGA devices) LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

Figure 9. APEX 20K Interconnect Structure

A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 13. Product-Term Logic in ESB

Note to Figure 13:

(1) APEX 20KE devices have four dedicated clocks.

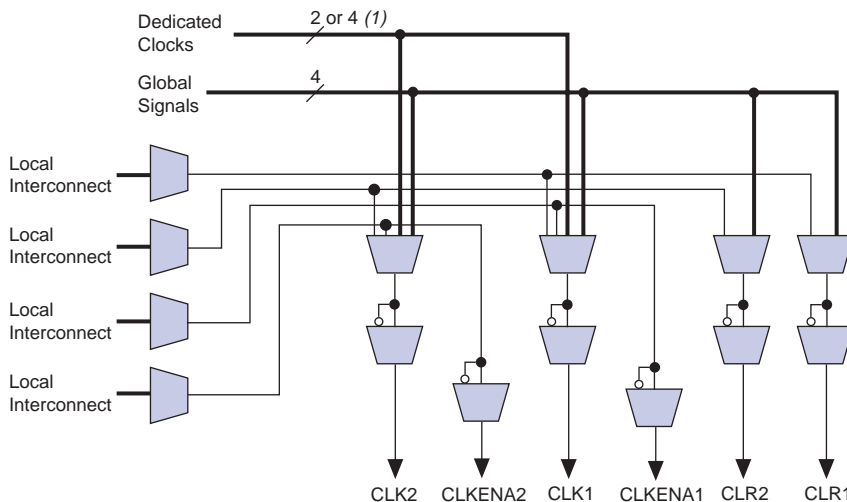
Macrocells

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Note to Figure 15:

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128×16 , 256×8 , 512×4 , $1,024 \times 2$, or $2,048 \times 1$. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128×16 RAM blocks can be combined to form a 128×32 RAM block, and two 512×4 RAM blocks can be combined to form a 512×8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).

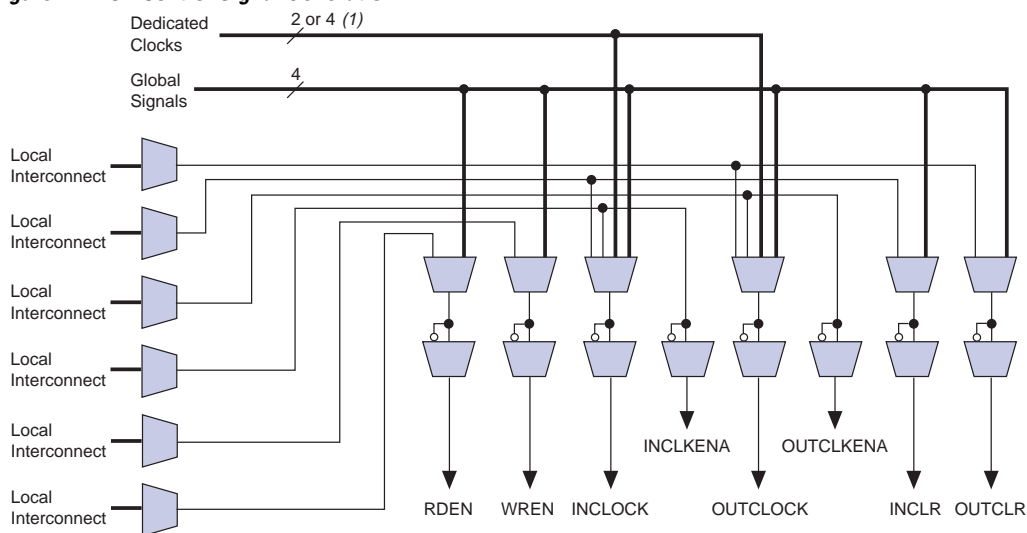


For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. [Figure 24](#) shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation



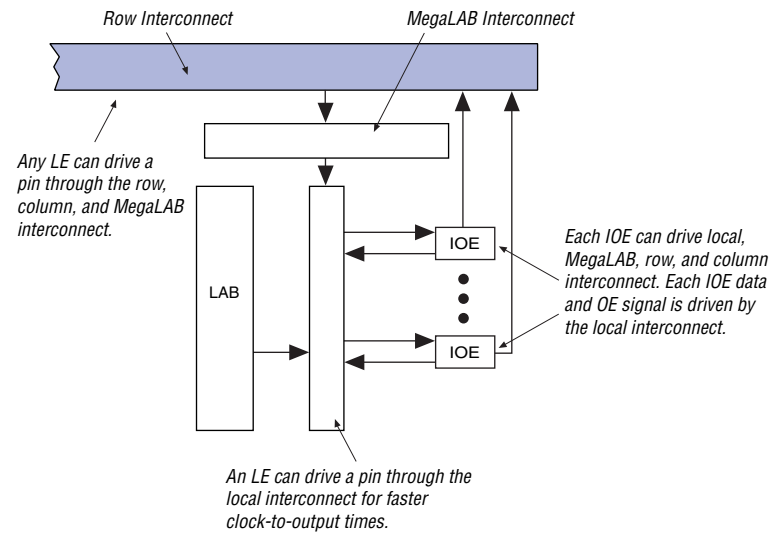
Note to Figure 24:

(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. **Figure 27** shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect



Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.



For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. [Figure 29](#) shows the arrangement of the APEX 20KE I/O banks.

MultiVolt I/O Interface

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V VCCINT level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support						
V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓(1)	✓(1)	✓		
3.3	✓	✓	✓(1)	✓(2)	✓	✓

Notes to Table 12:

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
- (2) When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual LOCK signals. The LOCK signal drives high when the ClockLock circuit has locked onto the input clock. The LOCK signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

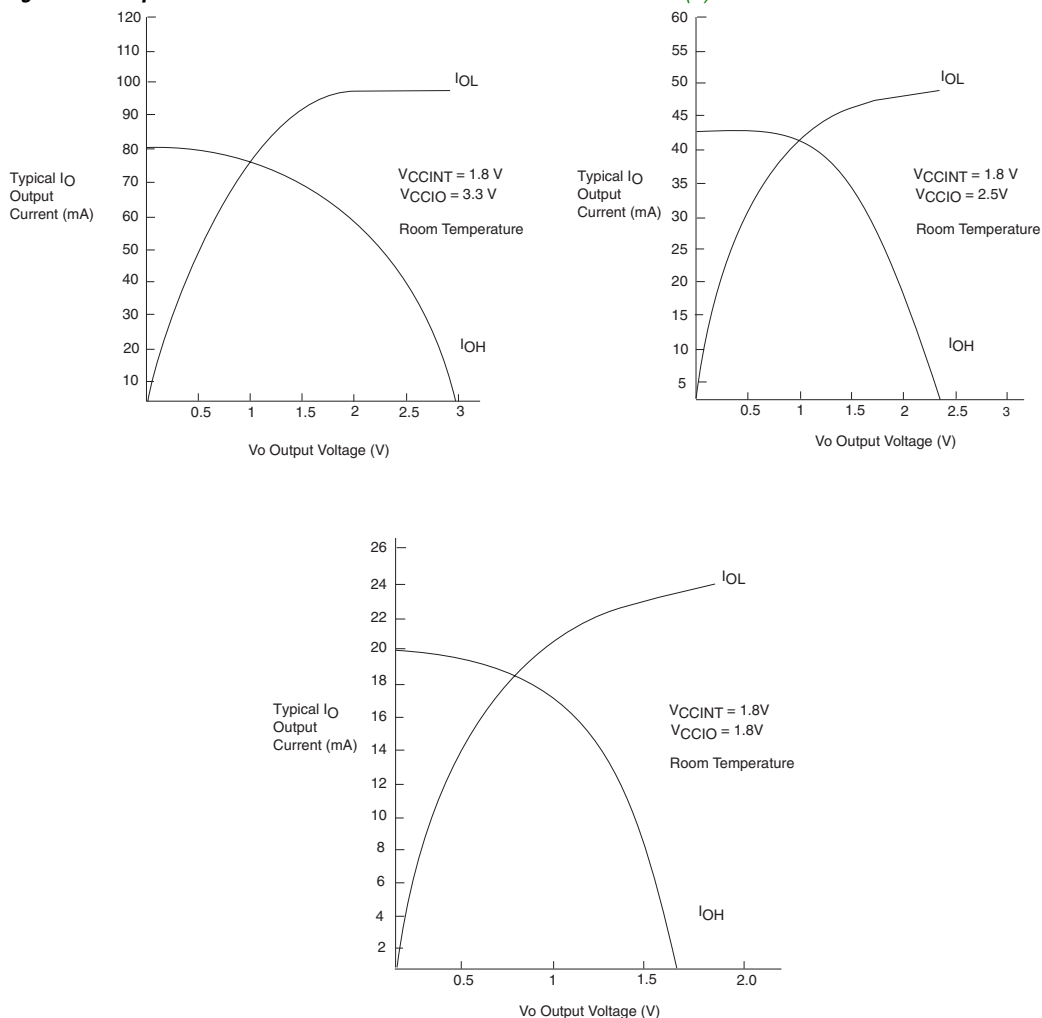
For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. [Figure 30](#) shows the incoming and generated clock specifications.



For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices *Note (1)*

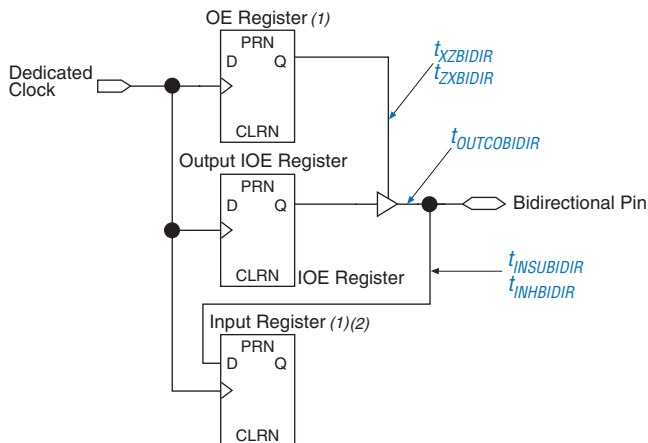


Note to Figure 35:

(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figure 40. Synchronous Bidirectional Pin External Timing**Notes to Figure 40:**

- (1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.
- (2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the f_{MAX} timing parameters shown in Figure 36 on page 68.

Table 31. APEX 20K t_{MAX} Timing Parameters (Part 1 of 2)

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in
t_{ESBRC}	ESB Asynchronous read cycle time
t_{ESBWC}	ESB Asynchronous write cycle time
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBADDRSU}$	ESB address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers

Tables 40 through 42 show the f_{MAX} timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

Table 40. EP20K100 f_{MAX} Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.5		0.6		0.8		ns
t_{H}	0.7		0.8		1.0		ns
t_{CO}		0.3		0.4		0.5	ns
t_{LUT}		0.8		1.0		1.3	ns
t_{ESBRC}		1.7		2.1		2.4	ns
t_{ESBWC}		5.7		6.9		8.1	ns
t_{ESBWESU}	3.3		3.9		4.6		ns
$t_{\text{ESBDATASU}}$	2.2		2.7		3.1		ns
t_{ESBDATAH}	0.6		0.8		0.9		ns
$t_{\text{ESBADDRSU}}$	2.4		2.9		3.3		ns
$t_{\text{ESBDATACO1}}$		1.3		1.6		1.8	ns
$t_{\text{ESBDATACO2}}$		2.6		3.1		3.6	ns
t_{ESBDD}		2.5		3.3		3.6	ns
t_{PD}		2.5		3.0		3.6	ns
t_{PTERMSU}	2.3		2.6		3.2		ns
t_{PTERMCO}		1.5		1.8		2.1	ns
$t_{\text{F1-4}}$		0.5		0.6		0.7	ns
$t_{\text{F5-20}}$		1.6		1.7		1.8	ns
$t_{\text{F20+}}$		2.2		2.2		2.3	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns
t_{CLRP}	0.3		0.4		0.4		ns
t_{PREP}	0.5		0.5		0.5		ns
t_{ESBCH}	2.0		2.5		3.0		ns
t_{ESBCL}	2.0		2.5		3.0		ns
t_{ESBWP}	1.6		1.9		2.2		ns
t_{ESBRP}	1.0		1.3		1.4		ns

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU} (1)	2.3		2.8		3.2		ns
t _{INH} (1)	0.0		0.0		0.0		ns
t _{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t _{INSU} (2)	1.1		1.2		—		ns
t _{INH} (2)	0.0		0.0		—		ns
t _{OUTCO} (2)	0.5	2.7	0.5	3.1	—	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR} (1)	2.3		2.8		3.2		ns
t _{INHBIDIR} (1)	0.0		0.0		0.0		ns
t _{OUTCOBIDIR} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t _{XZBIDIR} (1)		5.0		5.9		6.9	ns
t _{ZXBIDIR} (1)		5.0		5.9		6.9	ns
t _{INSUBIDIR} (2)	1.0		1.2		—		ns
t _{INHBIDIR} (2)	0.0		0.0		—		ns
t _{OUTCOBIDIR} (2)	0.5	2.7	0.5	3.1	—	—	ns
t _{XZBIDIR} (2)		4.3		5.0		—	ns
t _{ZXBIDIR} (2)		4.3		5.0		—	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU} (1)	1.9		2.3		2.6		ns
t _{INH} (1)	0.0		0.0		0.0		ns
t _{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t _{INSU} (2)	1.1		1.2		—		ns
t _{INH} (2)	0.0		0.0		—		ns
t _{OUTCO} (2)	0.5	2.7	0.5	3.1	—	—	ns

Table 56. EP20K60E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.83		2.57		3.79	ns
t_{ESBSRC}		2.46		3.26		4.61	ns
t_{ESBAWC}		3.50		4.90		7.23	ns
t_{ESBSWC}		3.77		4.90		6.79	ns
$t_{ESBWASU}$	1.59		2.23		3.29		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.75		2.46		3.62		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.76		2.47		3.64		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.68		2.49		3.87		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.08		0.43		1.04		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.29		0.72		1.46		ns
$t_{ESBRADDRSU}$	0.36		0.81		1.58		ns
$t_{ESBDATACO1}$		1.06		1.24		1.55	ns
$t_{ESBDATACO2}$		2.39		3.35		4.94	ns
t_{ESBDD}		3.50		4.90		7.23	ns
t_{PD}		1.72		2.41		3.56	ns
$t_{PTERMSU}$	0.99		1.56		2.55		ns
$t_{PTERMCO}$		1.07		1.26		1.08	ns

Table 74. EP20K200E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.68		2.06		2.24	ns
t_{ESBSRC}		2.27		2.77		3.18	ns
t_{ESBAWC}		3.10		3.86		4.50	ns
t_{ESBSWC}		2.90		3.67		4.21	ns
$t_{ESBWASU}$	0.55		0.67		0.74		ns
t_{ESBWAH}	0.36		0.46		0.48		ns
$t_{ESBWDSU}$	0.69		0.83		0.95		ns
t_{ESBWDH}	0.36		0.46		0.48		ns
$t_{ESBRASU}$	1.61		1.90		2.09		ns
t_{ESBRAH}	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.42		1.71		2.01		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.06		-0.07		0.05		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.13		0.31		ns
$t_{ESBRADDRSU}$	0.18		0.23		0.39		ns
$t_{ESBDATAO1}$		1.09		1.35		1.51	ns
$t_{ESBDATAO2}$		2.19		2.75		3.22	ns
t_{ESBDD}		2.75		3.41		4.03	ns
t_{PD}		1.58		1.97		2.33	ns
$t_{PTERMSU}$	1.00		1.22		1.51		ns
$t_{PTERMCO}$		1.10		1.37		1.09	ns

Table 75. EP20K200E t_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.27		0.29	ns
t_{F5-20}		1.02		1.20		1.41	ns
t_{F20+}		1.99		2.23		2.53	ns

Table 80. EP20K300E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.79		2.44		3.25	ns
t_{ESBSRC}		2.40		3.12		4.01	ns
t_{ESBAWC}		3.41		4.65		6.20	ns
t_{ESBSWC}		3.68		4.68		5.93	ns
$t_{ESBWASU}$	1.55		2.12		2.83		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.71		2.33		3.11		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.72		2.34		3.13		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.63		2.36		3.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.39		0.80		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.27		0.67		1.17		ns
$t_{ESBRADDRSU}$	0.34		0.75		1.28		ns
$t_{ESBDATACO1}$		1.03		1.20		1.40	ns
$t_{ESBDATACO2}$		2.33		3.18		4.24	ns
t_{ESBDD}		3.41		4.65		6.20	ns
t_{PD}		1.68		2.29		3.06	ns
$t_{PTERMSU}$	0.96		1.48		2.14		ns
$t_{PTERMCO}$		1.05		1.22		1.42	ns

Table 81. EP20K300E t_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.24		0.26	ns
t_{F5-20}		1.33		1.43		1.58	ns
t_{F20+}		3.63		3.93		4.35	ns

Table 82. EP20K300E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.25		1.43		1.67		ns
t _{CL}	1.25		1.43		1.67		ns
t _{CLRP}	0.19		0.26		0.35		ns
t _{PREP}	0.19		0.26		0.35		ns
t _{ESBCH}	1.25		1.43		1.67		ns
t _{ESBCL}	1.25		1.43		1.67		ns
t _{ESBWP}	1.25		1.71		2.28		ns
t _{ESBRP}	1.01		1.38		1.84		ns

Table 83. EP20K300E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.31		2.44		2.57		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.29	2.00	5.82	2.00	6.24	ns
t _{INSUPLL}	1.76		1.85		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.65	0.50	2.95	-	-	ns

Table 84. EP20K300E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	2.77		2.85		3.11		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	5.29	2.00	5.82	2.00	6.24	ns
t _{XZBIDIR}		7.59		8.30		9.09	ns
t _{ZXBIDIR}		7.59		8.30		9.09	ns
t _{INSUBIDIRPLL}	2.50		2.76		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.65	0.50	2.95	-	-	ns
t _{XZBIDIRPLL}		5.00		5.43		-	ns
t _{ZXBIDIRPLL}		5.00		5.43		-	ns

Table 92. EP20K600E t_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		2.39		3.11	ns
t_{ESBSRC}		2.27		3.07		3.86	ns
t_{ESBAWC}		3.19		4.56		5.93	ns
t_{ESBSWC}		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATAO1}$		1.01		1.19		1.37	ns
$t_{ESBDATAO2}$		2.18		3.12		4.05	ns
t_{ESBDD}		3.19		4.56		5.93	ns
t_{PD}		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

Table 93. EP20K600E t_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.25		0.26	ns
t_{F5-20}		1.26		1.39		1.52	ns
t_{F20+}		3.51		3.88		4.26	ns

Table 98. EP20K1000E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns