# Intel - EP20K160ETC144-1 Datasheet

**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 640 |
| Number of Logic Elements/Cells | 6400 |
| Total RAM Bits | 81920 |
| Number of I/O | 88 |
| Number of Gates | 404000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k160etc144-1 |

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock® feature reducing clock delay and skew
  - ClockBoost® feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ($t_{CO}$ + $t_{SU}$) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast $t_{CO}$ and $t_{SU}$ times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - Programmable clamp to $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
  - FineLine BGA® packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus® II development system for

*Table 5. APEX 20K FineLine BGA Package Options & I/O Count* *Notes (1), (2)*

| Device | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| EP20K30E | 93 | 128 | | | |
| EP20K60E | 93 | 196 | | | |
| EP20K100 | | 252 | | | |
| EP20K100E | 93 | 246 | | | |
| EP20K160E | | | 316 | | |
| EP20K200 | | | 382 | | |
| EP20K200E | | | 376 | 376 | |
| EP20K300E | | | | 408 | |
| EP20K400 | | | | 502 *(3)* | |
| EP20K400E | | | | 488 *(3)* | |
| EP20K600E | | | | 508 *(3)* | 588 |
| EP20K1000E | | | | 508 *(3)* | 708 |
| EP20K1500E | | | | | 808 |

***Notes to Tables 4 and 5:***

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

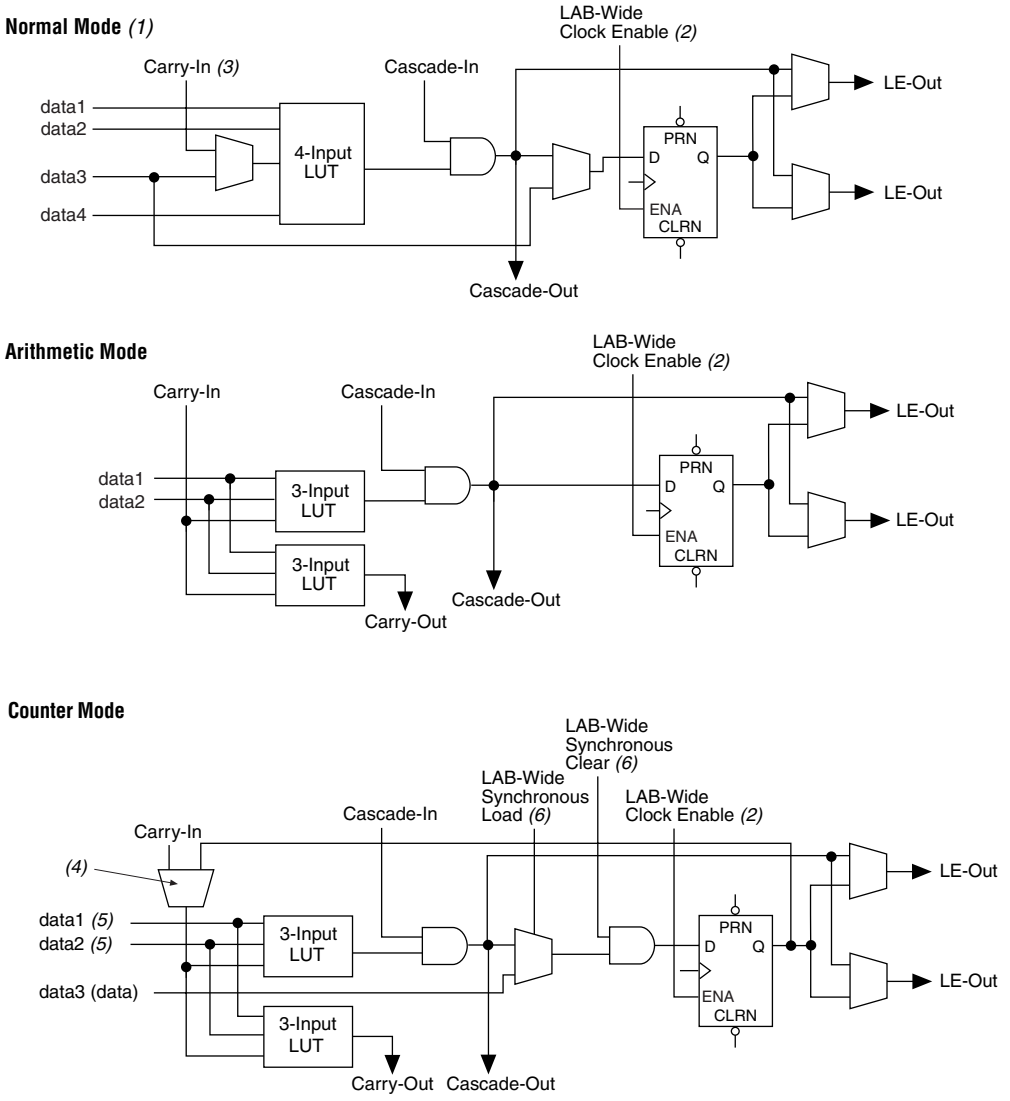
*Table 6. APEX 20K QFP, BGA & PGA Package Sizes*

| Feature | 144-Pin TQFP | 208-Pin QFP | 240-Pin QFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.27 | 1.27 | – |
| Area ($mm^2$) | 484 | 924 | 1,218 | 1,225 | 2,025 | 3,906 |
| Length × Width (mm × mm) | 22 × 22 | 30.4 × 30.4 | 34.9 × 34.9 | 35 × 35 | 45 × 45 | 62.5 × 62.5 |

*Table 7. APEX 20K FineLine BGA Package Sizes*

| Feature | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 169 | 361 | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 13 × 13 | 19 × 19 | 23 × 23 | 27 × 27 | 33 × 33 |

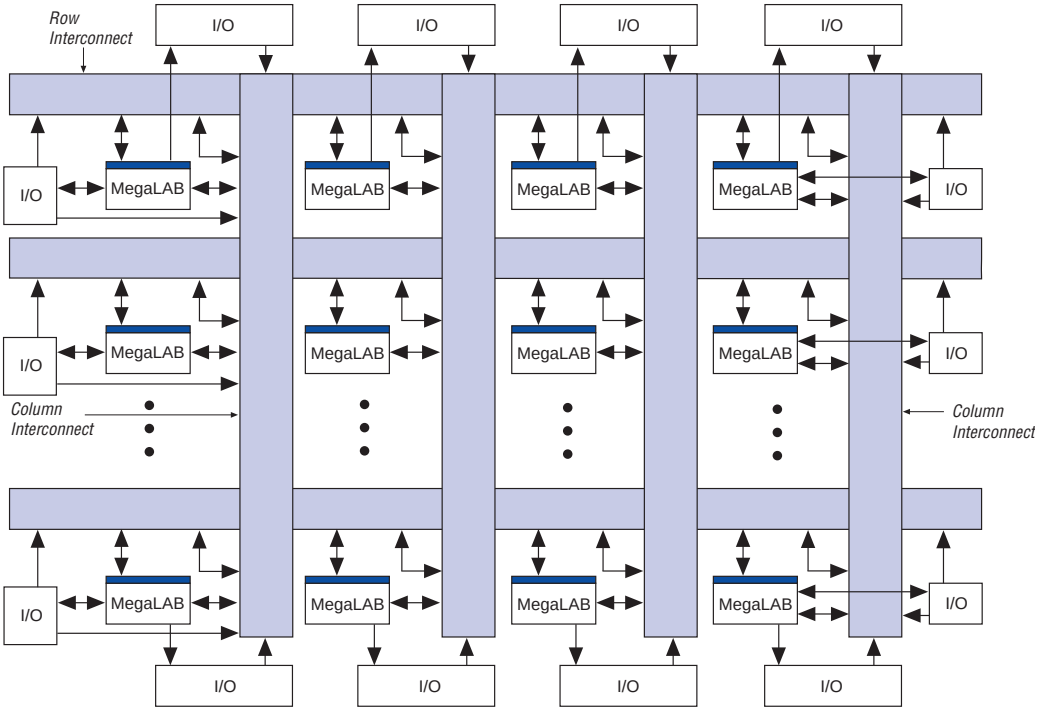
*Figure 8. APEX 20K LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

*Figure 9. APEX 20K Interconnect Structure*




A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

*Figure 10. FastTrack Connection to Local Interconnect*

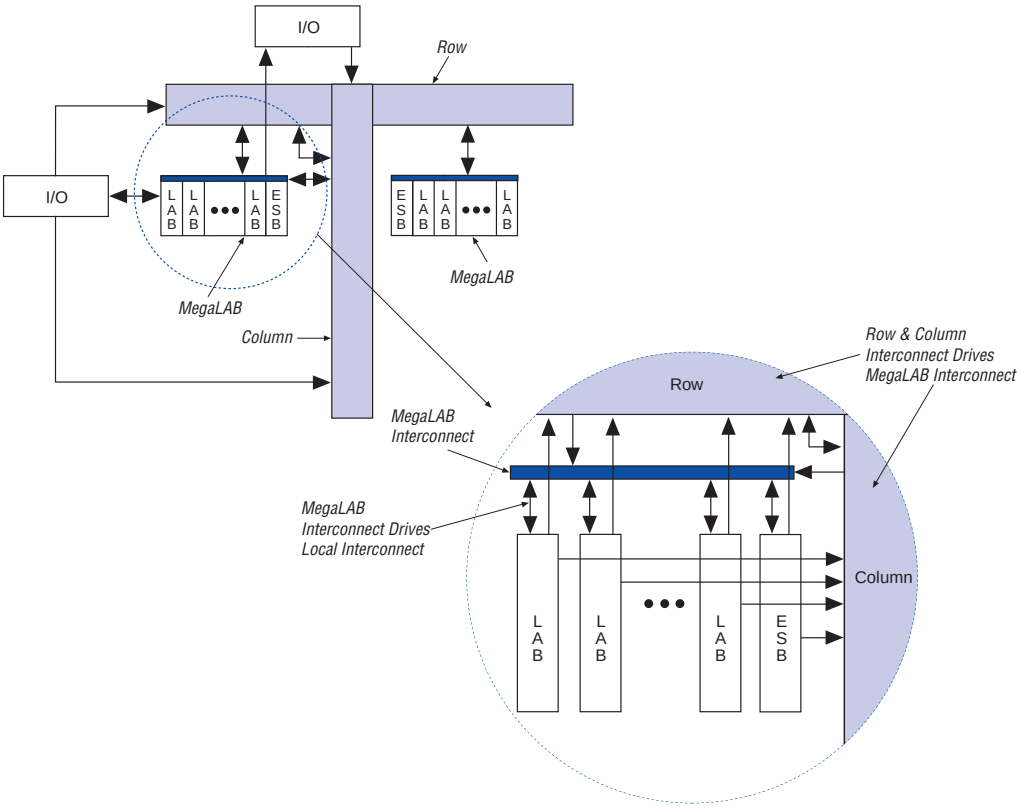
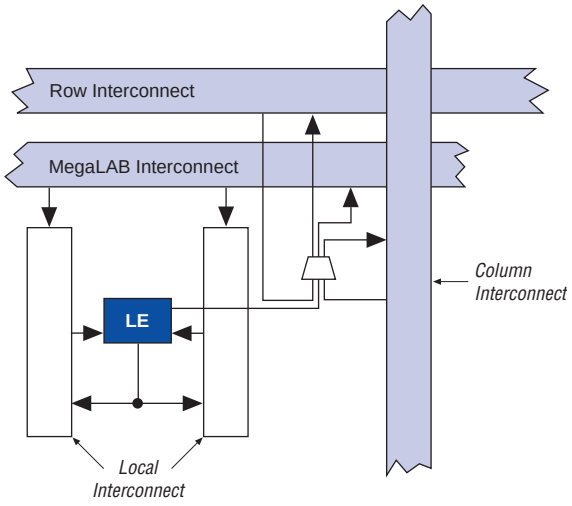


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

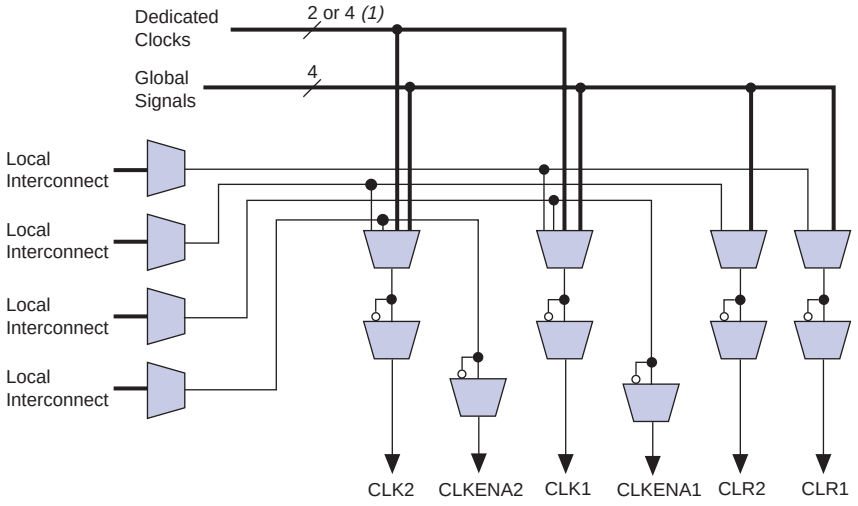
*Figure 11. Driving the FastTrack Interconnect*




APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABS in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*



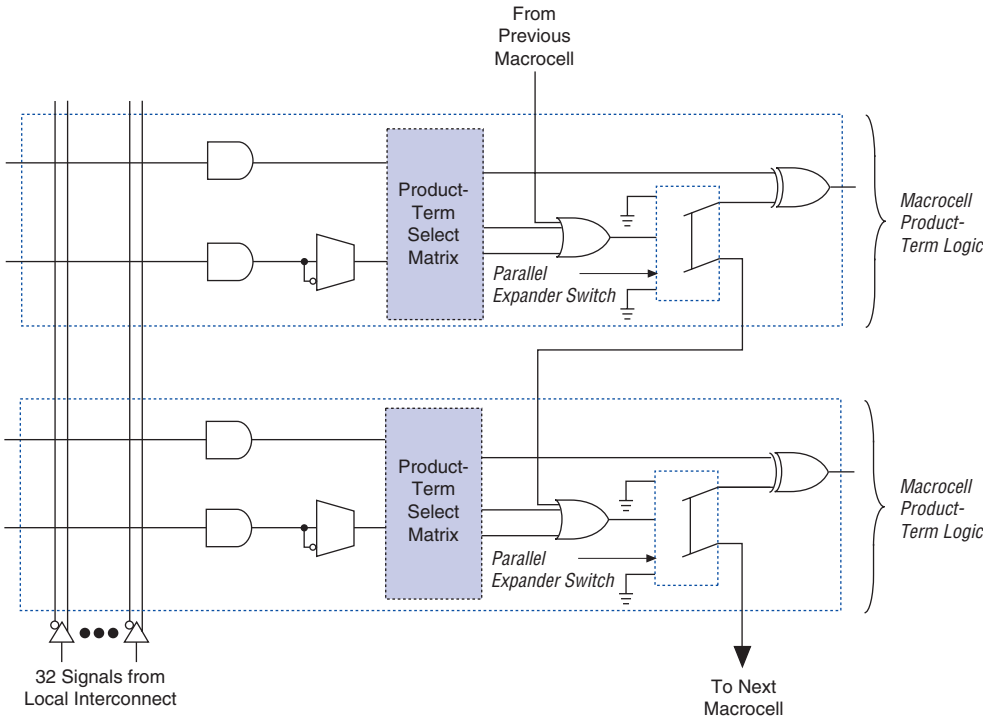

*Note to Figure 15:*
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

*Figure 16. APEX 20K Parallel Expanders*




## Embedded System Block

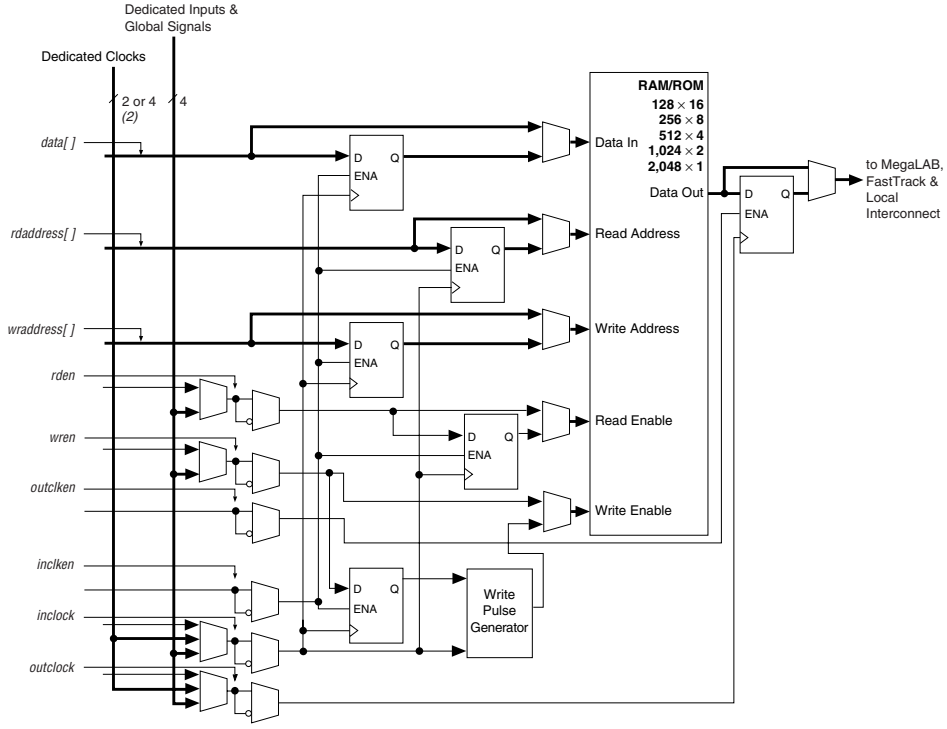
The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

***Figure 21. ESB in Input/Output Clock Mode*** *Note (1)*

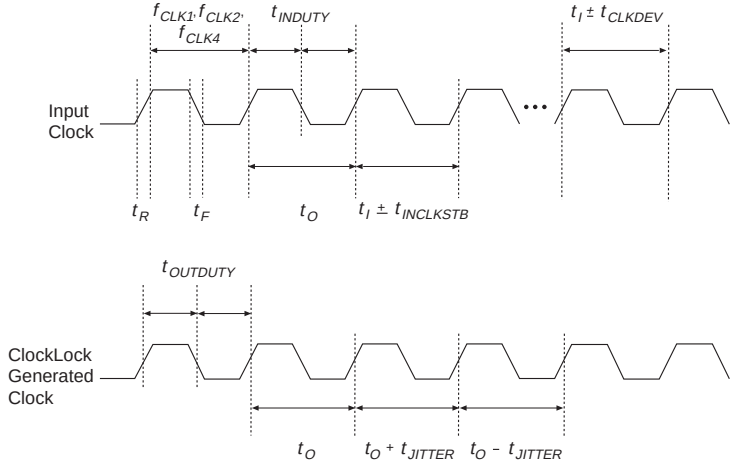



*Notes to Figure 21:*
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

*Figure 30. Specifications for the Incoming & Generated Clocks* *Note (1)*




*Note to Figure 30:*
(1) The tI parameter refers to the nominal input clock period; the tO parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

*Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | 25 | 180 | MHz |
| $f_{CLK1}$ *(1)* | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 180 *(1)* | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 90 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 48 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) *(2)* | | 25,000 *(3)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ClockBoost to acquire lock *(4)* | | 10 | µs |

*Table 42. EP20K400 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.1 | | 0.3 | | 0.6 | | ns |
| $t_{H}$ | 0.5 | | 0.8 | | 0.9 | | ns |
| $t_{CO}$ | | 0.1 | | 0.4 | | 0.6 | ns |
| $t_{LUT}$ | | 1.0 | | 1.2 | | 1.4 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.5 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.1 | | 3.6 | ns |
| $t_{PTERMSU}$ | 1.7 | | 2.1 | | 2.4 | | ns |
| $t_{PTERMCO}$ | | 1.0 | | 1.2 | | 1.4 | ns |
| $t_{F1-4}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{F5-20}$ | | 2.6 | | 2.8 | | 2.9 | ns |
| $t_{F20+}$ | | 3.7 | | 3.8 | | 3.9 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.5 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.2 | | 1.4 | | ns |

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

*Table 51. EP20K30E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

*Table 52. EP20K30E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CLRP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{PREP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{ESBCH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBCL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBWP}$ | 1.43 | | 2.01 | | 2.97 | | ns |
| $t_{ESBRP}$ | 1.15 | | 1.62 | | 2.39 | | ns |

*Table 53. EP20K30E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.02 | | 2.13 | | 2.24 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{INSUPLL}$ | 2.11 | | 2.23 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |

*Table 54. EP20K30E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.85 | | 1.77 | | 1.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{XZBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{ZXBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{INSUBIDIRPLL}$ | 4.12 | | 4.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |

*Table 72. EP20K160E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.86 | | 3.24 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{XZBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{ZXBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{INSUBIDIRPLL}$ | 4.93 | | 5.48 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |

Tables 73 through 78 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

*Table 73. EP20K200E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.26 | | 0.31 | | 0.36 | ns |
| $t_{LUT}$ | | 0.70 | | 0.90 | | 1.14 | ns |

*Table 76. EP20K200E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{CL}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{PREP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{ESBCH}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{ESBCL}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{ESBWP}$ | 1.18 | | 1.48 | | 1.76 | | ns |
| $t_{ESBRP}$ | 0.95 | | 1.17 | | 1.41 | | ns |

*Table 77. EP20K200E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.24 | | 2.35 | | 2.47 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.12 | 2.00 | 5.62 | 2.00 | 6.11 | ns |
| $t_{INSUPLL}$ | 2.13 | | 2.07 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.01 | 0.50 | 3.36 | - | - | ns |

*Table 80. EP20K300E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.79 | | 2.44 | | 3.25 | ns |
| $t_{ESBSRC}$ | | 2.40 | | 3.12 | | 4.01 | ns |
| $t_{ESBAWC}$ | | 3.41 | | 4.65 | | 6.20 | ns |
| $t_{ESBSWC}$ | | 3.68 | | 4.68 | | 5.93 | ns |
| $t_{ESBWASU}$ | 1.55 | | 2.12 | | 2.83 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.71 | | 2.33 | | 3.11 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.72 | | 2.34 | | 3.13 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.63 | | 2.36 | | 3.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.39 | | 0.80 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.27 | | 0.67 | | 1.17 | | ns |
| $t_{ESBRADDRSU}$ | 0.34 | | 0.75 | | 1.28 | | ns |
| $t_{ESBDATACO1}$ | | 1.03 | | 1.20 | | 1.40 | ns |
| $t_{ESBDATACO2}$ | | 2.33 | | 3.18 | | 4.24 | ns |
| $t_{ESBDD}$ | | 3.41 | | 4.65 | | 6.20 | ns |
| $t_{PD}$ | | 1.68 | | 2.29 | | 3.06 | ns |
| $t_{PTERMSU}$ | 0.96 | | 1.48 | | 2.14 | | ns |
| $t_{PTERMCO}$ | | 1.05 | | 1.22 | | 1.42 | ns |

*Table 81. EP20K300E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.24 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.33 | | 1.43 | | 1.58 | ns |
| $t_{F20+}$ | | 3.63 | | 3.93 | | 4.35 | ns |

*Table 82. EP20K300E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.19 | | 0.26 | | 0.35 | | ns |
| $t_{PREP}$ | 0.19 | | 0.26 | | 0.35 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.25 | | 1.71 | | 2.28 | | ns |
| $t_{ESBRP}$ | 1.01 | | 1.38 | | 1.84 | | ns |

*Table 83. EP20K300E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.31 | | 2.44 | | 2.57 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| $t_{INSUPLL}$ | 1.76 | | 1.85 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |

*Table 84. EP20K300E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.85 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| $t_{XZBIDIR}$ | | 7.59 | | 8.30 | | 9.09 | ns |
| $t_{ZXBIDIR}$ | | 7.59 | | 8.30 | | 9.09 | ns |
| $t_{INSUBIDIRPLL}$ | 2.50 | | 2.76 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.43 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.43 | | - | ns |

*Table 92. EP20K600E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 2.39 | | 3.11 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 3.07 | | 3.86 | ns |
| $t_{ESBAWC}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{ESBSWC}$ | | 3.51 | | 4.62 | | 5.72 | ns |
| $t_{ESBWASU}$ | 1.46 | | 2.08 | | 2.70 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.60 | | 2.29 | | 2.97 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 2.30 | | 2.99 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.49 | | 2.30 | | 3.11 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.01 | | 0.35 | | 0.71 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.19 | | 0.62 | | 1.06 | | ns |
| $t_{ESBRADDRSU}$ | 0.25 | | 0.71 | | 1.17 | | ns |
| $t_{ESBDATACO1}$ | | 1.01 | | 1.19 | | 1.37 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 3.12 | | 4.05 | ns |
| $t_{ESBDD}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{PD}$ | | 1.57 | | 2.25 | | 2.92 | ns |
| $t_{PTERMSU}$ | 0.85 | | 1.43 | | 2.01 | | ns |
| $t_{PTERMCO}$ | | 1.03 | | 1.21 | | 1.39 | ns |

*Table 93. EP20K600E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.26 | | 1.39 | | 1.52 | ns |
| $t_{F20+}$ | | 3.51 | | 3.88 | | 4.26 | ns |

*Table 98. EP20K1000E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.78 | | 2.02 | | 1.95 | ns |
| $t_{ESBSRC}$ | | 2.52 | | 2.91 | | 3.14 | ns |
| $t_{ESBAWC}$ | | 3.52 | | 4.11 | | 4.40 | ns |
| $t_{ESBSWC}$ | | 3.23 | | 3.84 | | 4.16 | ns |
| $t_{ESBWASU}$ | 0.62 | | 0.67 | | 0.61 | | ns |
| $t_{ESBWAH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.77 | | 0.79 | | 0.81 | | ns |
| $t_{ESBWDH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.74 | | 1.92 | | 1.85 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.01 | | 0.23 | | ns |
| $t_{ESBWESU}$ | 2.07 | | 2.28 | | 2.41 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.25 | | 0.27 | | 0.29 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.04 | | 0.11 | | ns |
| $t_{ESBRADDRSU}$ | 0.14 | | 0.11 | | 0.16 | | ns |
| $t_{ESBDATACO1}$ | | 1.29 | | 1.50 | | 1.63 | ns |
| $t_{ESBDATACO2}$ | | 2.55 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.12 | | 3.57 | | 3.85 | ns |
| $t_{PD}$ | | 1.84 | | 2.13 | | 2.32 | ns |
| $t_{PTERMSU}$ | 1.08 | | 1.19 | | 1.32 | | ns |
| $t_{PTERMCO}$ | | 1.31 | | 1.53 | | 1.66 | ns |

*Table 106. EP20K1500E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 107. EP20K1500E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.09 | | 3.30 | | 3.58 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 6.18 | 2.00 | 6.81 | 2.00 | 7.36 | ns |
| $t_{INSUPLL}$ | 1.94 | | 2.08 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.67 | 0.50 | 2.99 | - | - | ns |