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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	382
Number of Gates	526000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k200bc484-1x">https://www.e-xfl.com/product-detail/intel/ep20k200bc484-1x</a>

**Table 2. Additional APEX 20K Device Features** *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

*Note to Tables 1 and 2:*

- (1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

**Table 3. APEX 20K Supply Voltages**

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage ( $V_{CCINT}$ )	2.5 V	1.8 V
MultiVolt I/O interface voltage levels ( $V_{CCIO}$ )	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

*Note to Table 3:*

- (1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock<sup>®</sup> feature reducing clock delay and skew
  - ClockBoost<sup>®</sup> feature providing clock multiplication and division
  - ClockShift<sup>™</sup> programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ( $t_{CO} + t_{SU}$ ) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast  $t_{CO}$  and  $t_{SU}$  times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see [Table 3](#))
  - Programmable clamp to  $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack<sup>®</sup> Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see [Tables 4 through 7](#))
  - FineLine BGA<sup>®</sup> packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera<sup>®</sup> Quartus<sup>®</sup> II development system for

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP<sup>SM</sup>) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS)

**Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count**    *Notes (1), (2)*

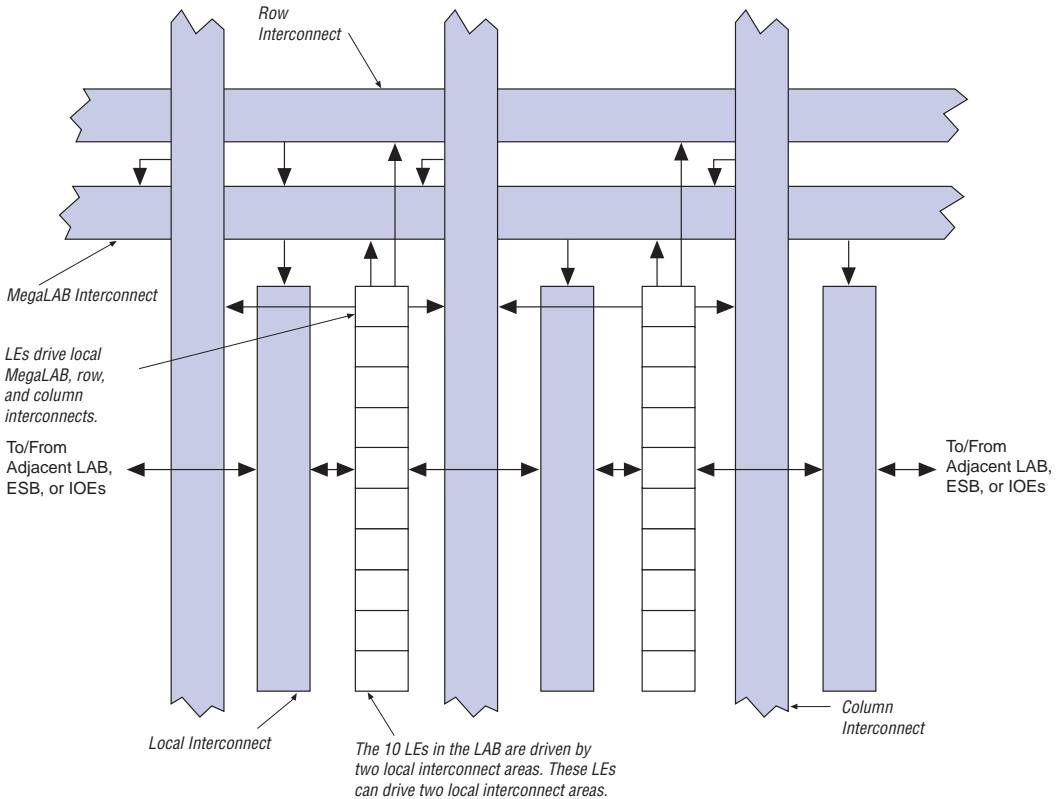
Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

**Figure 3. LAB Structure**



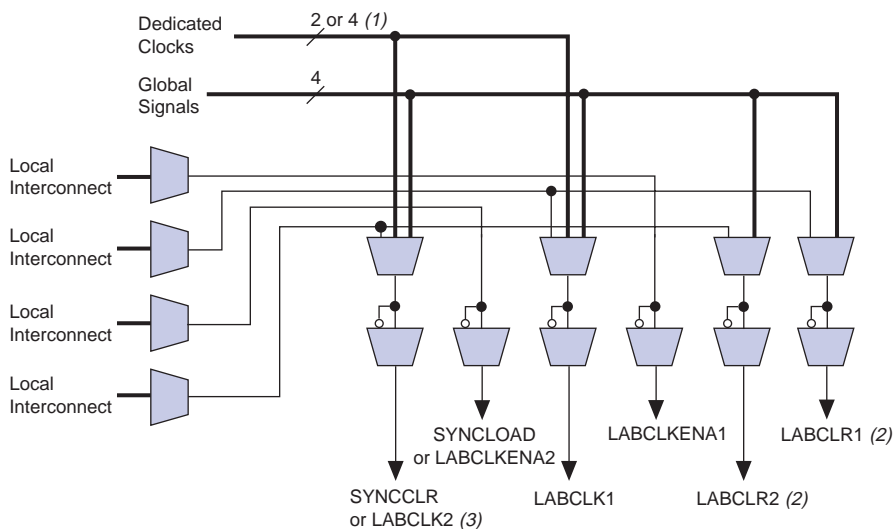
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using CLK1 will also use CLKENA1). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. **Figure 4** shows the LAB control signal generation circuit.

**Figure 4. LAB Control Signal Generation**



**Notes to Figure 4:**

- (1) APEX 20KE devices have four dedicated clocks.
- (2) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.
- (3) The SYNCCLR signal can be generated by the local interconnect or global signals.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV\_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

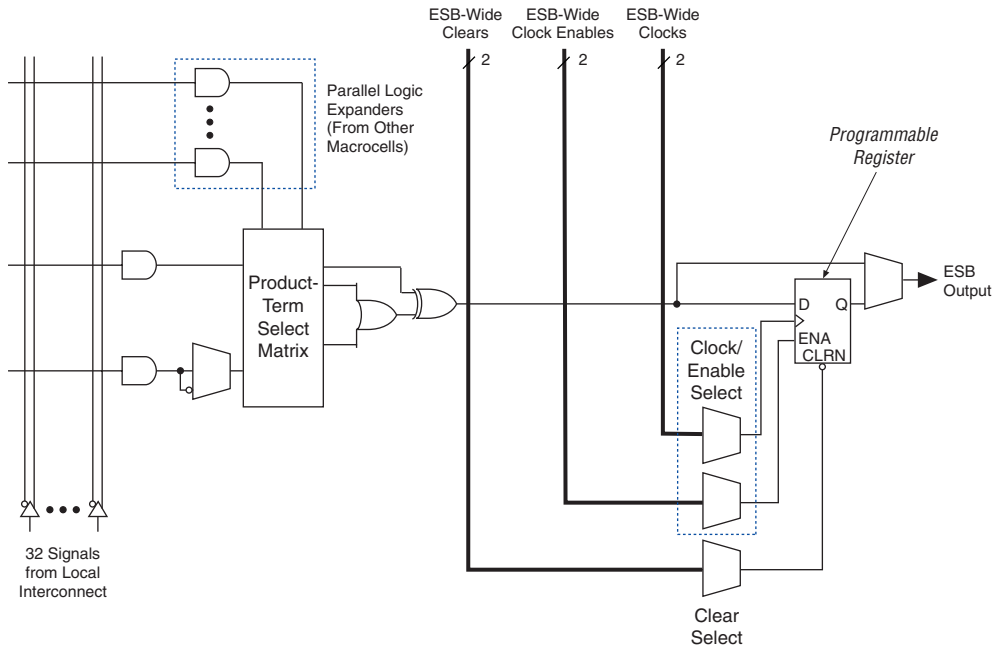
## **FastTrack Interconnect**

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See [Figure 9](#).



**Figure 14. APEX 20K Macrocell**



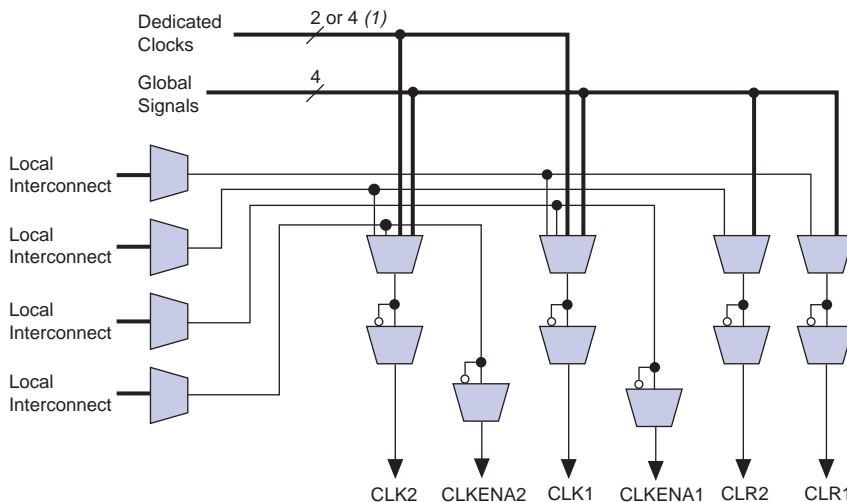
For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

**Figure 15. ESB Product-Term Mode Control Logic**



**Note to Figure 15:**

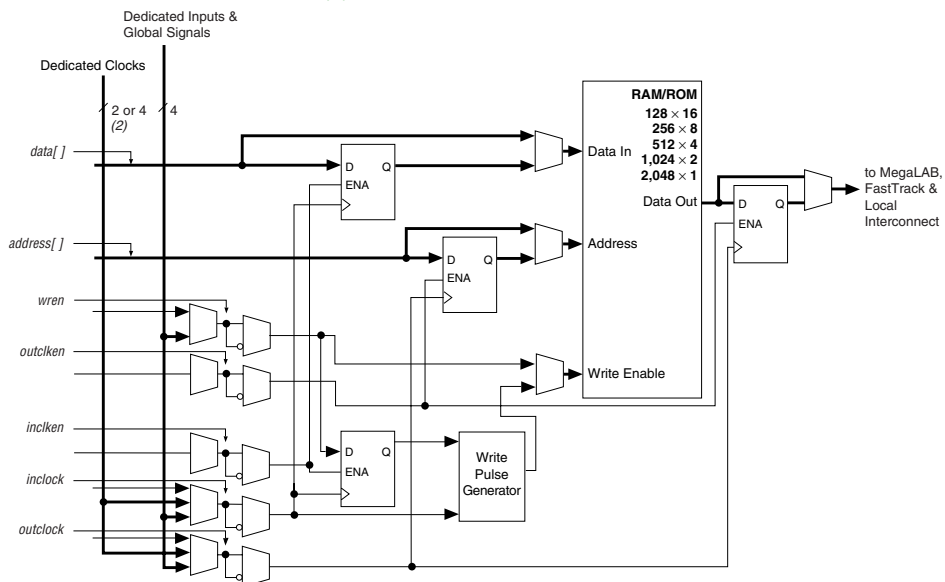
(1) APEX 20KE devices have four dedicated clocks.

### Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

**Figure 22. ESB in Single-Port Mode** *Note (1)*



Notes to **Figure 22:**

- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. [Figure 23](#) shows the CAM block diagram.

## Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

## Programmable Speed/Power Control

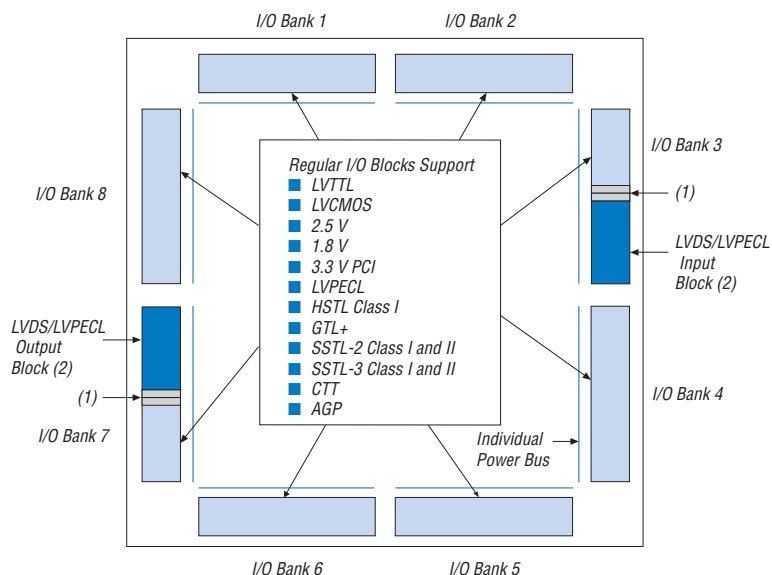
APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

**Figure 29. APEX 20KE I/O Banks**

**Notes to Figure 29:**

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with  $V_{CCIO}$  set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the  $V_{CCIO}$  and  $V_{CCINT}$  power supplies may be powered in any order.



For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

**Table 26. APEX 20K 5.0-V Tolerant Device Capacitance** *Notes (2), (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 23 through 26:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) All APEX 20K devices are 5.0-V tolerant.
- (3) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{C}$ ,  $V_{CCINT} = 2.5\text{ V}$ , and  $V_{CCIO} = 2.5\text{ or }3.3\text{ V}$ .
- (8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
- (9) The APEX 20K input buffers are compatible with  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVC MOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant when  $V_{CCIO}$  and  $V_{CCINT}$  meet the relationship shown in Figure 33 on page 68.
- (10) The  $I_{OH}$  parameter refers to high-level TTL, PCI or CMOS output current.
- (11) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (12) This value is specified for normal device operation. The value may vary during power-up.
- (13) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

**Table 27. APEX 20KE Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage	With respect to ground (2)	$-0.5$	2.5	V
$V_{CCIO}$			$-0.5$	4.6	V
$V_I$			$-0.5$	4.6	V
$I_{OUT}$	DC output current, per pin		$-25$	25	mA
$T_{STG}$	Storage temperature	No bias	$-65$	150	$^\circ\text{C}$
$T_{AMB}$	Ambient temperature	Under bias	$-65$	135	$^\circ\text{C}$
$T_J$	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	$^\circ\text{C}$
		Ceramic PGA packages, under bias		150	$^\circ\text{C}$

**Table 28. APEX 20KE Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
$V_I$	Input voltage	(5), (6)	−0.5	4.0	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Junction temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns



For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

**Table 30. APEX 20KE Device Capacitance** Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 27 through 30:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than  $100\text{ mA}$ . The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to  $100\%$  duty cycle.

$V_{IN}$	Max. Duty Cycle
$4.0\text{ V}$	$100\%$ (DC)
$4.1$	$90\%$
$4.2$	$50\%$
$4.3$	$30\%$
$4.4$	$17\%$
$4.5$	$10\%$
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 1.8\text{ V}$ , and  $V_{CCIO} = 1.8\text{ V}$ ,  $2.5\text{ V}$  or  $3.3\text{ V}$ .
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ , and  $I_I$  parameters when  $V_{CCIO} = 1.8\text{ V}$ .
- (10) The APEX 20KE input buffers are compatible with  $1.8\text{-V}$ ,  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVCMOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for  $3.3\text{-V}$  PCI compliance on APEX 20K devices.



Note to [Tables 32 and 33](#):

(1) These timing parameters are sample-tested only.

[Tables 34 through 37](#) show APEX 20KE LE, ESB, routing, and functional timing microparameters for the  $f_{MAX}$  timing model.

**Table 34. APEX 20KE LE Timing Microparameters**

Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LUT delay for data-in to data-out

**Table 35. APEX 20KE ESB Timing Microparameters**

Symbol	Parameter
$t_{ESBARC}$	ESB Asynchronous read cycle time
$t_{ESBSRC}$	ESB Synchronous read cycle time
$t_{ESBAWC}$	ESB Asynchronous write cycle time
$t_{ESBSWC}$	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
$t_{ESBWAH}$	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
$t_{ESBWDH}$	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
$t_{ESBRAH}$	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBWEH}$	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

**Table 42. EP20K400  $f_{MAX}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.1		0.3		0.6		ns
$t_H$	0.5		0.8		0.9		ns
$t_{CO}$		0.1		0.4		0.6	ns
$t_{LUT}$		1.0		1.2		1.4	ns
$t_{ESBRC}$		1.7		2.1		2.4	ns
$t_{ESBWC}$		5.7		6.9		8.1	ns
$t_{ESBWESU}$	3.3		3.9		4.6		ns
$t_{ESBDATASU}$	2.2		2.7		3.1		ns
$t_{ESBDATAH}$	0.6		0.8		0.9		ns
$t_{ESBADDRSU}$	2.4		2.9		3.3		ns
$t_{ESBDATACO1}$		1.3		1.6		1.8	ns
$t_{ESBDATACO2}$		2.5		3.1		3.6	ns
$t_{ESBDD}$		2.5		3.3		3.6	ns
$t_{PD}$		2.5		3.1		3.6	ns
$t_{PTERMSU}$	1.7		2.1		2.4		ns
$t_{PTERMCO}$		1.0		1.2		1.4	ns
$t_{F1-4}$		0.4		0.5		0.6	ns
$t_{F5-20}$		2.6		2.8		2.9	ns
$t_{F20+}$		3.7		3.8		3.9	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns
$t_{CLRP}$	0.5		0.6		0.8		ns
$t_{PREP}$	0.5		0.5		0.5		ns
$t_{ESBCH}$	2.0		2.5		3.0		ns
$t_{ESBCL}$	2.0		2.5		3.0		ns
$t_{ESBWP}$	1.5		1.9		2.2		ns
$t_{ESBRP}$	1.0		1.2		1.4		ns

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 68. EP20K160E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.65		2.02		2.11	ns
$t_{ESBSRC}$		2.21		2.70		3.11	ns
$t_{ESBAWC}$		3.04		3.79		4.42	ns
$t_{ESBSWC}$		2.81		3.56		4.10	ns
$t_{ESBWASU}$	0.54		0.66		0.73		ns
$t_{ESBWAH}$	0.36		0.45		0.47		ns
$t_{ESBWDSU}$	0.68		0.81		0.94		ns
$t_{ESBWDH}$	0.36		0.45		0.47		ns
$t_{ESBRASU}$	1.58		1.87		2.06		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.41		1.71		2.00		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.02		-0.03		0.09		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.14		0.17		0.35		ns
$t_{ESBRADDRSU}$	0.21		0.27		0.43		ns
$t_{ESBDATACO1}$		1.04		1.30		1.46	ns
$t_{ESBDATACO2}$		2.15		2.70		3.16	ns
$t_{ESBDD}$		2.69		3.35		3.97	ns
$t_{PD}$		1.55		1.93		2.29	ns
$t_{PTERMSU}$	1.01		1.23		1.52		ns
$t_{PTERMCO}$		1.06		1.32		1.04	ns

**Table 72. EP20K160E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.86		3.24		3.54		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{\text{XZBIDIR}}$		7.43		8.23		8.58	ns
$t_{\text{ZXBIDIR}}$		7.43		8.23		8.58	ns
$t_{\text{INSUBIDIRPLL}}$	4.93		5.48		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.36		5.99		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.36		5.99		-	ns

Tables 73 through 78 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

**Table 73. EP20K200E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.23		0.24		0.26		ns
$t_{\text{H}}$	0.23		0.24		0.26		ns
$t_{\text{CO}}$		0.26		0.31		0.36	ns
$t_{\text{LUT}}$		0.70		0.90		1.14	ns

**Table 86. EP20K400E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.67		1.91		1.99	ns
$t_{ESBSRC}$		2.30		2.66		2.93	ns
$t_{ESBAWC}$		3.09		3.58		3.99	ns
$t_{ESBSWC}$		3.01		3.65		4.05	ns
$t_{ESBWASU}$	0.54		0.63		0.65		ns
$t_{ESBWAH}$	0.36		0.43		0.42		ns
$t_{ESBWDSU}$	0.69		0.77		0.84		ns
$t_{ESBWDH}$	0.36		0.43		0.42		ns
$t_{ESBRASU}$	1.61		1.77		1.86		ns
$t_{ESBRAH}$	0.00		0.00		0.01		ns
$t_{ESBWESU}$	1.35		1.47		1.61		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.18		-0.30		-0.27		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	-0.02		-0.11		-0.03		ns
$t_{ESBRADDRSU}$	0.06		-0.01		-0.05		ns
$t_{ESBDATACO1}$		1.16		1.40		1.54	ns
$t_{ESBDATACO2}$		2.18		2.55		2.85	ns
$t_{ESBDD}$		2.73		3.17		3.58	ns
$t_{PD}$		1.57		1.83		2.07	ns
$t_{PTERMSU}$	0.92		0.99		1.18		ns
$t_{PTERMCO}$		1.18		1.43		1.17	ns