Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	277
Number of Gates	526000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200bi356-3

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
    - Built-in low-skew clock tree
    - Up to eight global clock signals
    - ClockLock® feature reducing clock delay and skew
    - ClockBoost® feature providing clock multiplication and division
    - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
    - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2* for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
    - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
    - Bidirectional I/O performance ($t_{CO} + t_{SU}$) up to 250 MHz
    - LVDS performance up to 840 Mbits per channel
    - Direct connection from I/O pins to local interconnect providing fast t_{CO} and t_{SU} times for complex logic
    - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
    - Programmable clamp to V_{CCIO}
    - Individual tri-state output enable control for each pin
    - Programmable output slew-rate control to reduce switching noise
    - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
    - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
    - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
    - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
    - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
    - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
    - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
    - FineLine BGA® packages maximize board space efficiency
- Advanced software support
    - Software design support and automatic place-and-route provided by the Altera® Quartus® II development system for

Table 8. Comparison of APEX 20K & APEX 20KE Features

Feature	APEX 20K Devices	APEX 20KE Devices
MultiCore system integration	Full support	Full support
SignalTap logic analysis	Full support	Full support
32/64-Bit, 33-MHz PCI	Full compliance in -1, -2 speed grades	Full compliance in -1, -2 speed grades
32/64-Bit, 66-MHz PCI	-	Full compliance in -1 speed grade
MultiVolt I/O	2.5-V or 3.3-V V_{CCIO} V_{CCIO} selected for device Certain devices are 5.0-V tolerant	1.8-V, 2.5-V, or 3.3-V V_{CCIO} V_{CCIO} selected block-by-block 5.0-V tolerant with use of external resistor
ClockLock support	Clock delay reduction $2\times$ and $4\times$ clock multiplication	Clock delay reduction $m/(n \times v)$ or $m/(n \times k)$ clock multiplication Drive ClockLock output off-chip External clock feedback ClockShift LVDS support Up to four PLLs ClockShift, clock phase adjustment
Dedicated clock and input pins	Six	Eight
I/O standard support	2.5-V, 3.3-V, 5.0-V I/O 3.3-V PCI Low-voltage complementary metal-oxide semiconductor (LVCMOS) Low-voltage transistor-to-transistor logic (LVTTL)	1.8-V, 2.5-V, 3.3-V, 5.0-V I/O 2.5-V I/O 3.3-V PCI and PCI-X 3.3-V Advanced Graphics Port (AGP) Center tap terminated (CTT) GTL+ LVCMOS LVTTL True-LVDS and LVPECL data pins (in EP20K300E and larger devices) LVDS and LVPECL signaling (in all BGA and FineLine BGA devices) LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices) HSTL Class I PCI-X SSTL-2 Class I and II SSTL-3 Class I and II
Memory support	Dual-port RAM FIFO RAM ROM	CAM Dual-port RAM FIFO RAM ROM

APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.
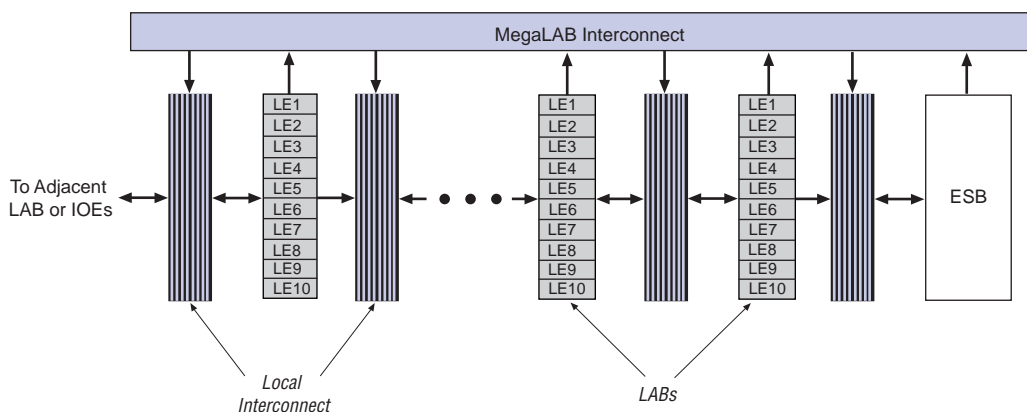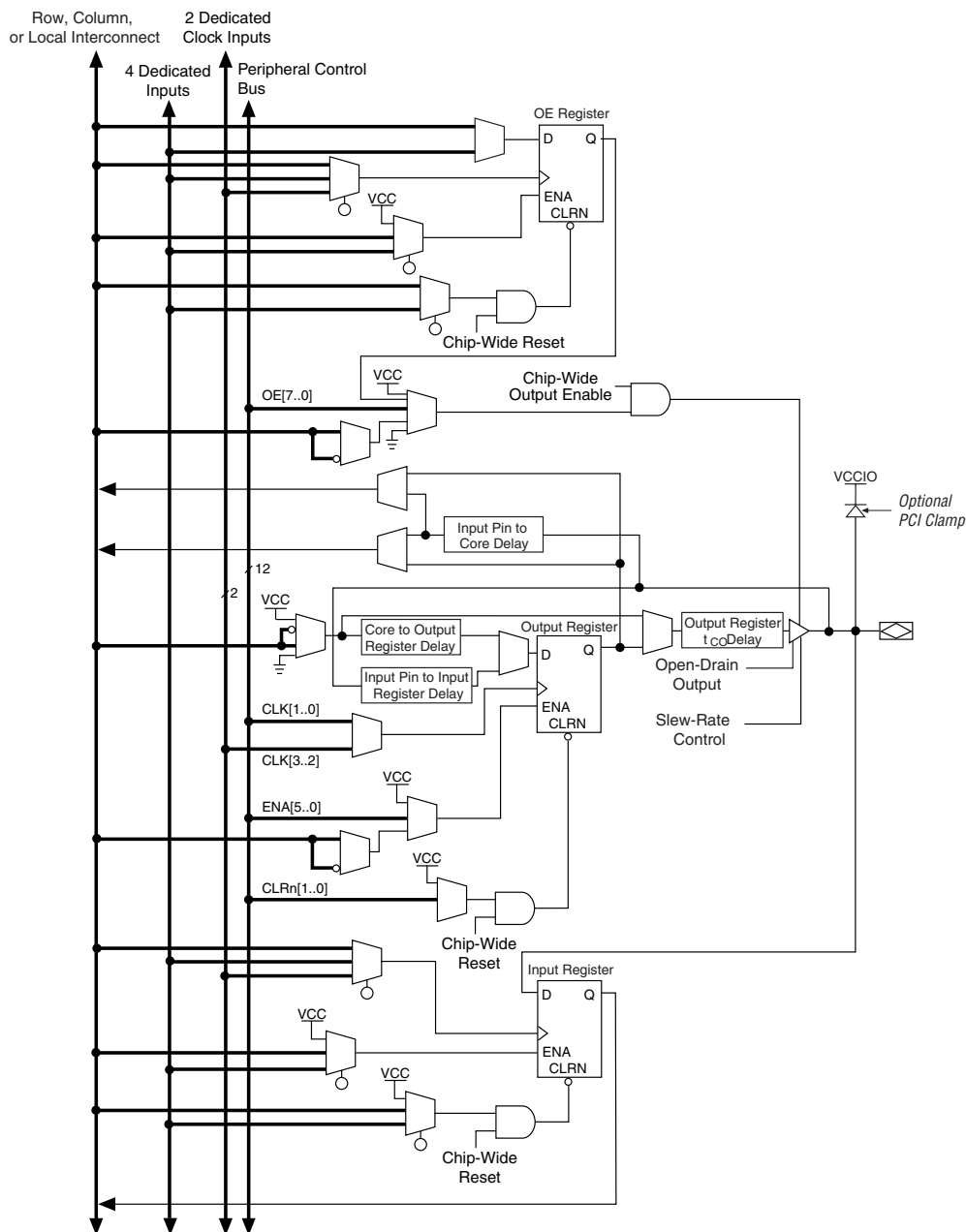
Figure 2. MegaLAB Structure

Figure 25. APEX 20K Bidirectional I/O Registers *Note (1)*

Note to Figure 25:
(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

Figure 29. APEX 20KE I/O Banks
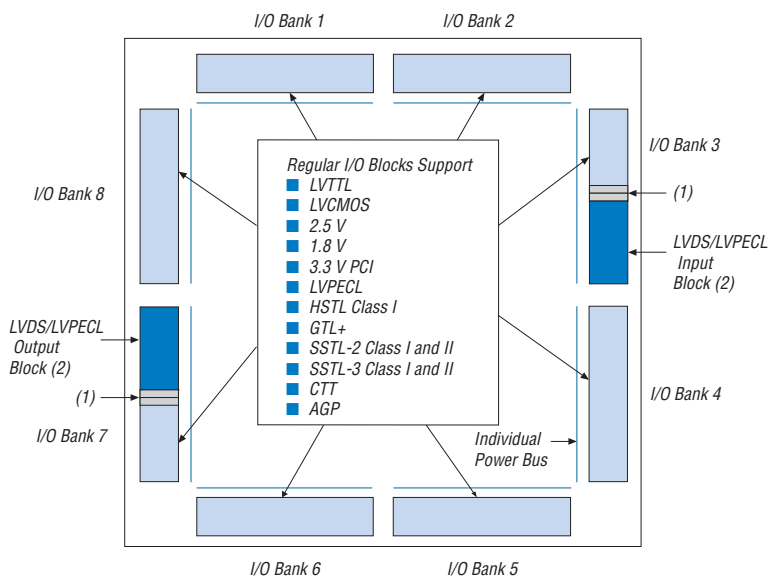
Notes to *Figure 29*:
(1)   For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
(2)   If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V V_{CCINT} level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support						
V_{CCIO} (V)	Input Signals (V)			Output Signals (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✔	✔(1)	✔(1)	✔		
3.3	✔	✔	✔(1)	✔(2)	✔	✔

Notes to Table 12:
(1)	The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.
(2)	When V_{CCIO} = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

Table 19. APEX 20K JTAG Instructions	
JTAG Instruction	**Description**
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS *(1)*	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`.
IDCODE	Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`.
ICR Instructions	Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap Instructions *(1)*	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 19:

(1)   The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

Figure 32. APEX 20K AC Test Conditions   *Note (1)*
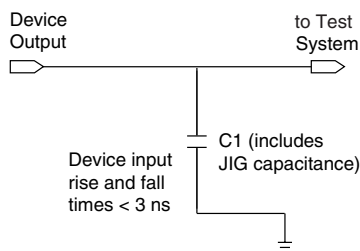
Note to Figure 32:

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings   *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	−0.5	3.6	V
V_{CCIO}			−0.5	4.6	V
V_I	DC input voltage		−2.0	5.75	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions   *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V$_{CCINT}$	Supply voltage for internal logic and input buffers	*(4)*, *(5)*	2.375 (2.375)	2.625 (2.625)	V
V$_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*, *(5)*	2.375 (2.375)	2.625 (2.625)	V
V$_I$	Input voltage	*(3)*, *(6)*	−0.5	5.75	V
V$_O$	Output voltage		0	V$_{CCIO}$	V
T$_J$	Junction temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t$_R$	Input rise time			40	ns
t$_F$	Input fall time			40	ns

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions *(Part 1 of 2)*   *Notes (2)*, *(7)*, *(8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V$_{IH}$	High-level input voltage		1.7, 0.5 × V$_{CCIO}$ *(9)*		5.75	V
V$_{IL}$	Low-level input voltage		−0.5		0.8, 0.3 × V$_{CCIO}$ *(9)*	V
V$_{OH}$	3.3-V high-level TTL output voltage	I$_{OH}$ = −8 mA DC, V$_{CCIO}$ = 3.00 V *(10)*	2.4			V
	3.3-V high-level CMOS output voltage	I$_{OH}$ = −0.1 mA DC, V$_{CCIO}$ = 3.00 V *(10)*	V$_{CCIO}$ − 0.2			V
	3.3-V high-level PCI output voltage	I$_{OH}$ = −0.5 mA DC, V$_{CCIO}$ = 3.00 to 3.60 V *(10)*	0.9 × V$_{CCIO}$			V
	2.5-V high-level output voltage	I$_{OH}$ = −0.1 mA DC, V$_{CCIO}$ = 2.30 V *(10)*	2.1			V
		I$_{OH}$ = −1 mA DC, V$_{CCIO}$ = 2.30 V *(10)*	2.0			V
		I$_{OH}$ = −2 mA DC, V$_{CCIO}$ = 2.30 V *(10)*	1.7			V

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices   Note (1)
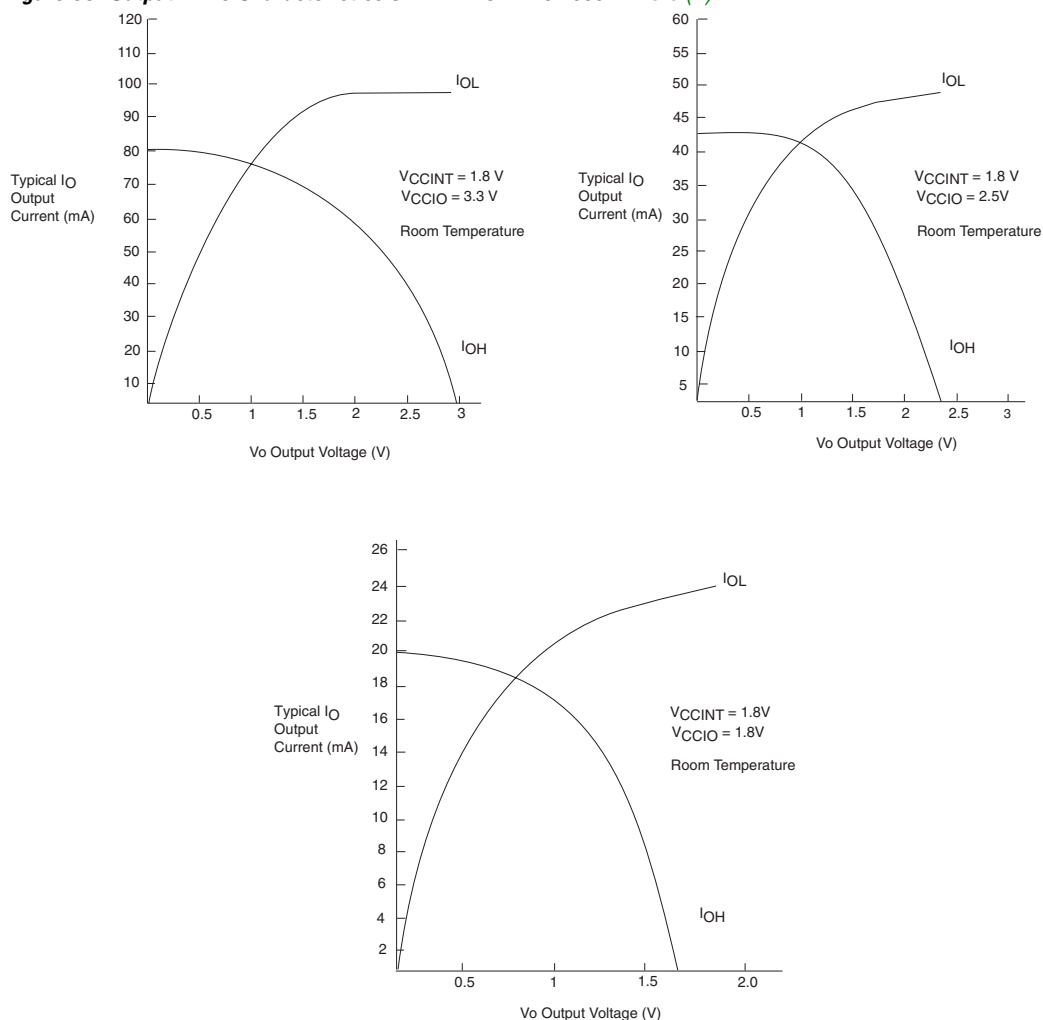
Note to Figure 35:
(1)   These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms

ESB Asynchronous Read

ESB Asynchronous Write
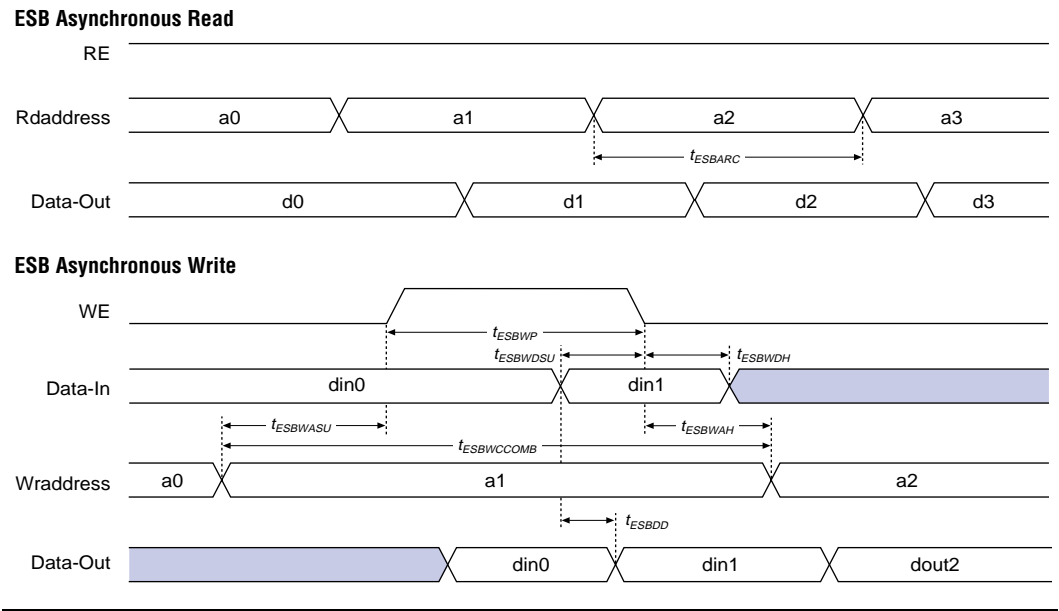
Note to Tables 32 and 33:

(1)   These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the f_{MAX} timing model.

Table 34. APEX 20KE LE Timing Microparameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 35. APEX 20KE ESB Timing Microparameters

Symbol	Parameter
t_{ESBARC}	ESB Asynchronous read cycle time
t_{ESBSRC}	ESB Synchronous read cycle time
t_{ESBAWC}	ESB Asynchronous write cycle time
t_{ESBSWC}	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
t_{ESBWEH}	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

Table 60. EP20K60E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.77		2.91		3.11		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{XZBIDIR}$		6.47		7.44		8.65	ns
$t_{ZXBIDIR}$		6.47		7.44		8.65	ns
$t_{INSUBIDIRPLL}$	3.44		3.24		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.37	0.50	3.69	-	-	ns
$t_{XZBIDIRPLL}$		5.00		5.82		-	ns
$t_{ZXBIDIRPLL}$		5.00		5.82		-	ns

Tables 61 through 66 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

Table 61. EP20K100E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.28		0.34	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 62. EP20K100E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.61		1.84		1.97	ns
t_{ESBSRC}		2.57		2.97		3.20	ns
t_{ESBAWC}		0.52		4.09		4.39	ns
t_{ESBSWC}		3.17		3.78		4.09	ns
t_{ESBWASU}	0.56		6.41		0.63		ns
t_{ESBWAH}	0.48		0.54		0.55		ns
t_{ESBWDSU}	0.71		0.80		0.81		ns
t_{ESBWDH}	.048		0.54		0.55		ns
t_{ESBRASU}	1.57		1.75		1.87		ns
t_{ESBRAH}	0.00		0.00		0.20		ns
t_{ESBWESU}	1.54		1.72		1.80		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
t_{ESBDATASU}	-0.16		-0.20		-0.20		ns
t_{ESBDATAH}	0.13		0.13		0.13		ns
t_{ESBWADDRSU}	0.12		0.08		0.13		ns
t_{ESBRADDRSU}	0.17		0.15		0.19		ns
t_{ESBDATACO1}		1.20		1.39		1.52	ns
t_{ESBDATACO2}		2.54		2.99		3.22	ns
t_{ESBDD}		3.06		3.56		3.85	ns
t_{PD}		1.73		2.02		2.20	ns
t_{PTERMSU}	1.11		1.26		1.38		ns
t_{PTERMCO}		1.19		1.40		1.08	ns

Table 63. EP20K100E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.29	ns
t_{F5-20}		1.04		1.26		1.52	ns
t_{F20+}		1.12		1.36		1.86	ns

Tables 67 through 72 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

Table 67. EP20K160E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.24		0.26		ns
t_H	0.22		0.24		0.26		ns
t_{CO}		0.25		0.31		0.35	ns
t_{LUT}		0.69		0.88		1.12	ns

Table 72. EP20K160E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.86		3.24		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{XZBIDIR}$		7.43		8.23		8.58	ns
$t_{ZXBIDIR}$		7.43		8.23		8.58	ns
$t_{INSUBIDIRPLL}$	4.93		5.48		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{XZBIDIRPLL}$		5.36		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.36		5.99		-	ns

Tables 73 through 78 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

Table 73. EP20K200E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.24		0.26		ns
t_{H}	0.23		0.24		0.26		ns
t_{CO}		0.26		0.31		0.36	ns
t_{LUT}		0.70		0.90		1.14	ns

Table 92. EP20K600E f*MAX* ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		2.39		3.11	ns
t_{ESBSRC}		2.27		3.07		3.86	ns
t_{ESBAWC}		3.19		4.56		5.93	ns
t_{ESBSWC}		3.51		4.62		5.72	ns
t_{ESBWASU}	1.46		2.08		2.70		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
t_{ESBWDSU}	1.60		2.29		2.97		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
t_{ESBRASU}	1.61		2.30		2.99		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
t_{ESBWESU}	1.49		2.30		3.11		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
t_{ESBDATASU}	-0.01		0.35		0.71		ns
t_{ESBDATAH}	0.13		0.13		0.13		ns
t_{ESBWADDRSU}	0.19		0.62		1.06		ns
t_{ESBRADDRSU}	0.25		0.71		1.17		ns
t_{ESBDATACO1}		1.01		1.19		1.37	ns
t_{ESBDATACO2}		2.18		3.12		4.05	ns
t_{ESBDD}		3.19		4.56		5.93	ns
t_{PD}		1.57		2.25		2.92	ns
t_{PTERMSU}	0.85		1.43		2.01		ns
t_{PTERMCO}		1.03		1.21		1.39	ns

Table 93. EP20K600E f*MAX* Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.25		0.26	ns
t_{F5-20}		1.26		1.39		1.52	ns
t_{F20+}		3.51		3.88		4.26	ns

Table 99. EP20K1000E f_MAX Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.27		0.27		0.27	ns
t_{F5-20}		1.45		1.63		1.75	ns
t_{F20+}		4.15		4.33		4.97	ns

Table 100. EP20K1000E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 101. EP20K1000E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.70		2.84		2.97		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{INSUPLL}$	1.64		2.09		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com

nsai

I.S. EN ISO 9001