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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	832
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	271
Number of Gates	-
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k200ebc356-1

Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan’s inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain

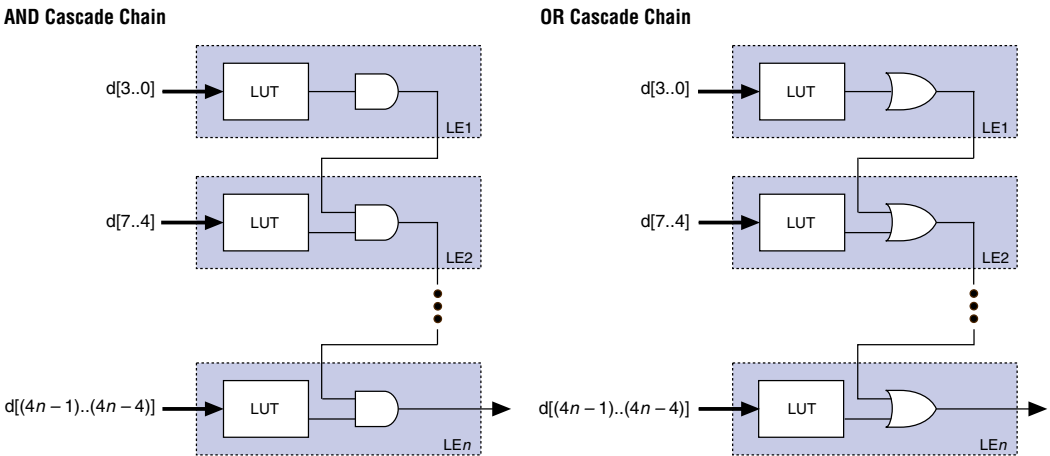


Figure 10. FastTrack Connection to Local Interconnect

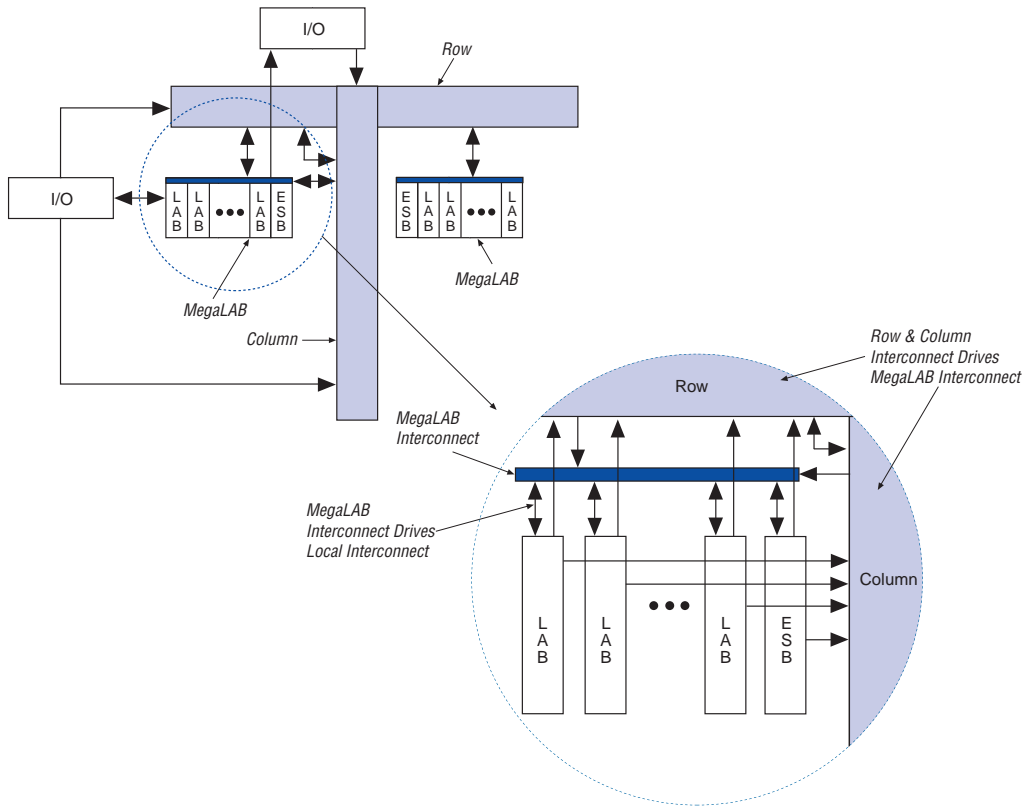


Table 9. APEX 20K Routing Scheme

Source	Destination								
	Row I/O Pin	Column I/O Pin	LE	ESB	Local Interconnect	MegaLAB Interconnect	Row FastTrack Interconnect	Column FastTrack Interconnect	FastRow Interconnect
Row I/O Pin					✓	✓	✓	✓	
Column I/O Pin								✓	✓ (1)
LE					✓	✓	✓	✓	
ESB					✓	✓	✓	✓	
Local Interconnect	✓	✓	✓	✓					
MegaLAB Interconnect					✓				
Row FastTrack Interconnect						✓		✓	
Column FastTrack Interconnect						✓	✓		
FastRow Interconnect					✓ (1)				

Note to **Table 9**:

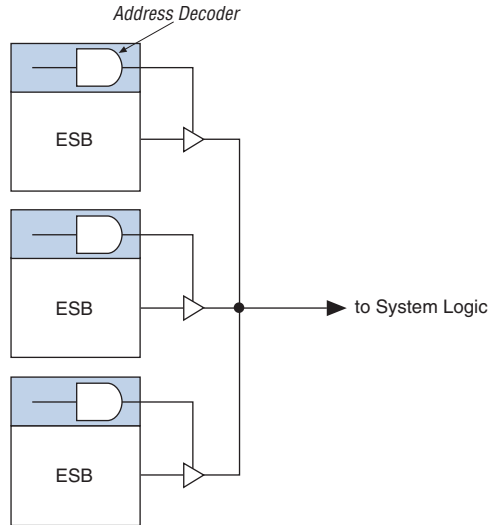
(1) This connection is supported in APEX 20KE devices only.

Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. **Figure 13** shows the ESB in product-term mode.

Figure 18. Deep Memory Block Implemented with Multiple ESBs



The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in [Figure 19](#).

Figure 19. APEX 20K ESB Implementing Dual-Port RAM

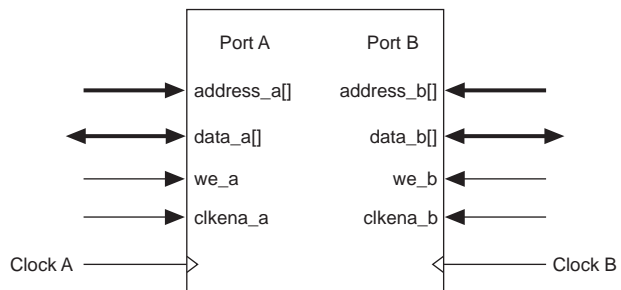


Figure 23. APEX 20KE CAM Block Diagram



CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

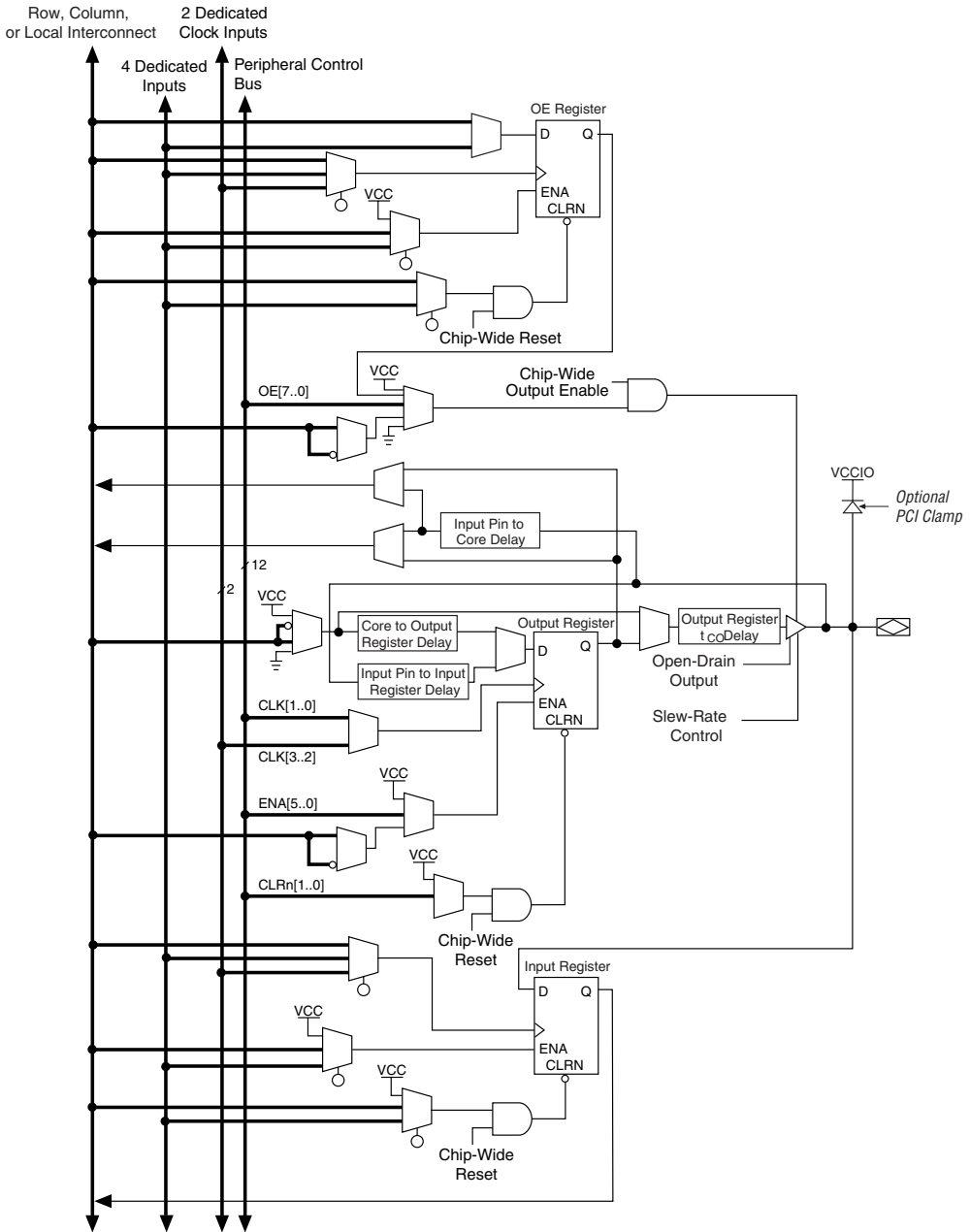
CAM supports writing “don’t care” bits into words of the memory. The “don’t-care” bit can be used as a mask for CAM comparisons; any bit set to “don’t-care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t-care” bits are used, a third clock cycle is required.

Figure 25. APEX 20K Bidirectional I/O Registers Note (1)



Note to Figure 25:

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

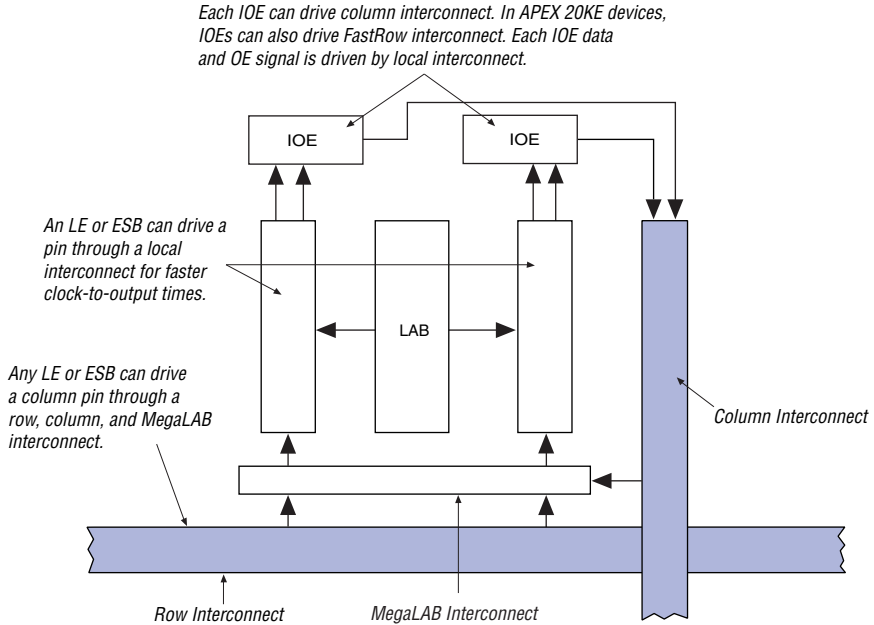
Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

<i>Table 11. APEX 20KE Programmable Delay Chains</i>	
Programmable Delays	Quartus II Logic Option
Input Pin to Core Delay	Decrease input delay to internal cells
Input Pin to Input Register Delay	Decrease input delay to input registers
Core to Output Register Delay	Decrease input delay to output register
Output Register t_{CO} Delay	Increase delay to output pin
Clock Enable Delay	Increase clock enable delay

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

Figure 28 shows how a column IOE connects to the interconnect.

Figure 28. Column IOE Connection to the Interconnect



Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.



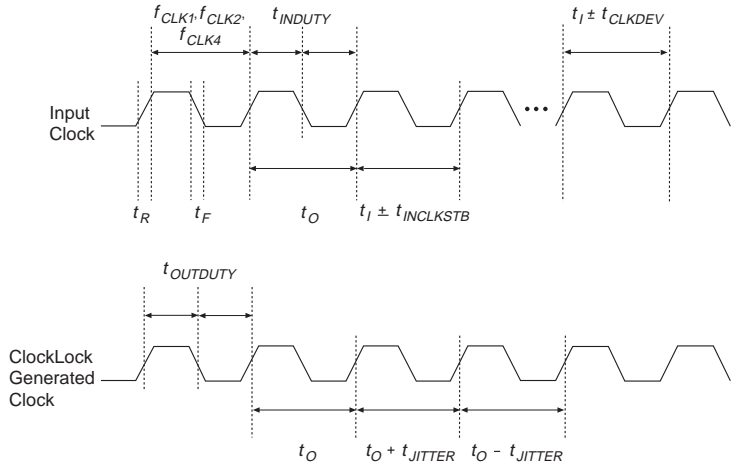
For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. [Figure 29](#) shows the arrangement of the APEX 20KE I/O banks.

Figure 30. Specifications for the Incoming & Generated Clocks *Note (1)*



Note to Figure 30:

(1) The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	180	MHz
f_{CLK1} (1)	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	180 (1)	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	90	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	48	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) (2)		25,000 (3)	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ClockBoost to acquire lock (4)		10	μ s

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) (2)
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 21:

- (1) The most significant bit (MSB) is on the left.
- (2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

Figure 31. APEX 20K JTAG Waveforms

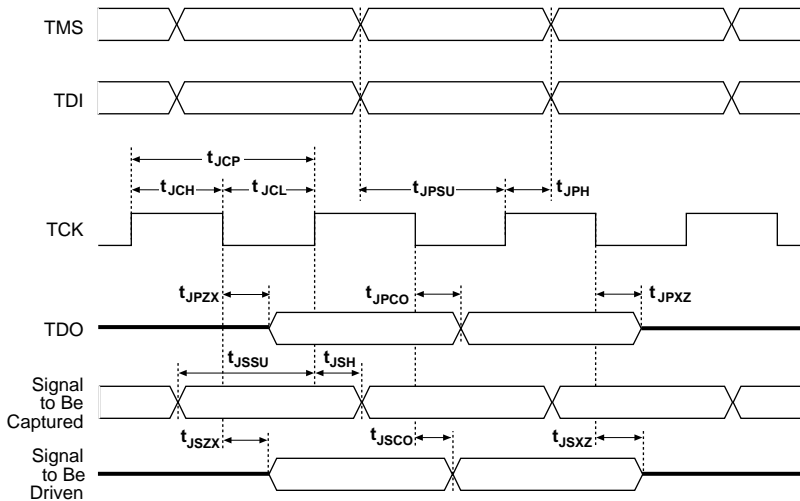


Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

Symbol	Parameter	Min	Max	Unit
t _{JCP}	TCK clock period	100		ns
t _{JCH}	TCK clock high time	50		ns
t _{JCL}	TCK clock low time	50		ns
t _{JPSU}	JTAG port setup time	20		ns
t _{JPH}	JTAG port hold time	45		ns
t _{JPCO}	JTAG port clock to output		25	ns
t _{JPZX}	JTAG port high impedance to valid output		25	ns
t _{JPXZ}	JTAG port valid output to high impedance		25	ns
t _{JSSU}	Capture register setup time	20		ns
t _{JSH}	Capture register hold time	45		ns
t _{JSCO}	Update register clock to output		35	ns
t _{JSZX}	Update register high impedance to valid output		35	ns
t _{JSXZ}	Update register valid output to high impedance		35	ns



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

Table 28. APEX 20KE Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	(5), (6)	-0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	°C
		For industrial use	-40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns



For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

Table 30. APEX 20KE Device Capacitance Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on dedicated clock pin	V _{IN} = 0 V, f = 1.0 MHz		12	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to Tables 27 through 30:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
- (5) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

V _{in}	Max. Duty Cycle
4.0V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (7) Typical values are for T_A = 25° C, V_{CCINT} = 1.8 V, and V_{CCIO} = 1.8 V, 2.5 V or 3.3 V.
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the V_{IH}, V_{IL}, V_{OH}, V_{OL}, and I_I parameters when V_{CCIO} = 1.8 V.
- (10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO}.
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance on APEX 20K devices.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the f_{MAX} timing model for APEX 20K devices.

Figure 36. APEX 20K t_{MAX} Timing Model

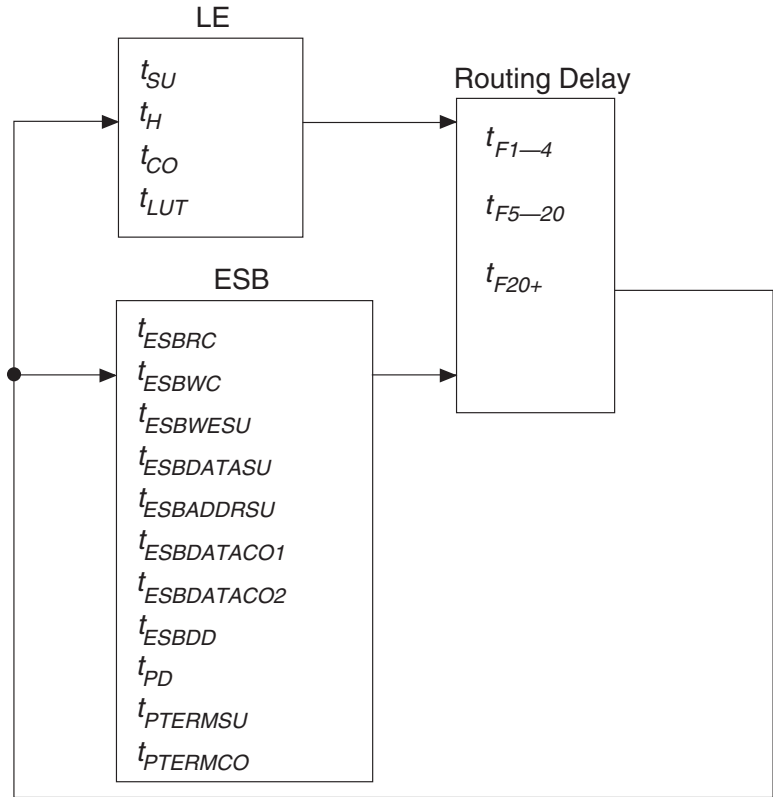


Figure 37 shows the f_{MAX} timing model for APEX 20KE devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Figure 39. ESB Synchronous Timing Waveforms

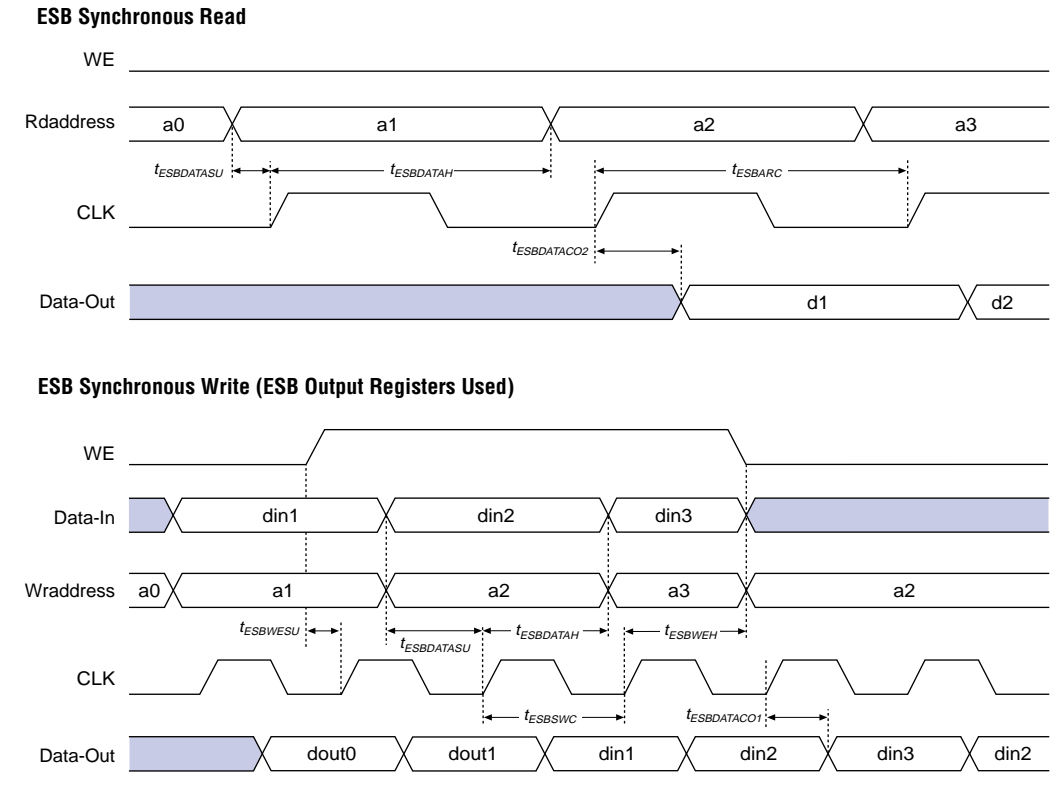


Figure 40 shows the timing model for bidirectional I/O pin timing.

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU} (1)$	2.3		2.8		3.2		ns
$t_{INH} (1)$	0.0		0.0		0.0		ns
$t_{OUTCO} (1)$	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{INSU} (2)$	1.1		1.2		–		ns
$t_{INH} (2)$	0.0		0.0		–		ns
$t_{OUTCO} (2)$	0.5	2.7	0.5	3.1	–	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR} (1)$	2.3		2.8		3.2		ns
$t_{INHBIDIR} (1)$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR} (1)$	2.0	4.5	2.0	4.9	2.0	6.6	ns
$t_{XZBIDIR} (1)$		5.0		5.9		6.9	ns
$t_{ZXBIDIR} (1)$		5.0		5.9		6.9	ns
$t_{INSUBIDIR} (2)$	1.0		1.2		–		ns
$t_{INHBIDIR} (2)$	0.0		0.0		–		ns
$t_{OUTCOBIDIR} (2)$	0.5	2.7	0.5	3.1	–	–	ns
$t_{XZBIDIR} (2)$		4.3		5.0		–	ns
$t_{ZXBIDIR} (2)$		4.3		5.0		–	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU} (1)$	1.9		2.3		2.6		ns
$t_{INH} (1)$	0.0		0.0		0.0		ns
$t_{OUTCO} (1)$	2.0	4.6	2.0	5.6	2.0	6.8	ns
$t_{INSU} (2)$	1.1		1.2		–		ns
$t_{INH} (2)$	0.0		0.0		–		ns
$t_{OUTCO} (2)$	0.5	2.7	0.5	3.1	–	–	ns

Table 52. EP20K30E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	0.55		0.78		1.15		ns
t _{CL}	0.55		0.78		1.15		ns
t _{CLRP}	0.22		0.31		0.46		ns
t _{PREP}	0.22		0.31		0.46		ns
t _{ESBCH}	0.55		0.78		1.15		ns
t _{ESBCL}	0.55		0.78		1.15		ns
t _{ESBWP}	1.43		2.01		2.97		ns
t _{ESBRP}	1.15		1.62		2.39		ns

Table 53. EP20K30E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.02		2.13		2.24		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	4.88	2.00	5.36	2.00	5.88	ns
t _{INSUPLL}	2.11		2.23		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.60	0.50	2.88	-	-	ns

Table 54. EP20K30E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	1.85		1.77		1.54		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	4.88	2.00	5.36	2.00	5.88	ns
t _{XZBIDIR}		7.48		8.46		9.83	ns
t _{ZXBIDIR}		7.48		8.46		9.83	ns
t _{INSUBIDIRPLL}	4.12		4.24		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.60	0.50	2.88	-	-	ns
t _{XZBIDIRPLL}		5.21		5.99		-	ns
t _{ZXBIDIRPLL}		5.21		5.99		-	ns

Table 82. EP20K300E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{CH}	1.25		1.43		1.67		ns
t _{CL}	1.25		1.43		1.67		ns
t _{CLRP}	0.19		0.26		0.35		ns
t _{PREP}	0.19		0.26		0.35		ns
t _{ESBCH}	1.25		1.43		1.67		ns
t _{ESBCL}	1.25		1.43		1.67		ns
t _{ESBWP}	1.25		1.71		2.28		ns
t _{ESBRP}	1.01		1.38		1.84		ns

Table 83. EP20K300E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU}	2.31		2.44		2.57		ns
t _{INH}	0.00		0.00		0.00		ns
t _{OUTCO}	2.00	5.29	2.00	5.82	2.00	6.24	ns
t _{INSUPLL}	1.76		1.85		-		ns
t _{INHPLL}	0.00		0.00		-		ns
t _{OUTCOPLL}	0.50	2.65	0.50	2.95	-	-	ns

Table 84. EP20K300E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR}	2.77		2.85		3.11		ns
t _{INHBIDIR}	0.00		0.00		0.00		ns
t _{OUTCOBIDIR}	2.00	5.29	2.00	5.82	2.00	6.24	ns
t _{XZBIDIR}		7.59		8.30		9.09	ns
t _{ZXBIDIR}		7.59		8.30		9.09	ns
t _{INSUBIDIRPLL}	2.50		2.76		-		ns
t _{INHBIDIRPLL}	0.00		0.00		-		ns
t _{OUTCOBIDIRPLL}	0.50	2.65	0.50	2.95	-	-	ns
t _{XZBIDIRPLL}		5.00		5.43		-	ns
t _{ZXBIDIRPLL}		5.00		5.43		-	ns

Table 92. EP20K600E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.67		2.39		3.11	ns
t_{ESBSRC}		2.27		3.07		3.86	ns
t_{ESBAWC}		3.19		4.56		5.93	ns
t_{ESBSWC}		3.51		4.62		5.72	ns
$t_{ESBWASU}$	1.46		2.08		2.70		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.60		2.29		2.97		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.61		2.30		2.99		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.49		2.30		3.11		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.01		0.35		0.71		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.19		0.62		1.06		ns
$t_{ESBRADDRSU}$	0.25		0.71		1.17		ns
$t_{ESBDATACO1}$		1.01		1.19		1.37	ns
$t_{ESBDATACO2}$		2.18		3.12		4.05	ns
t_{ESBDD}		3.19		4.56		5.93	ns
t_{PD}		1.57		2.25		2.92	ns
$t_{PTERMSU}$	0.85		1.43		2.01		ns
$t_{PTERMCO}$		1.03		1.21		1.39	ns

Table 93. EP20K600E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.22		0.25		0.26	ns
t_{F5-20}		1.26		1.39		1.52	ns
t_{F20+}		3.51		3.88		4.26	ns