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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	376
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	652-BGA
Supplier Device Package	652-BGA (45x45)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k200ebc652-1x">https://www.e-xfl.com/product-detail/intel/ep20k200ebc652-1x</a>

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations

- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP<sup>SM</sup>) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS )

**Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count** *Notes (1), (2)*

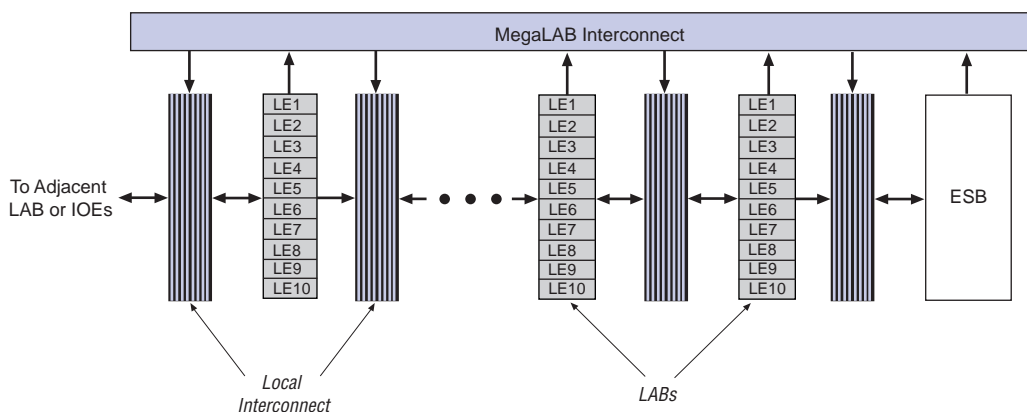
Device	144-Pin TQFP	208-Pin PQFP RQFP	240-Pin PQFP RQFP	356-Pin BGA	652-Pin BGA	655-Pin PGA
EP20K30E	92	125				
EP20K60E	92	148	151	196		
EP20K100	101	159	189	252		
EP20K100E	92	151	183	246		
EP20K160E	88	143	175	271		
EP20K200		144	174	277		
EP20K200E		136	168	271	376	
EP20K300E			152		408	
EP20K400					502	502
EP20K400E					488	
EP20K600E					488	
EP20K1000E					488	
EP20K1500E					488	

APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

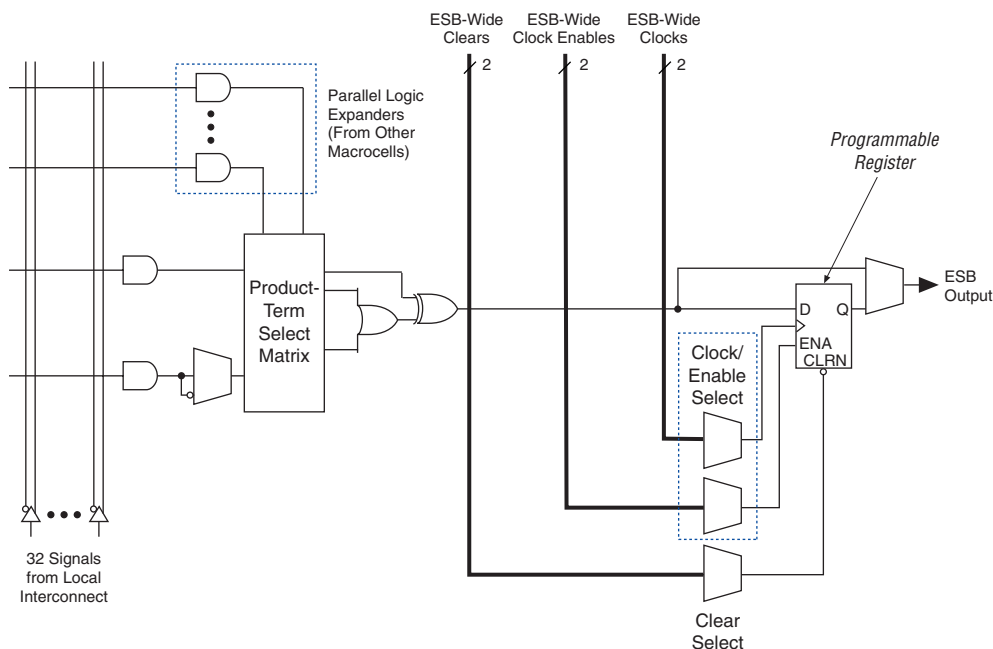
## MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

**Figure 2. MegaLAB Structure**



**Figure 14. APEX 20K Macrocell**

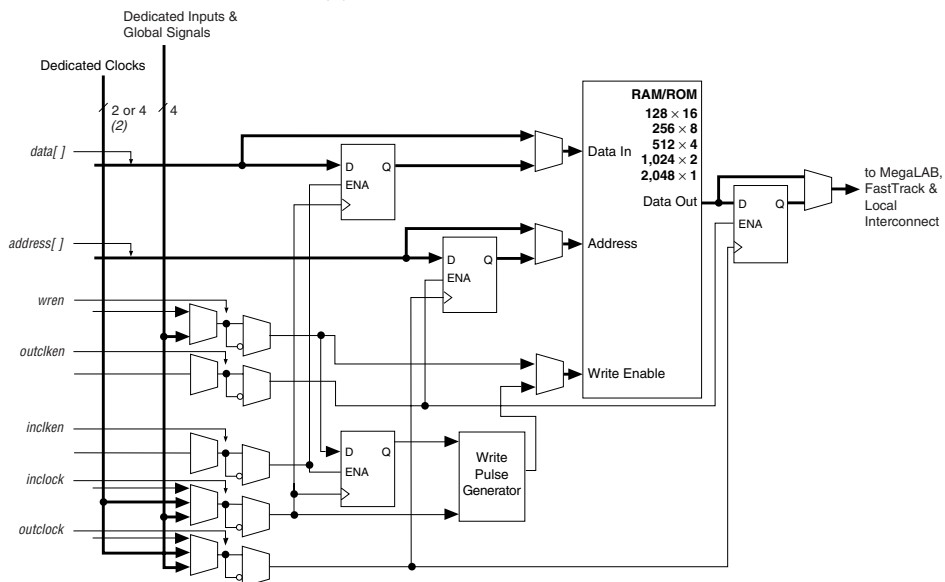


For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

**Figure 22. ESB in Single-Port Mode** *Note (1)*



*Notes to Figure 22:*

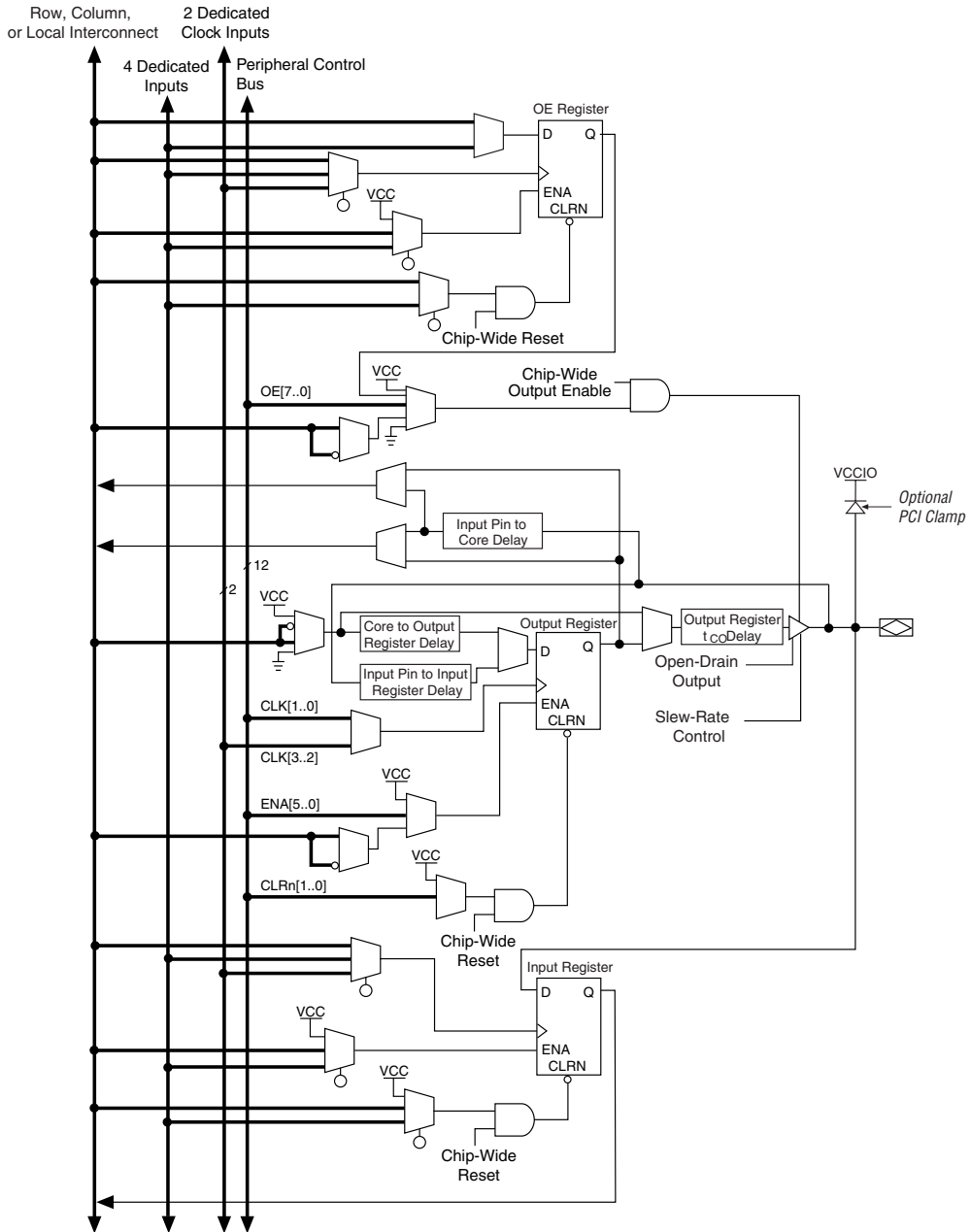
- (1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. [Figure 23](#) shows the CAM block diagram.

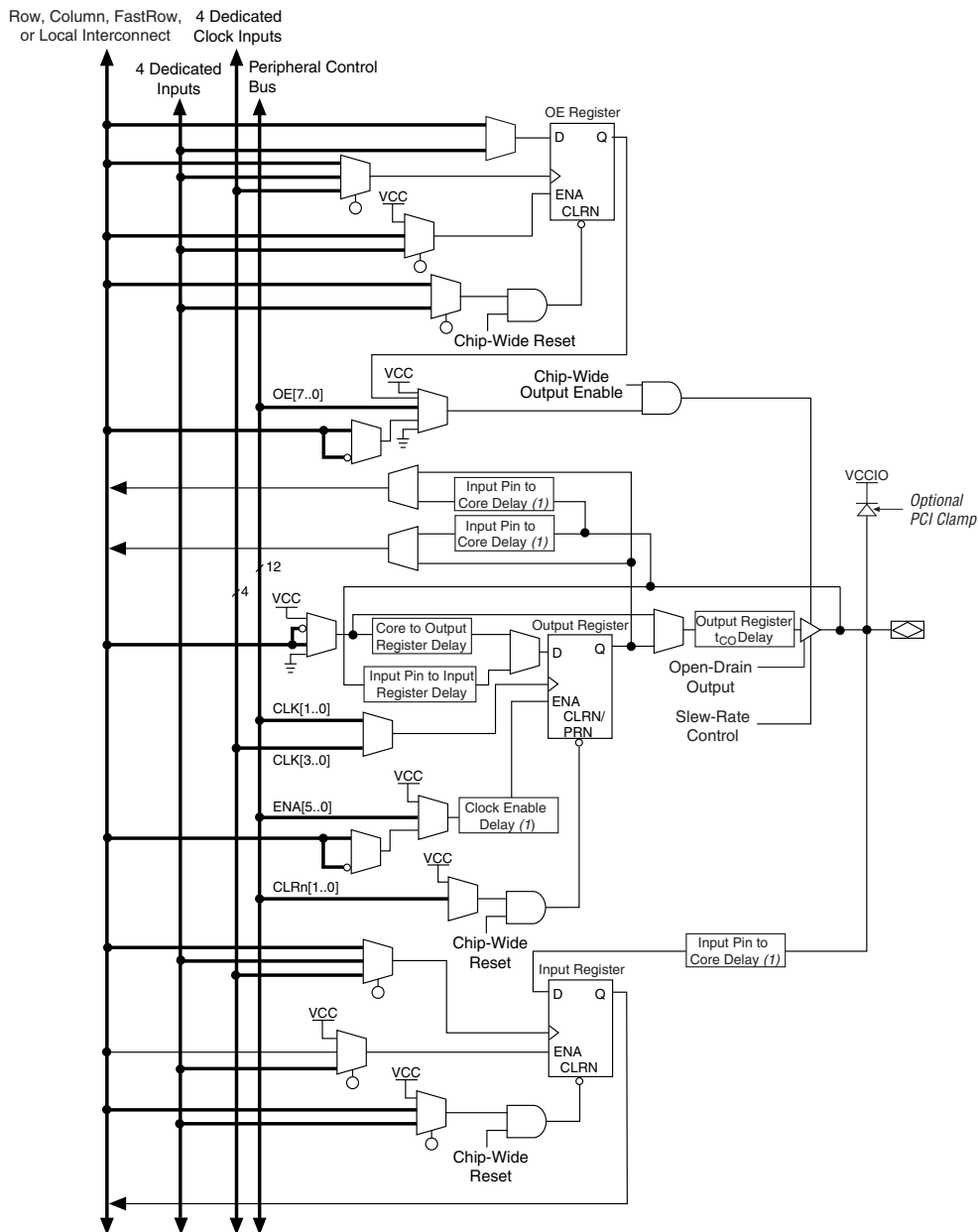
**Figure 25. APEX 20K Bidirectional I/O Registers** *Note (1)*



**Note to Figure 25:**

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

**Figure 26. APEX 20KE Bidirectional I/O Registers** *Notes (1), (2)*



**Notes to Figure 26:**

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

**Table 14. Multiplication Factor Combinations**

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

## APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

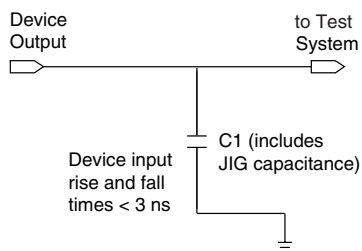
The following sections describe some of the features offered by the APEX 20KE PLLs.

### External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

### Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by  $m/(n \times k)$  or  $m/(n \times v)$ , where  $m$  and  $k$  range from 2 to 160, and  $n$  and  $v$  range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

**Figure 32. APEX 20K AC Test Conditions** *Note (1)*


**Note to Figure 32:**

- (1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

**Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings** *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage	With respect to ground (3)	–0.5	3.6	V
$V_{CCIO}$			–0.5	4.6	V
$V_I$			–2.0	5.75	V
$I_{OUT}$	DC output current, per pin		–25	25	mA
$T_{STG}$	Storage temperature	No bias	–65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	–65	135	°C
$T_J$	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

**Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions** *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(4), (5)	2.375 (2.375)	2.625 (2.625)	V
$V_I$	Input voltage	(3), (6)	−0.5	5.75	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Junction temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)** *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (9)		5.75	V
$V_{IL}$	Low-level input voltage		−0.5		$0.8, 0.3 \times V_{CCIO}$ (9)	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (10)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (10)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (10)	1.7			V

**Table 28. APEX 20KE Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
$V_{CCIO}$	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	(3), (4)	1.71 (1.71)	1.89 (1.89)	V
$V_I$	Input voltage	(5), (6)	−0.5	4.0	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_J$	Junction temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 29. APEX 20KE Device DC Operating Conditions** *Notes (7), (8), (9)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level LVTTTL, CMOS, or 3.3-V PCI input voltage		1.7, $0.5 \times V_{CCIO}$ (10)		4.1	V
$V_{IL}$	Low-level LVTTTL, CMOS, or 3.3-V PCI input voltage		-0.5		$0.8, 0.3 \times V_{CCIO}$ (10)	V
$V_{OH}$	3.3-V high-level LVTTTL output voltage	$I_{OH} = -12$ mA DC, $V_{CCIO} = 3.00$ V (11)	2.4			V
	3.3-V high-level LVCMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (11)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (11)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (11)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (11)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (11)	1.7			V
$V_{OL}$	3.3-V low-level LVTTTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (12)			0.4	V
	3.3-V low-level LVCMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (12)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (12)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (12)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (12)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (12)			0.7	V
$I_I$	Input pin leakage current	$V_I = 4.1$ to $-0.5$ V (13)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = 4.1$ to $-0.5$ V (13)	-10		10	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby) (All ESBs in power-down mode)	$V_I =$ ground, no load, no toggling inputs, -1 speed grade		10		mA
		$V_I =$ ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
$R_{CONF}$	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (14)	20		50	k $\Omega$
		$V_{CCIO} = 2.375$ V (14)	30		80	k $\Omega$
		$V_{CCIO} = 1.71$ V (14)	60		150	k $\Omega$



For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

**Table 30. APEX 20KE Device Capacitance** Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 27 through 30:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than  $100\text{ mA}$ . The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to  $100\%$  duty cycle.

$V_{in}$	Max. Duty Cycle
$4.0\text{ V}$	$100\%$ (DC)
$4.1$	$90\%$
$4.2$	$50\%$
$4.3$	$30\%$
$4.4$	$17\%$
$4.5$	$10\%$
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 1.8\text{ V}$ , and  $V_{CCIO} = 1.8\text{ V}$ ,  $2.5\text{ V}$  or  $3.3\text{ V}$ .
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ , and  $I_I$  parameters when  $V_{CCIO} = 1.8\text{ V}$ .
- (10) The APEX 20KE input buffers are compatible with  $1.8\text{-V}$ ,  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVCMOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for  $3.3\text{-V}$  PCI compliance on APEX 20K devices.

Figure 33. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

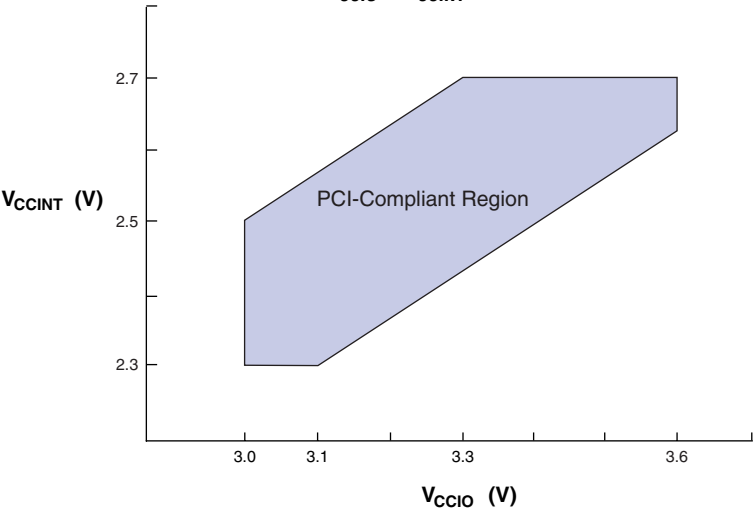
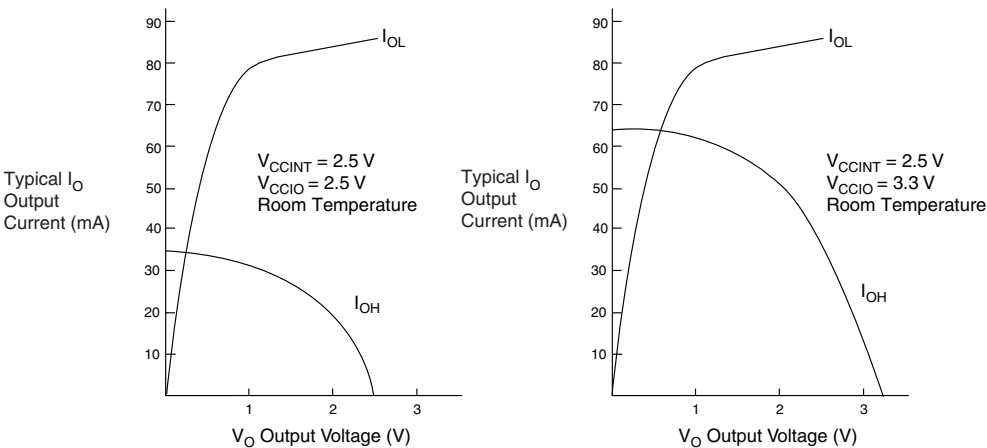


Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when  $V_{CCIO}$  pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

Figure 34. Output Drive Characteristics of APEX 20K Device *Note (1)*



Note to Figure 34:

(1) These are transient (AC) currents.

Tables 40 through 42 show the  $f_{\text{MAX}}$  timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

**Table 40. EP20K100  $f_{\text{MAX}}$  Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Units
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.5		0.6		0.8		ns
$t_{\text{H}}$	0.7		0.8		1.0		ns
$t_{\text{CO}}$		0.3		0.4		0.5	ns
$t_{\text{LUT}}$		0.8		1.0		1.3	ns
$t_{\text{ESBRC}}$		1.7		2.1		2.4	ns
$t_{\text{ESBWC}}$		5.7		6.9		8.1	ns
$t_{\text{ESBWESU}}$	3.3		3.9		4.6		ns
$t_{\text{ESBDATASU}}$	2.2		2.7		3.1		ns
$t_{\text{ESBDATAH}}$	0.6		0.8		0.9		ns
$t_{\text{ESBADDRSU}}$	2.4		2.9		3.3		ns
$t_{\text{ESBDATACO1}}$		1.3		1.6		1.8	ns
$t_{\text{ESBDATACO2}}$		2.6		3.1		3.6	ns
$t_{\text{ESBDD}}$		2.5		3.3		3.6	ns
$t_{\text{PD}}$		2.5		3.0		3.6	ns
$t_{\text{PTERMSU}}$	2.3		2.6		3.2		ns
$t_{\text{PTERMCO}}$		1.5		1.8		2.1	ns
$t_{\text{F1-4}}$		0.5		0.6		0.7	ns
$t_{\text{F5-20}}$		1.6		1.7		1.8	ns
$t_{\text{F20+}}$		2.2		2.2		2.3	ns
$t_{\text{CH}}$	2.0		2.5		3.0		ns
$t_{\text{CL}}$	2.0		2.5		3.0		ns
$t_{\text{CLRP}}$	0.3		0.4		0.4		ns
$t_{\text{PREP}}$	0.5		0.5		0.5		ns
$t_{\text{ESBCH}}$	2.0		2.5		3.0		ns
$t_{\text{ESBCL}}$	2.0		2.5		3.0		ns
$t_{\text{ESBWP}}$	1.6		1.9		2.2		ns
$t_{\text{ESBRP}}$	1.0		1.3		1.4		ns

**Table 56. EP20K60E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.83		2.57		3.79	ns
$t_{ESBSRC}$		2.46		3.26		4.61	ns
$t_{ESBAWC}$		3.50		4.90		7.23	ns
$t_{ESBSWC}$		3.77		4.90		6.79	ns
$t_{ESBWASU}$	1.59		2.23		3.29		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.75		2.46		3.62		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.76		2.47		3.64		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.68		2.49		3.87		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.08		0.43		1.04		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.29		0.72		1.46		ns
$t_{ESBRADDRSU}$	0.36		0.81		1.58		ns
$t_{ESBDATACO1}$		1.06		1.24		1.55	ns
$t_{ESBDATACO2}$		2.39		3.35		4.94	ns
$t_{ESBDD}$		3.50		4.90		7.23	ns
$t_{PD}$		1.72		2.41		3.56	ns
$t_{PTERMSU}$	0.99		1.56		2.55		ns
$t_{PTERMCO}$		1.07		1.26		1.08	ns

**Table 99. EP20K1000E  $t_{MAX}$  Routing Delays**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.27		0.27		0.27	ns
$t_{F5-20}$		1.45		1.63		1.75	ns
$t_{F20+}$		4.15		4.33		4.97	ns

**Table 100. EP20K1000E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	1.25		1.43		1.67		ns
$t_{CL}$	1.25		1.43		1.67		ns
$t_{CLRP}$	0.20		0.20		0.20		ns
$t_{PREP}$	0.20		0.20		0.20		ns
$t_{ESBCH}$	1.25		1.43		1.67		ns
$t_{ESBCL}$	1.25		1.43		1.67		ns
$t_{ESBWP}$	1.28		1.51		1.65		ns
$t_{ESBRP}$	1.11		1.29		1.41		ns

**Table 101. EP20K1000E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.70		2.84		2.97		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	5.75	2.00	6.33	2.00	6.90	ns
$t_{INSUPLL}$	1.64		2.09		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.99	-	-	ns

**Table 106. EP20K1500E Minimum Pulse Width Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.25		1.43		1.67		ns
t <sub>CL</sub>	1.25		1.43		1.67		ns
t <sub>CLRP</sub>	0.20		0.20		0.20		ns
t <sub>PREP</sub>	0.20		0.20		0.20		ns
t <sub>ESBCH</sub>	1.25		1.43		1.67		ns
t <sub>ESBCL</sub>	1.25		1.43		1.67		ns
t <sub>ESBWP</sub>	1.28		1.51		1.65		ns
t <sub>ESBRP</sub>	1.11		1.29		1.41		ns

**Table 107. EP20K1500E External Timing Parameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	3.09		3.30		3.58		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	6.18	2.00	6.81	2.00	7.36	ns
t <sub>INSUPLL</sub>	1.94		2.08		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.67	0.50	2.99	-	-	ns

## Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

### Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

### Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for  $t_{ESB\text{DATAH}}$  parameter.

### Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

### Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$  added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).



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