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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	376
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep20k200efc484-1">https://www.e-xfl.com/product-detail/intel/ep20k200efc484-1</a>

**Table 2. Additional APEX 20K Device Features** *Note (1)*

Feature	EP20K300E	EP20K400	EP20K400E	EP20K600E	EP20K1000E	EP20K1500E
Maximum system gates	728,000	1,052,000	1,052,000	1,537,000	1,772,000	2,392,000
Typical gates	300,000	400,000	400,000	600,000	1,000,000	1,500,000
LEs	11,520	16,640	16,640	24,320	38,400	51,840
ESBs	72	104	104	152	160	216
Maximum RAM bits	147,456	212,992	212,992	311,296	327,680	442,368
Maximum macrocells	1,152	1,664	1,664	2,432	2,560	3,456
Maximum user I/O pins	408	502	488	588	708	808

*Note to Tables 1 and 2:*

- (1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

**Table 3. APEX 20K Supply Voltages**

Feature	Device	
	EP20K100 EP20K200 EP20K400	EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E EP20K300E EP20K400E EP20K600E EP20K1000E EP20K1500E
Internal supply voltage ( $V_{CCINT}$ )	2.5 V	1.8 V
MultiVolt I/O interface voltage levels ( $V_{CCIO}$ )	2.5 V, 3.3 V, 5.0 V	1.8 V, 2.5 V, 3.3 V, 5.0 V (1)

*Note to Table 3:*

- (1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

## Functional Description

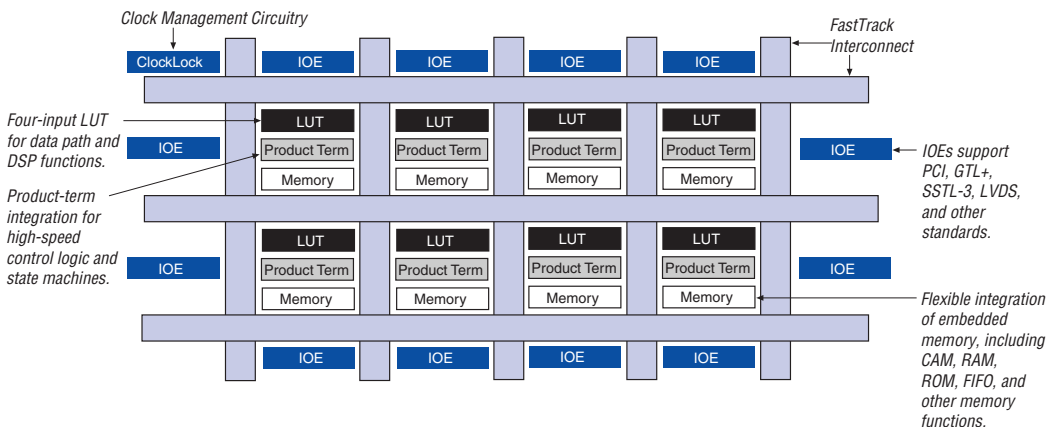
APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack<sup>®</sup> Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

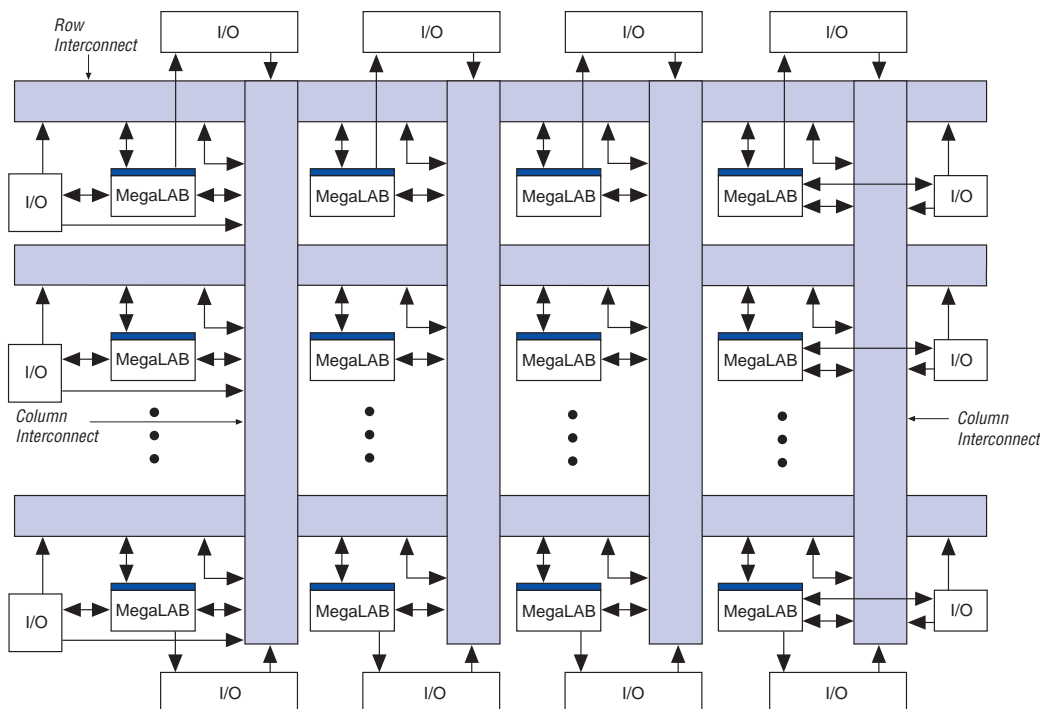
The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX 20K device.

**Figure 1. APEX 20K Device Block Diagram**





**Figure 9. APEX 20K Interconnect Structure**

A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

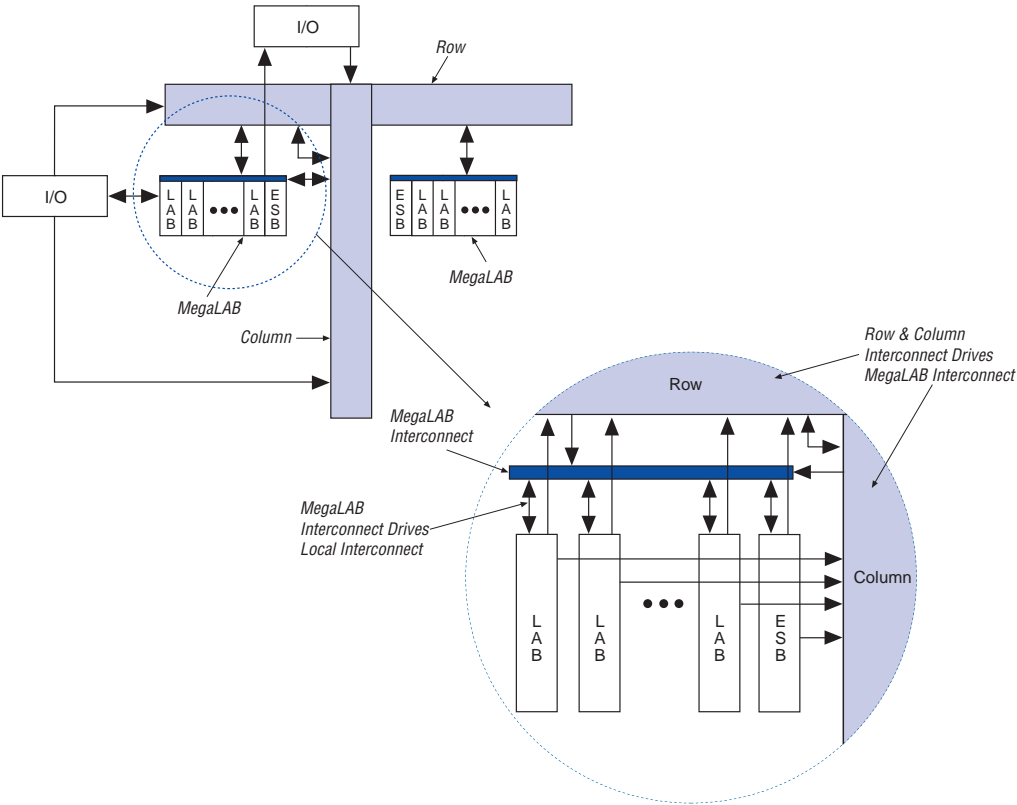


Figure 12. APEX 20KE FastRow Interconnect

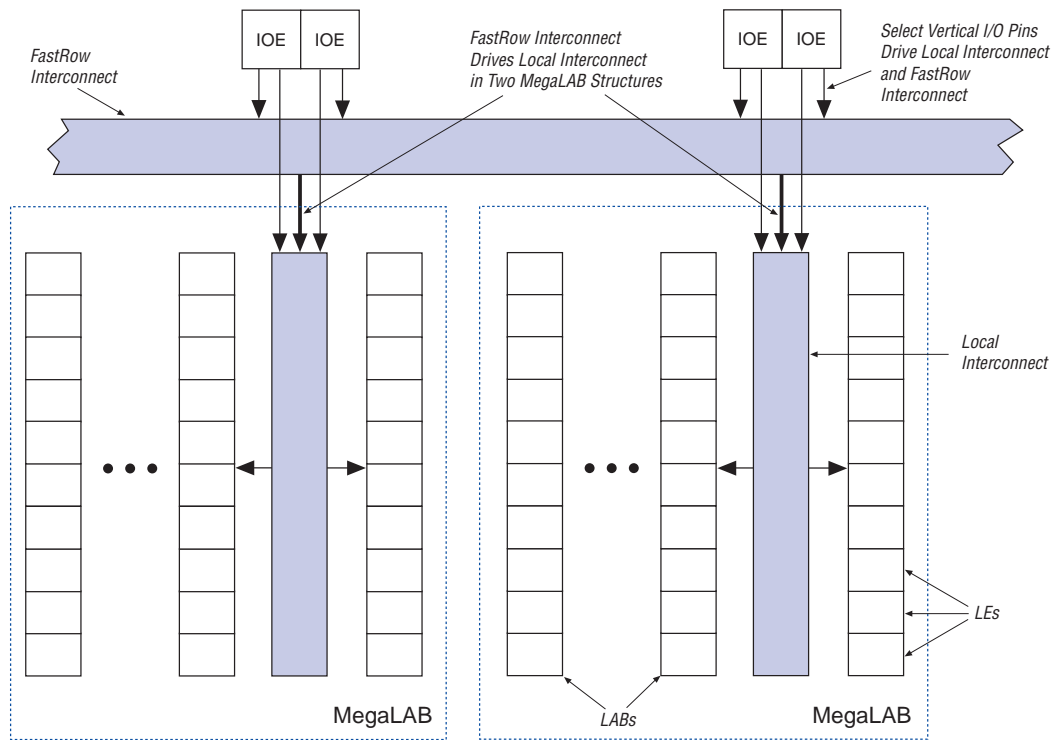


Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes:  $128 \times 16$ ,  $256 \times 8$ ,  $512 \times 4$ ,  $1,024 \times 2$ , or  $2,048 \times 1$ . By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two  $128 \times 16$  RAM blocks can be combined to form a  $128 \times 32$  RAM block, and two  $512 \times 4$  RAM blocks can be combined to form a  $512 \times 8$  RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See [Figure 18](#).



**Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
$f_{VCO}$ (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
$f_{CLOCK0}$	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
$f_{CLOCK1}$	clock1 PLL output frequency for internal use		20	335	20	200	MHz
$f_{CLOCK0\_EXT}$	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
$f_{CLOCK1\_EXT}$	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

**Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)** Notes (2), (7), (8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 12 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (11)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ V}$ (11)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5 \text{ mA DC}$ , $V_{CCIO} = 3.00 \text{ to } 3.60 \text{ V}$ (11)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (11)			0.2	V
		$I_{OL} = 1 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (11)			0.4	V
		$I_{OL} = 2 \text{ mA DC}$ , $V_{CCIO} = 2.30 \text{ V}$ (11)			0.7	V
$I_I$	Input pin leakage current	$V_I = 5.75 \text{ to } -0.5 \text{ V}$	-10		10	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = 5.75 \text{ to } -0.5 \text{ V}$	-10		10	$\mu\text{A}$
$I_{CC0}$	$V_{CC}$ supply current (standby) (All ESBs in power-down mode)	$V_I = \text{ground}$ , no load, no toggling inputs, -1 speed grade (12)		10		mA
		$V_I = \text{ground}$ , no load, no toggling inputs, -2, -3 speed grades (12)		5		mA
$R_{CONF}$	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0 \text{ V}$ (13)	20		50	W
		$V_{CCIO} = 2.375 \text{ V}$ (13)	30		80	W



For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

**Table 30. APEX 20KE Device Capacitance** Note (15)

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		8	pF

**Notes to Tables 27 through 30:**

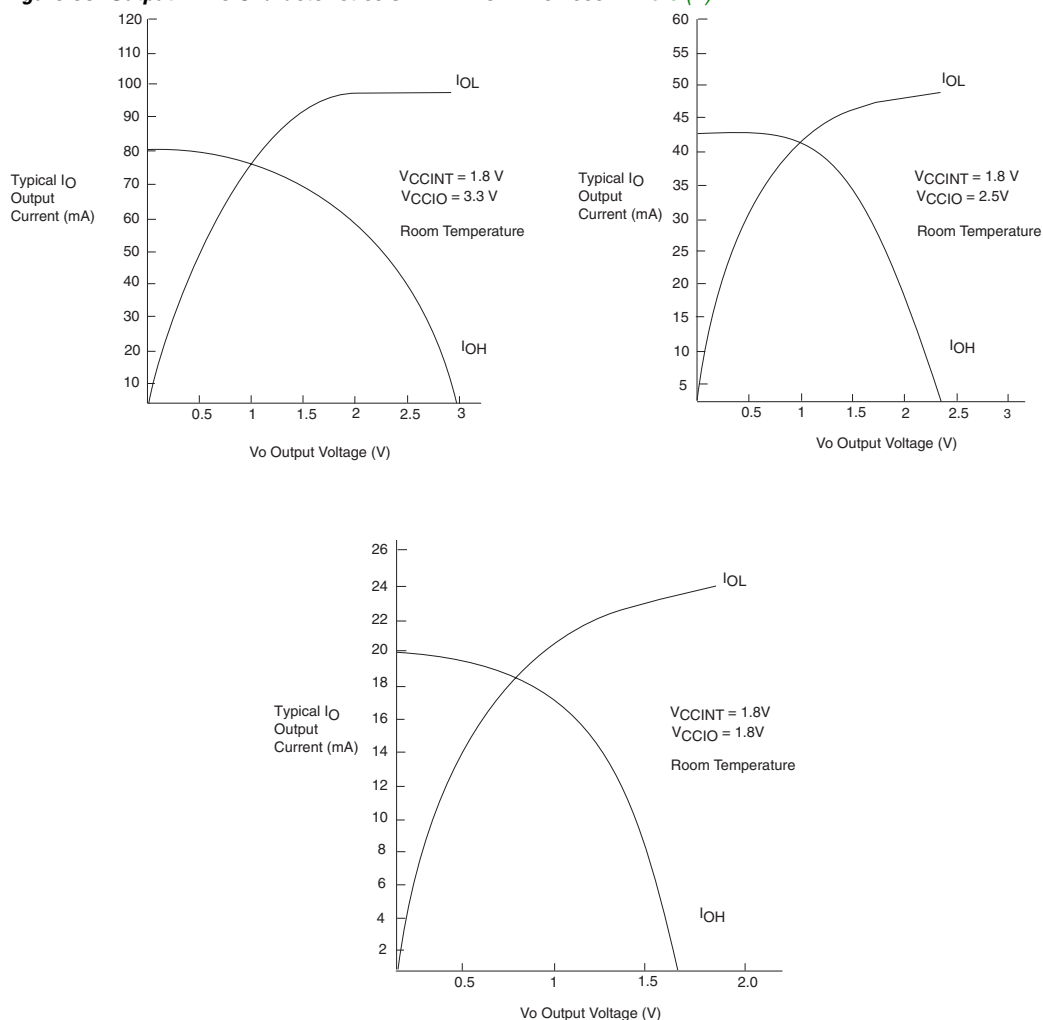
- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $5.75\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than  $100\text{ mA}$ . The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to  $100\%$  duty cycle.

$V_{IN}$	Max. Duty Cycle
$4.0\text{ V}$	$100\%$ (DC)
$4.1$	$90\%$
$4.2$	$50\%$
$4.3$	$30\%$
$4.4$	$17\%$
$4.5$	$10\%$
- (6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (7) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 1.8\text{ V}$ , and  $V_{CCIO} = 1.8\text{ V}$ ,  $2.5\text{ V}$  or  $3.3\text{ V}$ .
- (8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
- (9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the  $V_{IH}$ ,  $V_{IL}$ ,  $V_{OH}$ ,  $V_{OL}$ , and  $I_I$  parameters when  $V_{CCIO} = 1.8\text{ V}$ .
- (10) The APEX 20KE input buffers are compatible with  $1.8\text{-V}$ ,  $2.5\text{-V}$  and  $3.3\text{-V}$  (LVTTTL and LVCMOS) signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
- (11) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (12) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (13) This value is specified for normal device operation. The value may vary during power-up.
- (14) Pin pull-up resistance values will be lower if an external source drives the pin higher than  $V_{CCIO}$ .
- (15) Capacitance is sample-tested only.

Figure 33 shows the relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for  $3.3\text{-V}$  PCI compliance on APEX 20K devices.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

**Figure 35. Output Drive Characteristics of APEX 20KE Devices** *Note (1)*



**Note to Figure 35:**

(1) These are transient (AC) currents.

## Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the  $f_{MAX}$  timing model for APEX 20K devices.

**Figure 36. APEX 20K  $t_{MAX}$  Timing Model**

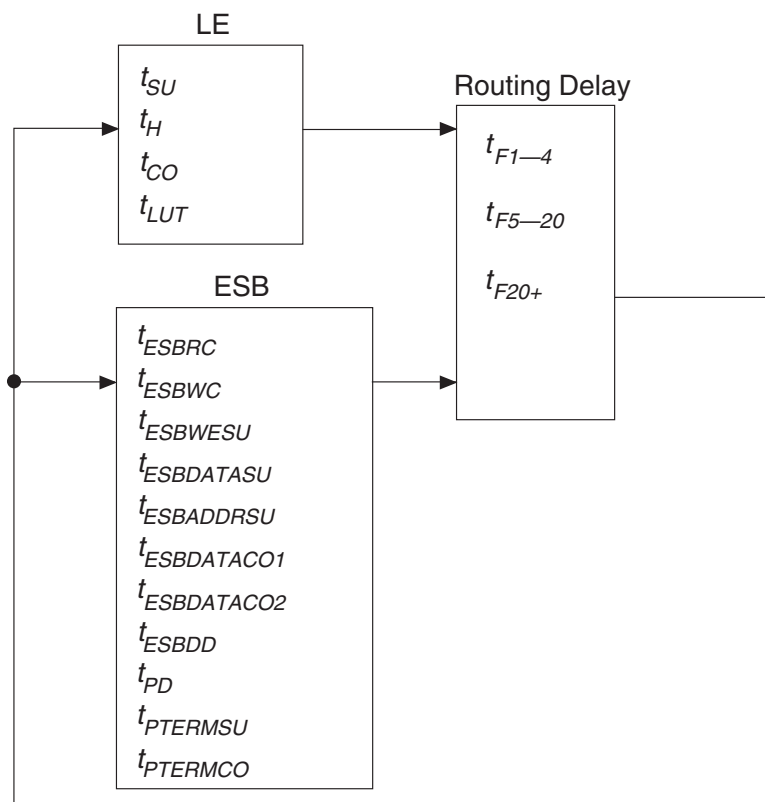


Figure 37 shows the  $f_{MAX}$  timing model for APEX 20KE devices. These parameters can be used to estimate  $f_{MAX}$  for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

Note to [Tables 32 and 33](#):

(1) These timing parameters are sample-tested only.

[Tables 34 through 37](#) show APEX 20KE LE, ESB, routing, and functional timing microparameters for the  $f_{MAX}$  timing model.

**Table 34. APEX 20KE LE Timing Microparameters**

Symbol	Parameter
$t_{SU}$	LE register setup time before clock
$t_H$	LE register hold time after clock
$t_{CO}$	LE register clock-to-output delay
$t_{LUT}$	LUT delay for data-in to data-out

**Table 35. APEX 20KE ESB Timing Microparameters**

Symbol	Parameter
$t_{ESBARC}$	ESB Asynchronous read cycle time
$t_{ESBSRC}$	ESB Synchronous read cycle time
$t_{ESBAWC}$	ESB Asynchronous write cycle time
$t_{ESBSWC}$	ESB Synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
$t_{ESBWAH}$	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
$t_{ESBWdH}$	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
$t_{ESBRAH}$	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBWEH}$	ESB WE hold time after clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBDATAH}$	ESB data hold time after clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
$t_{ESBDD}$	ESB data-in to data-out delay for RAM mode
$t_{PD}$	ESB Macrocell input to non-registered output
$t_{PTERMSU}$	ESB Macrocell register setup time before clock
$t_{PTERMCO}$	ESB Macrocell register clock-to-output delay

Notes to **Tables 43 through 48**:

- (1) This parameter is measured without using ClockLock or ClockBoost circuits.
- (2) This parameter is measured using ClockLock or ClockBoost circuits.

**Tables 49 through 54** describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K30E APEX 20KE devices.

<b>Table 49. EP20K30E <math>f_{MAX}</math> LE Timing Microparameters</b>							
<b>Symbol</b>	<b>-1</b>		<b>-2</b>		<b>-3</b>		<b>Unit</b>
	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
$t_{SU}$	0.01		0.02		0.02		ns
$t_H$	0.11		0.16		0.23		ns
$t_{CO}$		0.32		0.45		0.67	ns
$t_{LUT}$		0.85		1.20		1.77	ns

**Table 56. EP20K60E  $t_{MAX}$  ESB Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{ESBARC}$		1.83		2.57		3.79	ns
$t_{ESBSRC}$		2.46		3.26		4.61	ns
$t_{ESBAWC}$		3.50		4.90		7.23	ns
$t_{ESBSWC}$		3.77		4.90		6.79	ns
$t_{ESBWASU}$	1.59		2.23		3.29		ns
$t_{ESBWAH}$	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.75		2.46		3.62		ns
$t_{ESBWDH}$	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.76		2.47		3.64		ns
$t_{ESBRAH}$	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.68		2.49		3.87		ns
$t_{ESBWEH}$	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.08		0.43		1.04		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.29		0.72		1.46		ns
$t_{ESBRADDRSU}$	0.36		0.81		1.58		ns
$t_{ESBDATACO1}$		1.06		1.24		1.55	ns
$t_{ESBDATACO2}$		2.39		3.35		4.94	ns
$t_{ESBDD}$		3.50		4.90		7.23	ns
$t_{PD}$		1.72		2.41		3.56	ns
$t_{PTERMSU}$	0.99		1.56		2.55		ns
$t_{PTERMCO}$		1.07		1.26		1.08	ns



**Table 57. EP20K60E  $t_{MAX}$  Routing Delays**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{F1-4}$		0.24		0.26		0.30	ns
$t_{F5-20}$		1.45		1.58		1.79	ns
$t_{F20+}$		1.96		2.14		2.45	ns

**Table 58. EP20K60E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CH}$	2.00		2.50		2.75		ns
$t_{CL}$	2.00		2.50		2.75		ns
$t_{CLRP}$	0.20		0.28		0.41		ns
$t_{PREP}$	0.20		0.28		0.41		ns
$t_{ESBCH}$	2.00		2.50		2.75		ns
$t_{ESBCL}$	2.00		2.50		2.75		ns
$t_{ESBWP}$	1.29		1.80		2.66		ns
$t_{ESBRP}$	1.04		1.45		2.14		ns

**Table 59. EP20K60E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSU}$	2.03		2.12		2.23		ns
$t_{INH}$	0.00		0.00		0.00		ns
$t_{OUTCO}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
$t_{INSUPLL}$	1.12		1.15		-		ns
$t_{INHPLL}$	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	3.37	0.50	3.69	-	-	ns

**Table 78. EP20K200E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.81		3.19		3.54		ns
$t_{\text{INHBIDIR}}$	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{\text{XZBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{ZXBIDIR}}$		7.51		8.32		8.67	ns
$t_{\text{INSUBIDIRPLL}}$	3.30		3.64		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.40		6.05		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.40		6.05		-	ns

Tables 79 through 84 describe  $f_{\text{MAX}}$  LE Timing Microparameters,  $f_{\text{MAX}}$  ESB Timing Microparameters,  $f_{\text{MAX}}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

**Table 79. EP20K300E  $f_{\text{MAX}}$  LE Timing Microparameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{SU}}$	0.16		0.17		0.18		ns
$t_{\text{H}}$	0.31		0.33		0.38		ns
$t_{\text{CO}}$		0.28		0.38		0.51	ns
$t_{\text{LUT}}$		0.79		1.07		1.43	ns

**Table 82. EP20K300E Minimum Pulse Width Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>CH</sub>	1.25		1.43		1.67		ns
t <sub>CL</sub>	1.25		1.43		1.67		ns
t <sub>CLRP</sub>	0.19		0.26		0.35		ns
t <sub>PREP</sub>	0.19		0.26		0.35		ns
t <sub>ESBCH</sub>	1.25		1.43		1.67		ns
t <sub>ESBCL</sub>	1.25		1.43		1.67		ns
t <sub>ESBWP</sub>	1.25		1.71		2.28		ns
t <sub>ESBRP</sub>	1.01		1.38		1.84		ns

**Table 83. EP20K300E External Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSU</sub>	2.31		2.44		2.57		ns
t <sub>INH</sub>	0.00		0.00		0.00		ns
t <sub>OUTCO</sub>	2.00	5.29	2.00	5.82	2.00	6.24	ns
t <sub>INSUPLL</sub>	1.76		1.85		-		ns
t <sub>INHPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOPLL</sub>	0.50	2.65	0.50	2.95	-	-	ns

**Table 84. EP20K300E External Bidirectional Timing Parameters**

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t <sub>INSUBIDIR</sub>	2.77		2.85		3.11		ns
t <sub>INHBIDIR</sub>	0.00		0.00		0.00		ns
t <sub>OUTCOBIDIR</sub>	2.00	5.29	2.00	5.82	2.00	6.24	ns
t <sub>XZBIDIR</sub>		7.59		8.30		9.09	ns
t <sub>ZXBIDIR</sub>		7.59		8.30		9.09	ns
t <sub>INSUBIDIRPLL</sub>	2.50		2.76		-		ns
t <sub>INHBIDIRPLL</sub>	0.00		0.00		-		ns
t <sub>OUTCOBIDIRPLL</sub>	0.50	2.65	0.50	2.95	-	-	ns
t <sub>XZBIDIRPLL</sub>		5.00		5.43		-	ns
t <sub>ZXBIDIRPLL</sub>		5.00		5.43		-	ns

Tables 97 through 102 describe  $f_{MAX}$  LE Timing Microparameters,  $f_{MAX}$  ESB Timing Microparameters,  $f_{MAX}$  Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

**Table 97. EP20K1000E  $f_{MAX}$  LE Timing Microparameters**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{SU}$	0.25		0.25		0.25		ns
$t_H$	0.25		0.25		0.25		ns
$t_{CO}$		0.28		0.32		0.33	ns
$t_{LUT}$		0.80		0.95		1.13	ns



101 Innovation Drive  
San Jose, CA 95134  
(408) 544-7000  
<http://www.altera.com>  
**Applications Hotline:**  
(800) 800-EPLD  
**Customer Marketing:**  
(408) 544-7104  
**Literature Services:**  
[lit\\_req@altera.com](mailto:lit_req@altera.com)

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