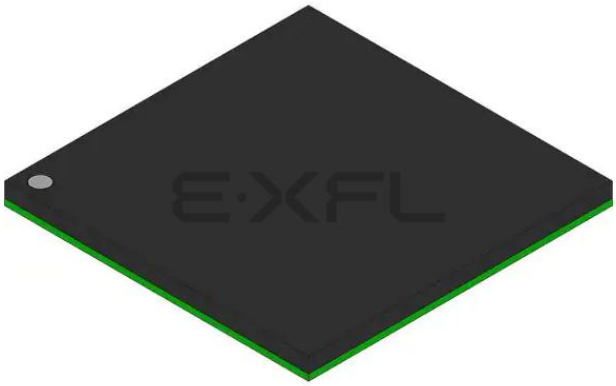


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	376
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep20k200efc484-2

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

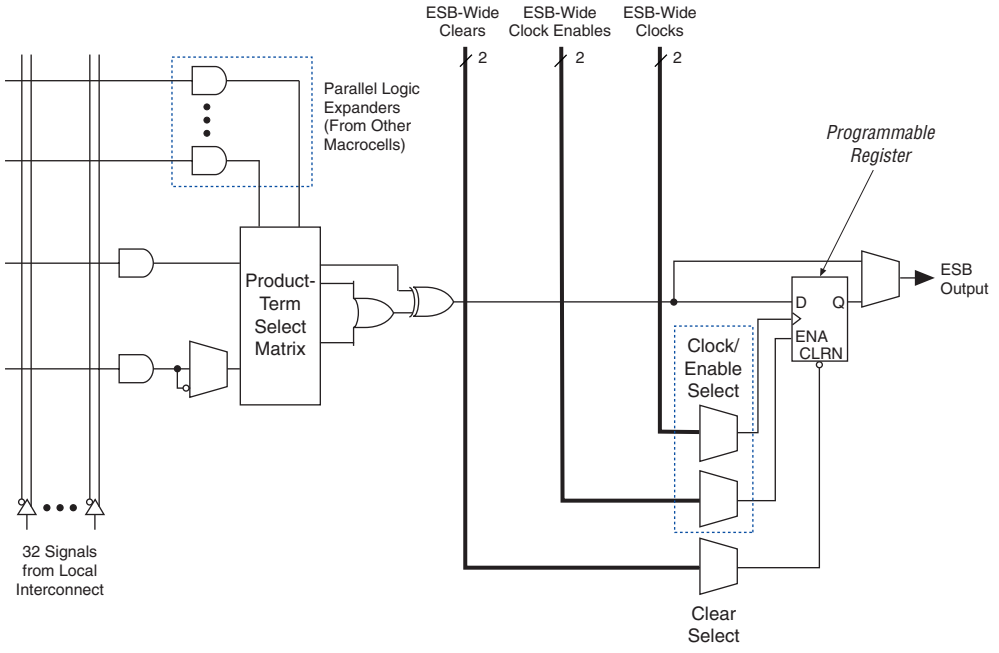
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 14. APEX 20K Macrocell



For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 14. Multiplication Factor Combinations

Clock 1	Clock 2
×1	×1
×1, ×2	×2
×1, ×2, ×4	×4

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where m and k range from 2 to 160, and n and v range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Clock Phase & Delay Adjustment

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

LVDS Support

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

Lock Signals

The APEX 20KE ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{SKEW}	Skew delay between related ClockLock/ClockBoost-generated clocks		500	ps
t_{JITTER}	Jitter on ClockLock/ClockBoost-generated clock *(5)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Notes to Table 15:

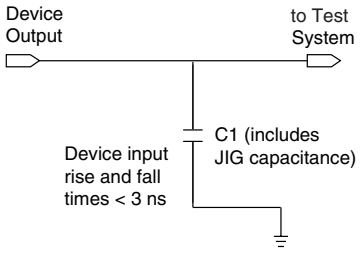
(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, t_{JITTER} is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{OUT}	Output frequency	25	170	MHz
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)	25	170	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)	16	80	MHz
f_{CLK4}	Input clock frequency (ClockBoost clock multiplication factor equals 4)	10	34	MHz
$t_{OUTDUTY}$	Duty cycle for ClockLock/ClockBoost-generated clock	40	60	%
f_{CLKDEV}	Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)*		25,000 *(2)*	PPM
t_R	Input rise time		5	ns
t_F	Input fall time		5	ns
t_{LOCK}	Time required for ClockLock/ ClockBoost to acquire lock *(3)*		10	µs
t_{SKEW}	Skew delay between related ClockLock/ ClockBoost-generated clock	500	500	ps
t_{JITTER}	Jitter on ClockLock/ ClockBoost-generated clock *(4)*		200	ps
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)		50	ps

Figure 32. APEX 20K AC Test Conditions *Note (1)*



Note to Figure 32:

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4), (5)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4), (5)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(4), (5)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(3), (6)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2) *Notes (2), (7), (8)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		1.7, 0.5 × V_{CCIO} *(9)*		5.75	V
V_{IL}	Low-level input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(9)*	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(10)*	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(10)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(10)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(10)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(10)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(10)*	1.7			V

Table 28. APEX 20KE Device Recommended Operating Conditions

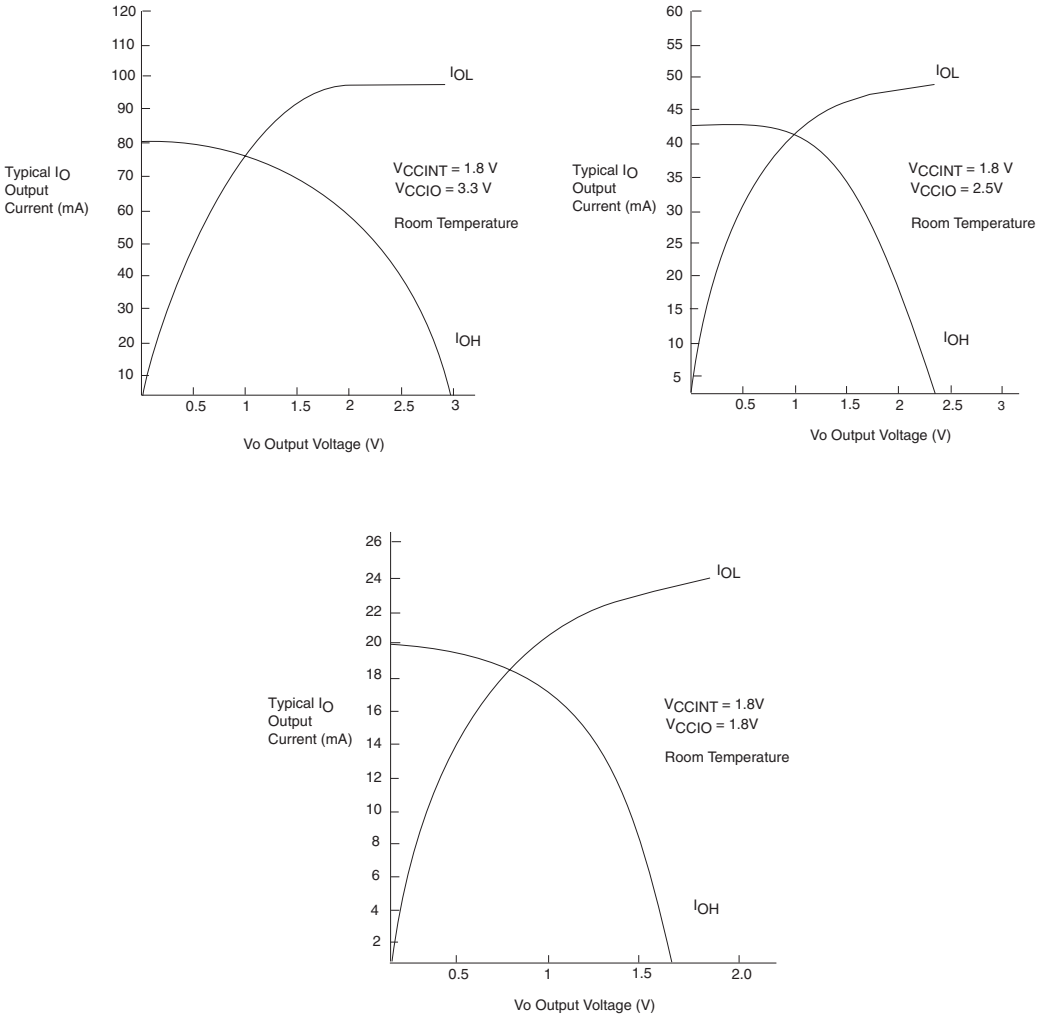
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
	Supply voltage for output buffers, 1.8-V operation	*(3)*, *(4)*	1.71 (1.71)	1.89 (1.89)	V
V_I	Input voltage	*(5)*, *(6)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 29. APEX 20KE Device DC Operating Conditions *Notes (7), (8), (9)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTL, CMOS, or 3.3-V PCI input voltage		1.7, 0.5 × V_{CCIO} *(10)*		4.1	V
V_{IL}	Low-level LVTTL, CMOS, or 3.3-V PCI input voltage		–0.5		0.8, 0.3 × V_{CCIO} *(10)*	V
V_{OH}	3.3-V high-level LVTTL output voltage	I_{OH} = –12 mA DC, V_{CCIO} = 3.00 V *(11)*	2.4			V
	3.3-V high-level LVCMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(11)*	V_{CCIO} – 0.2			V
	3.3-V high-level PCI output voltage	I_{OH} = –0.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(11)*	0.9 × V_{CCIO}			V
	2.5-V high-level output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 2.30 V *(11)*	2.1			V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(11)*	2.0			V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(11)*	1.7			V
V_{OL}	3.3-V low-level LVTTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(12)*			0.4	V
	3.3-V low-level LVCMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(12)*			0.2	V
	3.3-V low-level PCI output voltage	I_{OL} = 1.5 mA DC, V_{CCIO} = 3.00 to 3.60 V *(12)*			0.1 × V_{CCIO}	V
	2.5-V low-level output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 2.30 V *(12)*			0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(12)*			0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(12)*			0.7	V
I_I	Input pin leakage current	V_I = 4.1 to –0.5 V *(13)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	V_O = 4.1 to –0.5 V *(13)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -1 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(14)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(14)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(14)*	60		150	kΩ

Figure 35 shows the output drive characteristics of APEX 20KE devices.

Figure 35. Output Drive Characteristics of APEX 20KE Devices *Note (1)*



Note to Figure 35:
(1) These are transient (AC) currents.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Table 50. EP20K30E f_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.03		2.86		4.24	ns
t_{ESBSRC}		2.58		3.49		5.02	ns
t_{ESBAWC}		3.88		5.45		8.08	ns
t_{ESBSWC}		4.08		5.35		7.48	ns
$t_{ESBWASU}$	1.77		2.49		3.68		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.95		2.74		4.05		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.96		2.75		4.07		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.80		2.73		4.28		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.07		0.48		1.17		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.30		0.80		1.64		ns
$t_{ESBRADDRSU}$	0.37		0.90		1.78		ns
$t_{ESBDATACO1}$		1.11		1.32		1.67	ns
$t_{ESBDATACO2}$		2.65		3.73		5.53	ns
t_{ESBDD}		3.88		5.45		8.08	ns
t_{PD}		1.91		2.69		3.98	ns
$t_{PTERMSU}$	1.04		1.71		2.82		ns
$t_{PTERMCO}$		1.13		1.34		1.69	ns

Table 51. EP20K30E f_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.31	ns
t_{F5-20}		1.03		1.14		1.30	ns
t_{F20+}		1.42		1.54		1.77	ns

Table 52. EP20K30E Minimum Pulse Width Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	0.55		0.78		1.15		ns
t_{CL}	0.55		0.78		1.15		ns
t_{CLRP}	0.22		0.31		0.46		ns
t_{PREP}	0.22		0.31		0.46		ns
t_{ESBCH}	0.55		0.78		1.15		ns
t_{ESBCL}	0.55		0.78		1.15		ns
t_{ESBWP}	1.43		2.01		2.97		ns
t_{ESBRP}	1.15		1.62		2.39		ns

Table 53. EP20K30E External Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.02		2.13		2.24		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{INSUPLL}$	2.11		2.23		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.88	-	-	ns

Table 54. EP20K30E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	1.85		1.77		1.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	4.88	2.00	5.36	2.00	5.88	ns
$t_{XZBIDIR}$		7.48		8.46		9.83	ns
$t_{ZXBIDIR}$		7.48		8.46		9.83	ns
$t_{INSUBIDIRPLL}$	4.12		4.24		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	2.60	0.50	2.88	-	-	ns
$t_{XZBIDIRPLL}$		5.21		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.21		5.99		-	ns

Tables 55 through 60 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

Table 55. EP20K60E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.17		0.15		0.16		ns
t_{H}	0.32		0.33		0.39		ns
t_{CO}		0.29		0.40		0.60	ns
t_{LUT}		0.77		1.07		1.59	ns

Table 72. EP20K160E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.86		3.24		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.07	2.00	5.59	2.00	6.13	ns
$t_{XZBIDIR}$		7.43		8.23		8.58	ns
$t_{ZXBIDIR}$		7.43		8.23		8.58	ns
$t_{INSUBIDIRPLL}$	4.93		5.48		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.00	0.50	3.35	-	-	ns
$t_{XZBIDIRPLL}$		5.36		5.99		-	ns
$t_{ZXBIDIRPLL}$		5.36		5.99		-	ns

Tables 73 through 78 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

Table 73. EP20K200E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.23		0.24		0.26		ns
t_{H}	0.23		0.24		0.26		ns
t_{CO}		0.26		0.31		0.36	ns
t_{LUT}		0.70		0.90		1.14	ns

Table 78. EP20K200E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	2.81		3.19		3.54		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	5.12	2.00	5.62	2.00	6.11	ns
$t_{XZBIDIR}$		7.51		8.32		8.67	ns
$t_{ZXBIDIR}$		7.51		8.32		8.67	ns
$t_{INSUBIDIRPLL}$	3.30		3.64		-		ns
$t_{INHBIDIRPLL}$	0.00		0.00		-		ns
$t_{OUTCOBIDIRPLL}$	0.50	3.01	0.50	3.36	-	-	ns
$t_{XZBIDIRPLL}$		5.40		6.05		-	ns
$t_{ZXBIDIRPLL}$		5.40		6.05		-	ns

Tables 79 through 84 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

Table 79. EP20K300E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.16		0.17		0.18		ns
t_{H}	0.31		0.33		0.38		ns
t_{CO}		0.28		0.38		0.51	ns
t_{LUT}		0.79		1.07		1.43	ns

Table 104. EP20K1500E f_{MAX} ESB Timing Microparameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.78		2.02		1.95	ns
t_{ESBSRC}		2.52		2.91		3.14	ns
t_{ESBAWC}		3.52		4.11		4.40	ns
t_{ESBSWC}		3.23		3.84		4.16	ns
$t_{ESBWASU}$	0.62		0.67		0.61		ns
t_{ESBWAH}	0.41		0.55		0.55		ns
$t_{ESBWDSU}$	0.77		0.79		0.81		ns
t_{ESBWDH}	0.41		0.55		0.55		ns
$t_{ESBRASU}$	1.74		1.92		1.85		ns
t_{ESBRAH}	0.00		0.01		0.23		ns
$t_{ESBWESU}$	2.07		2.28		2.41		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	0.25		0.27		0.29		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.11		0.04		0.11		ns
$t_{ESBRADDRSU}$	0.14		0.11		0.16		ns
$t_{ESBDATACO1}$		1.29		1.50		1.63	ns
$t_{ESBDATACO2}$		2.55		2.99		3.22	ns
t_{ESBDD}		3.12		3.57		3.85	ns
t_{PD}		1.84		2.13		2.32	ns
$t_{PTERMSU}$	1.08		1.19		1.32		ns
$t_{PTERMCO}$		1.31		1.53		1.66	ns

Table 105. EP20K1500E f_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.28		0.28		0.28	ns
t_{F5-20}		1.36		1.50		1.62	ns
t_{F20+}		4.43		4.48		5.07	ns

Table 106. EP20K1500E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.25		1.43		1.67		ns
t_{CL}	1.25		1.43		1.67		ns
t_{CLRP}	0.20		0.20		0.20		ns
t_{PREP}	0.20		0.20		0.20		ns
t_{ESBCH}	1.25		1.43		1.67		ns
t_{ESBCL}	1.25		1.43		1.67		ns
t_{ESBWP}	1.28		1.51		1.65		ns
t_{ESBRP}	1.11		1.29		1.41		ns

Table 107. EP20K1500E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.09		3.30		3.58		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{INSUPLL}$	1.94		2.08		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.67	0.50	2.99	-	-	ns

Table 108. EP20K1500E External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.47		3.68		3.99		ns
$t_{INHBIDIR}$	0.00		0.00		0.00		ns
$t_{OUTCOBIDIR}$	2.00	6.18	2.00	6.81	2.00	7.36	ns
$t_{XZBIDIR}$		6.91		7.62		8.38	ns
$t_{ZXBIDIR}$		6.91		7.62		8.38	ns
$t_{INSUBIDIRPLL}$	3.05		3.26				ns
$t_{INHBIDIRPLL}$	0.00		0.00				ns
$t_{OUTCOBIDIRPLL}$	0.50	2.67	0.50	2.99			ns
$t_{XZBIDIRPLL}$		3.41		3.80			ns
$t_{ZXBIDIRPLL}$		3.41		3.80			ns

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

Table 109. Selectable I/O Standard Input Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
2.5 V		0.00		0.04		0.05	ns
1.8 V		–0.11		0.03		0.04	ns
PCI		0.01		0.09		0.10	ns
GTL+		–0.24		–0.23		–0.19	ns
SSTL-3 Class I		–0.32		–0.21		–0.47	ns
SSTL-3 Class II		–0.08		0.03		–0.23	ns
SSTL-2 Class I		–0.17		–0.06		–0.32	ns
SSTL-2 Class II		–0.16		–0.05		–0.31	ns
LVDS		–0.12		–0.12		–0.12	ns
CTT		0.00		0.00		0.00	ns
AGP		0.00		0.00		0.00	ns

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Table 111. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, EPC16 configuration devices
Passive serial (PS)	MasterBlaster or ByteBlasterMV download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information