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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

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Details

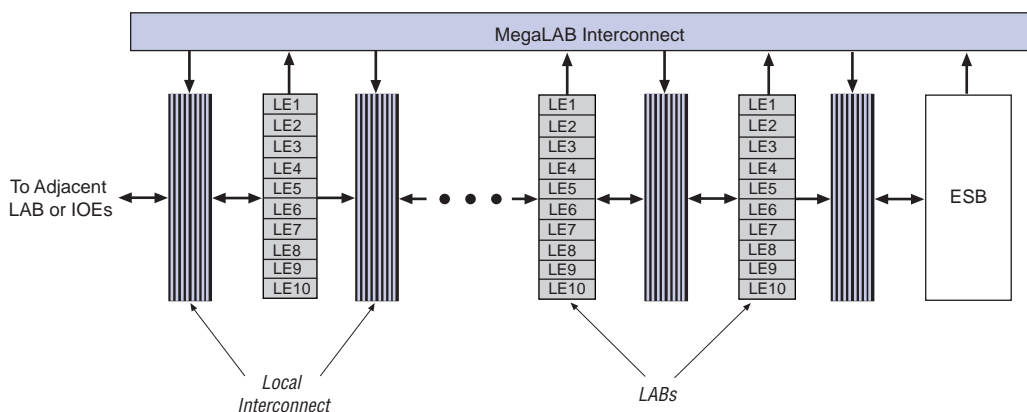
Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	376
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200efc484-2ab

APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



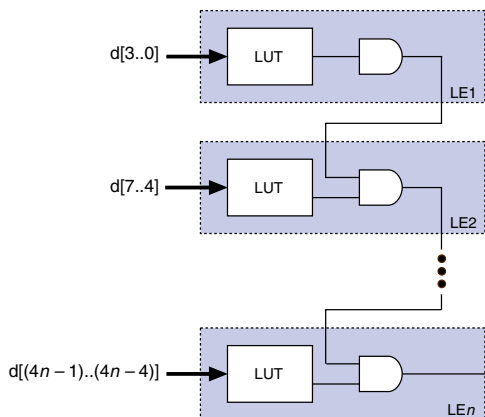
Cascade Chain

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

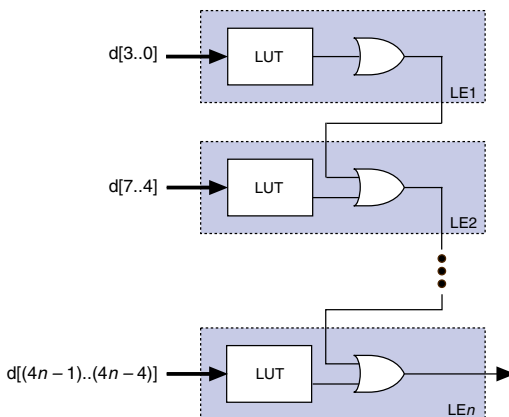
Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX 20K Cascade Chain

AND Cascade Chain



OR Cascade Chain



Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 8](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

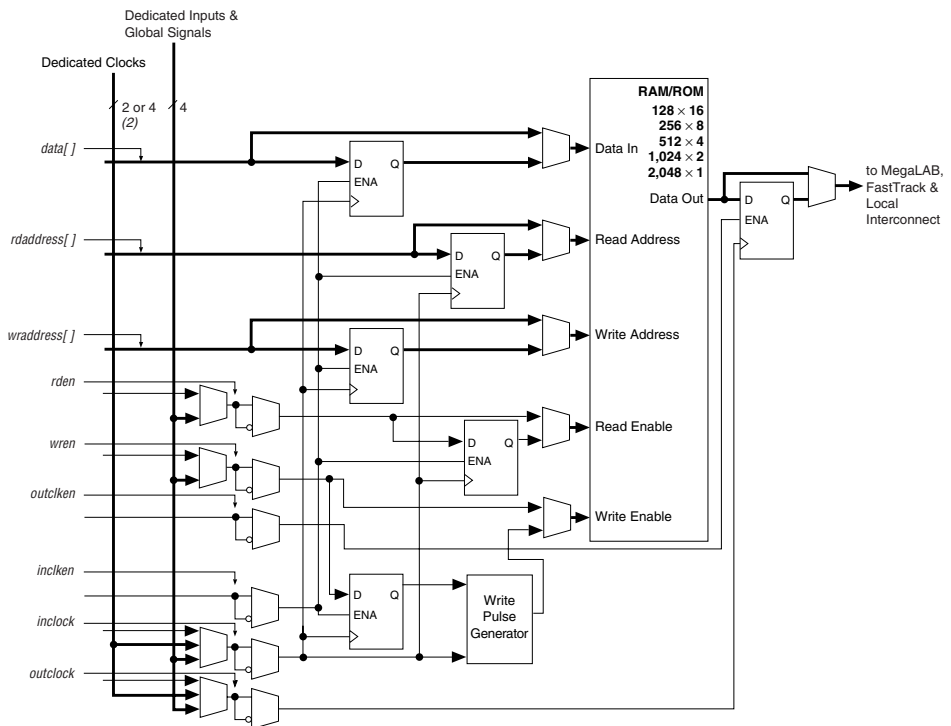
Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

Figure 21. ESB in Input/Output Clock Mode Note (1)

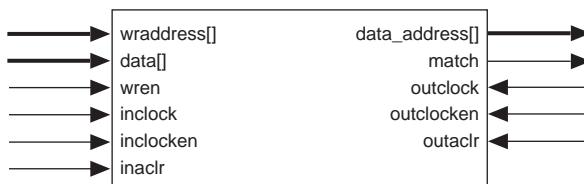


Notes to Figure 21:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

Figure 23. APEX 20KE CAM Block Diagram

CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

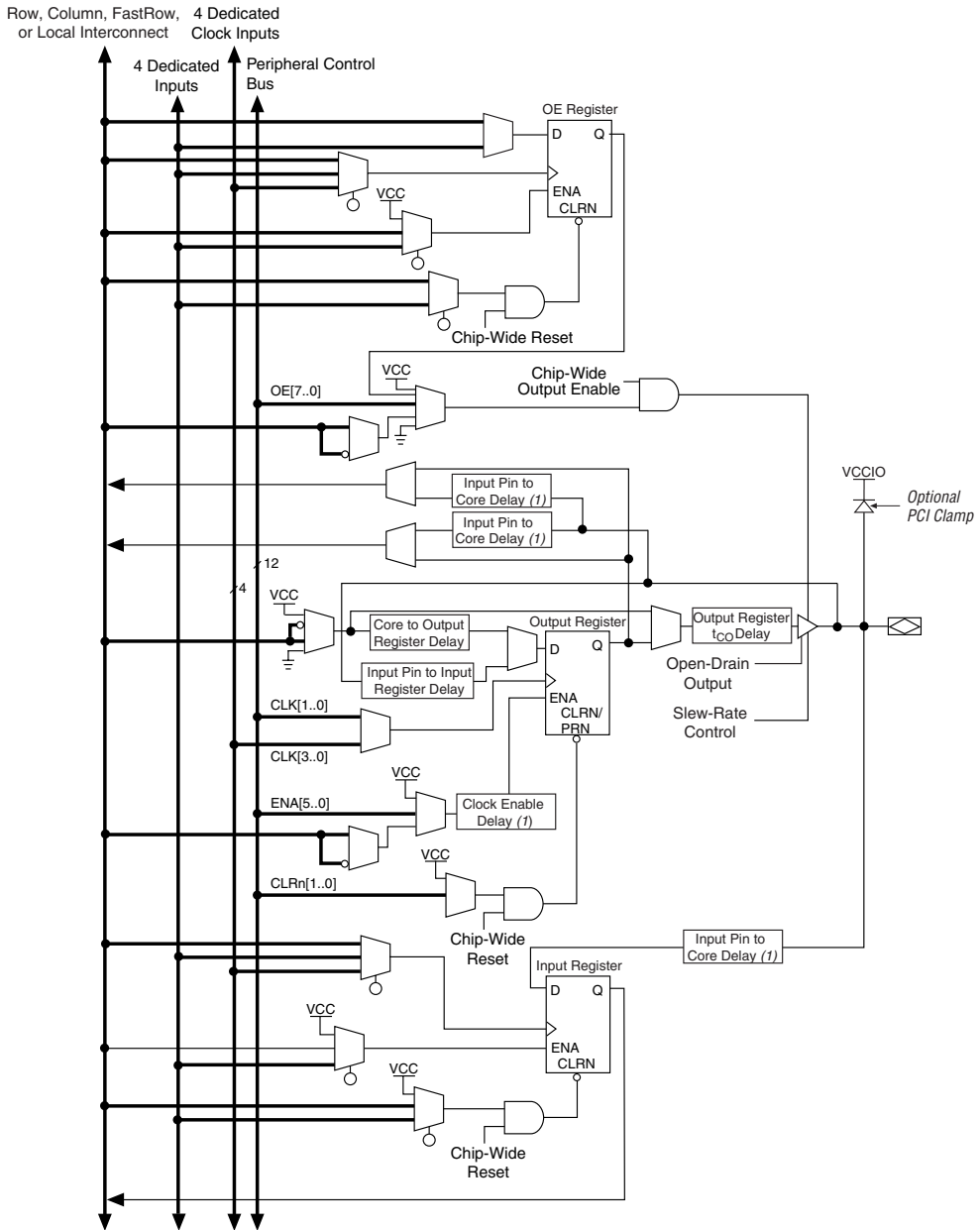
CAM supports writing “don’t care” bits into words of the memory. The “don’t-care” bit can be used as a mask for CAM comparisons; any bit set to “don’t-care” has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data’s location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM’s output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When “don’t-care” bits are used, a third clock cycle is required.

Figure 26. APEX 20KE Bidirectional I/O Registers *Notes (1), (2)*



Notes to Figure 26:

- (1) This programmable delay has four settings: off and three levels of delay.
- (2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. **Figure 27** shows how a row IOE connects to the interconnect.

Figure 27. Row IOE Connection to the Interconnect

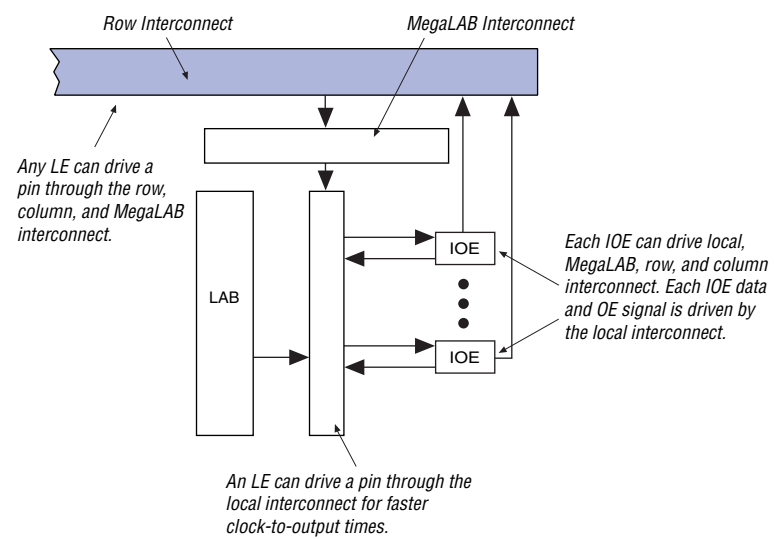
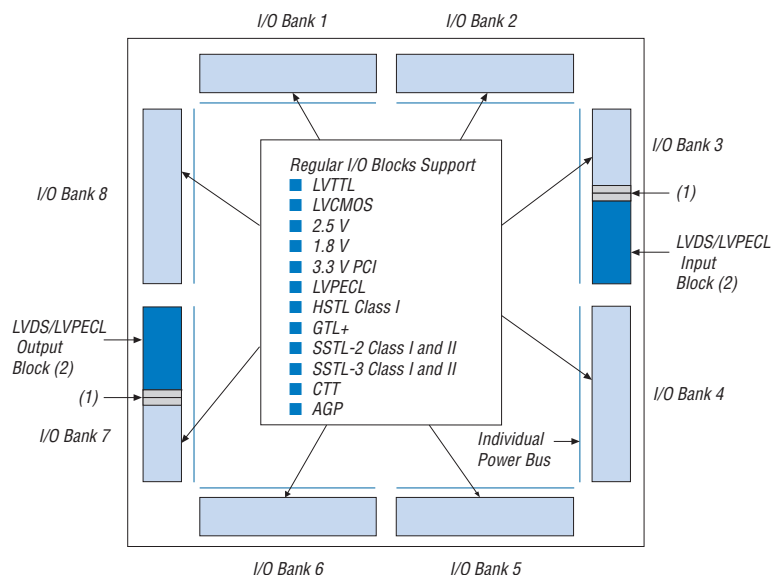


Figure 29. APEX 20KE I/O Banks

Notes to Figure 29:

- (1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices)*.
- (2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, or 1.8 V.

Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.



For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2) Note (1)

Symbol	Parameter	I/O Standard	-1X Speed Grade		-2X Speed Grade		Units
			Min	Max	Min	Max	
f_{VCO} (4)	Voltage controlled oscillator operating range		200	500	200	500	MHz
f_{CLOCK0}	clock0 PLL output frequency for internal use		1.5	335	1.5	200	MHz
f_{CLOCK1}	clock1 PLL output frequency for internal use		20	335	20	200	MHz
f_{CLOCK0_EXT}	Output clock frequency for external clock0 output	3.3-V LVTTTL	1.5	245	1.5	226	MHz
		2.5-V LVTTTL	1.5	234	1.5	221	MHz
		1.8-V LVTTTL	1.5	223	1.5	216	MHz
		GTL+	1.5	205	1.5	193	MHz
		SSTL-2 Class I	1.5	158	1.5	157	MHz
		SSTL-2 Class II	1.5	142	1.5	142	MHz
		SSTL-3 Class I	1.5	166	1.5	162	MHz
		SSTL-3 Class II	1.5	149	1.5	146	MHz
		LVDS	1.5	420	1.5	350	MHz
f_{CLOCK1_EXT}	Output clock frequency for external clock1 output	3.3-V LVTTTL	20	245	20	226	MHz
		2.5-V LVTTTL	20	234	20	221	MHz
		1.8-V LVTTTL	20	223	20	216	MHz
		GTL+	20	205	20	193	MHz
		SSTL-2 Class I	20	158	20	157	MHz
		SSTL-2 Class II	20	142	20	142	MHz
		SSTL-3 Class I	20	166	20	162	MHz
		SSTL-3 Class II	20	149	20	146	MHz
		LVDS	20	420	20	350	MHz

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. [Tables 20 and 21](#) show the boundary-scan register length and device IDCODE information for APEX 20K devices.

Table 20. APEX 20K Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP20K30E	420
EP20K60E	624
EP20K100	786
EP20K100E	774
EP20K160E	984
EP20K200	1,176
EP20K200E	1,164
EP20K300E	1,266
EP20K400	1,536
EP20K400E	1,506
EP20K600E	1,806
EP20K1000E	2,190
EP20K1500E	1 (1)

Note to [Table 20](#):

- (1) This device does not support JTAG boundary scan testing.

Table 21. 32-Bit APEX 20K Device IDCODE

Device	IDCODE (32 Bits) ⁽¹⁾			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	1 (1 Bit) ⁽²⁾
EP20K30E	0000	1000 0000 0011 0000	000 0110 1110	1
EP20K60E	0000	1000 0000 0110 0000	000 0110 1110	1
EP20K100	0000	0000 0100 0001 0110	000 0110 1110	1
EP20K100E	0000	1000 0001 0000 0000	000 0110 1110	1
EP20K160E	0000	1000 0001 0110 0000	000 0110 1110	1
EP20K200	0000	0000 1000 0011 0010	000 0110 1110	1
EP20K200E	0000	1000 0010 0000 0000	000 0110 1110	1
EP20K300E	0000	1000 0011 0000 0000	000 0110 1110	1
EP20K400	0000	0001 0110 0110 0100	000 0110 1110	1
EP20K400E	0000	1000 0100 0000 0000	000 0110 1110	1
EP20K600E	0000	1000 0110 0000 0000	000 0110 1110	1
EP20K1000E	0000	1001 0000 0000 0000	000 0110 1110	1

Notes to Table 21:

- (1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

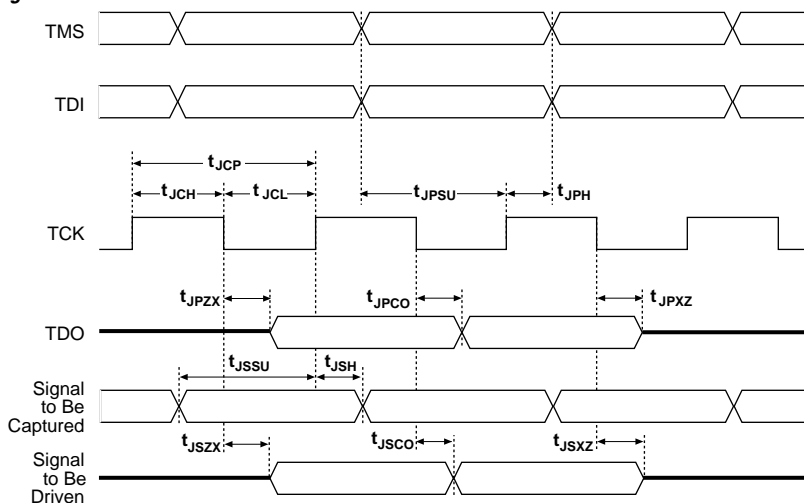
Figure 31. APEX 20K JTAG Waveforms

Table 26. APEX 20K 5.0-V Tolerant Device Capacitance *Notes (2), (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF
C_{INCLK}	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		8	pF

Notes to Tables 23 through 26:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) All APEX 20K devices are 5.0-V tolerant.
- (3) Minimum DC input is -0.5 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns .
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Maximum V_{CC} rise time is 100 ms , and V_{CC} must rise monotonically.
- (6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (7) Typical values are for $T_A = 25^\circ\text{C}$, $V_{CCINT} = 2.5\text{ V}$, and $V_{CCIO} = 2.5\text{ or }3.3\text{ V}$.
- (8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
- (9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTTL and LVC MOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in Figure 33 on page 68.
- (10) The I_{OH} parameter refers to high-level TTL, PCI or CMOS output current.
- (11) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (12) This value is specified for normal device operation. The value may vary during power-up.
- (13) Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO} .
- (14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

Table 27. APEX 20KE Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground (2)	-0.5	2.5	V
V_{CCIO}			-0.5	4.6	V
V_I			-0.5	4.6	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	$^\circ\text{C}$
T_{AMB}	Ambient temperature	Under bias	-65	135	$^\circ\text{C}$
T_J	Junction temperature	PQFP, RQFP, TQFP, and BGA packages, under bias		135	$^\circ\text{C}$
		Ceramic PGA packages, under bias		150	$^\circ\text{C}$

Table 29. APEX 20KE Device DC Operating Conditions *Notes (7), (8), (9)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level LVTTTL, CMOS, or 3.3-V PCI input voltage		1.7, $0.5 \times V_{CCIO}$ (10)		4.1	V
V_{IL}	Low-level LVTTTL, CMOS, or 3.3-V PCI input voltage		-0.5		$0.8, 0.3 \times V_{CCIO}$ (10)	V
V_{OH}	3.3-V high-level LVTTTL output voltage	$I_{OH} = -12$ mA DC, $V_{CCIO} = 3.00$ V (11)	2.4			V
	3.3-V high-level LVCMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (11)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (11)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (11)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (11)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (11)	1.7			V
V_{OL}	3.3-V low-level LVTTTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (12)			0.4	V
	3.3-V low-level LVCMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (12)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (12)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (12)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (12)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (12)			0.7	V
I_I	Input pin leakage current	$V_I = 4.1$ to -0.5 V (13)	-10		10	μ A
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = 4.1$ to -0.5 V (13)	-10		10	μ A
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	$V_I =$ ground, no load, no toggling inputs, -1 speed grade		10		mA
		$V_I =$ ground, no load, no toggling inputs, -2, -3 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (14)	20		50	k Ω
		$V_{CCIO} = 2.375$ V (14)	30		80	k Ω
		$V_{CCIO} = 1.71$ V (14)	60		150	k Ω

Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

Figure 38. ESB Asynchronous Timing Waveforms

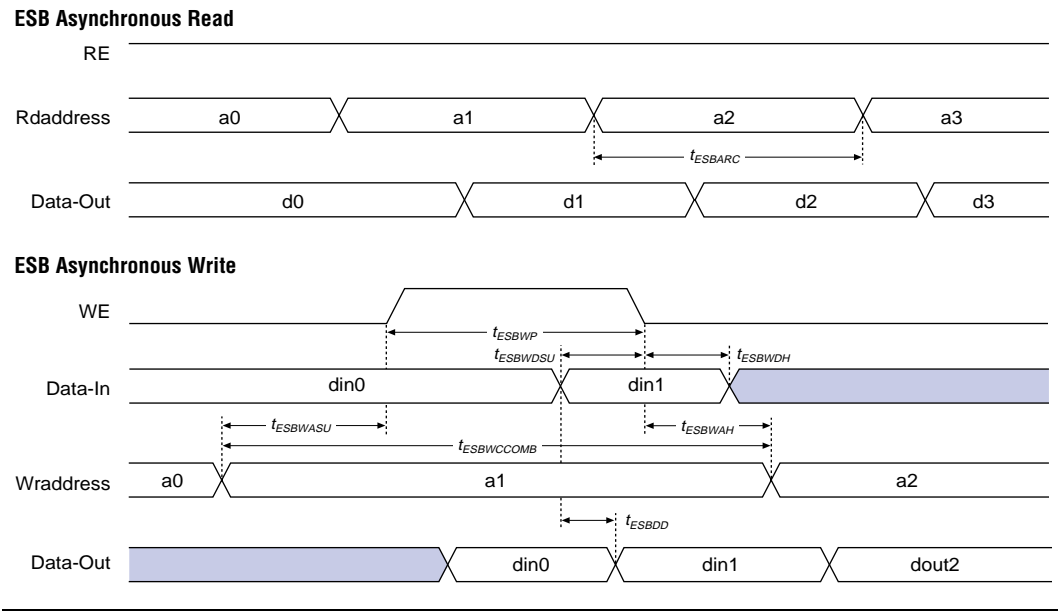
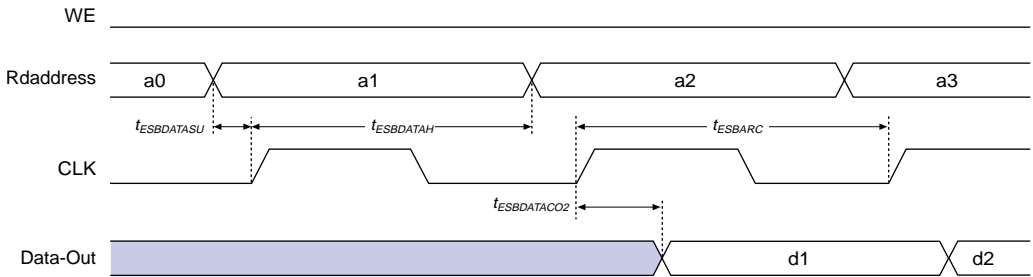


Figure 39. ESB Synchronous Timing Waveforms

ESB Synchronous Read



ESB Synchronous Write (ESB Output Registers Used)

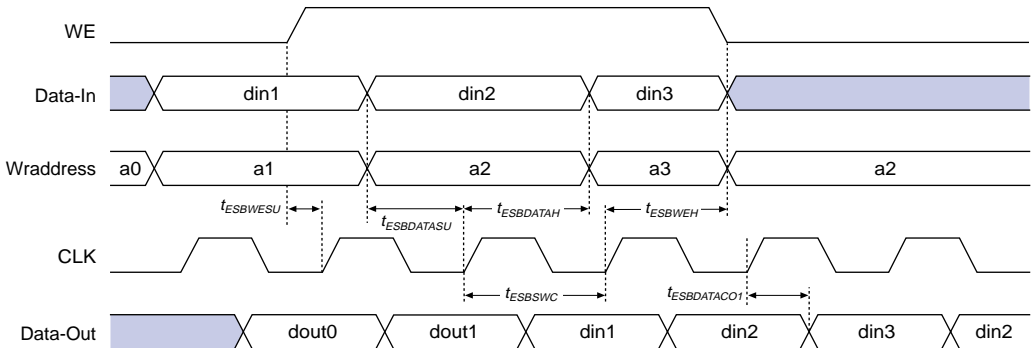


Figure 40 shows the timing model for bidirectional I/O pin timing.

Table 43. EP20K100 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU} (1)	2.3		2.8		3.2		ns
t _{INH} (1)	0.0		0.0		0.0		ns
t _{OUTCO} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t _{INSU} (2)	1.1		1.2		—		ns
t _{INH} (2)	0.0		0.0		—		ns
t _{OUTCO} (2)	0.5	2.7	0.5	3.1	—	4.8	ns

Table 44. EP20K100 External Bidirectional Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSUBIDIR} (1)	2.3		2.8		3.2		ns
t _{INHBIDIR} (1)	0.0		0.0		0.0		ns
t _{OUTCOBIDIR} (1)	2.0	4.5	2.0	4.9	2.0	6.6	ns
t _{XZBIDIR} (1)		5.0		5.9		6.9	ns
t _{ZXBIDIR} (1)		5.0		5.9		6.9	ns
t _{INSUBIDIR} (2)	1.0		1.2		—		ns
t _{INHBIDIR} (2)	0.0		0.0		—		ns
t _{OUTCOBIDIR} (2)	0.5	2.7	0.5	3.1	—	—	ns
t _{XZBIDIR} (2)		4.3		5.0		—	ns
t _{ZXBIDIR} (2)		4.3		5.0		—	ns

Table 45. EP20K200 External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t _{INSU} (1)	1.9		2.3		2.6		ns
t _{INH} (1)	0.0		0.0		0.0		ns
t _{OUTCO} (1)	2.0	4.6	2.0	5.6	2.0	6.8	ns
t _{INSU} (2)	1.1		1.2		—		ns
t _{INH} (2)	0.0		0.0		—		ns
t _{OUTCO} (2)	0.5	2.7	0.5	3.1	—	—	ns

Table 60. EP20K60E External Bidirectional Timing Parameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.77		2.91		3.11		ns
t_{INHBIDIR}	0.00		0.00		0.00		ns
$t_{\text{OUTCOBIDIR}}$	2.00	4.84	2.00	5.31	2.00	5.81	ns
t_{XZBIDIR}		6.47		7.44		8.65	ns
t_{ZXBIDIR}		6.47		7.44		8.65	ns
$t_{\text{INSUBIDIRPLL}}$	3.44		3.24		-		ns
$t_{\text{INHBIDIRPLL}}$	0.00		0.00		-		ns
$t_{\text{OUTCOBIDIRPLL}}$	0.50	3.37	0.50	3.69	-	-	ns
$t_{\text{XZBIDIRPLL}}$		5.00		5.82		-	ns
$t_{\text{ZXBIDIRPLL}}$		5.00		5.82		-	ns

Tables 61 through 66 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

Table 61. EP20K100E f_{MAX} LE Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.25		0.25		ns
t_{H}	0.25		0.25		0.25		ns
t_{CO}		0.28		0.28		0.34	ns
t_{LUT}		0.80		0.95		1.13	ns

Table 62. EP20K100E t_{MAX} ESB Timing Microparameters

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.61		1.84		1.97	ns
t_{ESBSRC}		2.57		2.97		3.20	ns
t_{ESBAWC}		0.52		4.09		4.39	ns
t_{ESBSWC}		3.17		3.78		4.09	ns
$t_{ESBWASU}$	0.56		6.41		0.63		ns
t_{ESBWAH}	0.48		0.54		0.55		ns
$t_{ESBWDSU}$	0.71		0.80		0.81		ns
t_{ESBWDH}	.048		0.54		0.55		ns
$t_{ESBRASU}$	1.57		1.75		1.87		ns
t_{ESBRAH}	0.00		0.00		0.20		ns
$t_{ESBWESU}$	1.54		1.72		1.80		ns
t_{ESBWEH}	0.00		0.00		0.00		ns
$t_{ESBDATASU}$	-0.16		-0.20		-0.20		ns
$t_{ESBDATAH}$	0.13		0.13		0.13		ns
$t_{ESBWADDRSU}$	0.12		0.08		0.13		ns
$t_{ESBRADDRSU}$	0.17		0.15		0.19		ns
$t_{ESBDATAO1}$		1.20		1.39		1.52	ns
$t_{ESBDATAO2}$		2.54		2.99		3.22	ns
t_{ESBDD}		3.06		3.56		3.85	ns
t_{PD}		1.73		2.02		2.20	ns
$t_{PTERMSU}$	1.11		1.26		1.38		ns
$t_{PTERMCO}$		1.19		1.40		1.08	ns

Table 63. EP20K100E t_{MAX} Routing Delays

Symbol	-1		-2		-3		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.24		0.27		0.29	ns
t_{F5-20}		1.04		1.26		1.52	ns
t_{F20+}		1.12		1.36		1.86	ns

Table 87. EP20K400E t_{MAX} Routing Delays

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}		0.25		0.25		0.26	ns
t_{F5-20}		1.01		1.12		1.25	ns
t_{F20+}		3.71		3.92		4.17	ns

Table 88. EP20K400E Minimum Pulse Width Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.36		2.22		2.35		ns
t_{CL}	1.36		2.26		2.35		ns
t_{CLRP}	0.18		0.18		0.19		ns
t_{PREP}	0.18		0.18		0.19		ns
t_{ESBCH}	1.36		2.26		2.35		ns
t_{ESBCL}	1.36		2.26		2.35		ns
t_{ESBWP}	1.17		1.38		1.56		ns
t_{ESBRP}	0.94		1.09		1.25		ns

Table 89. EP20K400E External Timing Parameters

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.51		2.64		2.77		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	5.25	2.00	5.79	2.00	6.32	ns
$t_{INSUPLL}$	3.221		3.38		-		ns
t_{INHPLL}	0.00		0.00		-		ns
$t_{OUTCOPLL}$	0.50	2.25	0.50	2.45	-	-	ns

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- t_{ESBWEH} added to [Figure 37](#) and [Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104](#).
- Updated EP20K300E device internal and external timing numbers in [Tables 79 through 84](#).