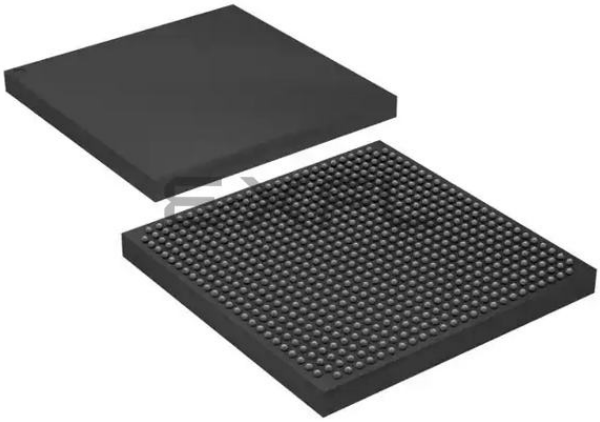

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 832 |
| Number of Logic Elements/Cells | 8320 |
| Total RAM Bits | 106496 |
| Number of I/O | 376 |
| Number of Gates | 526000 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep20k200efc672-3 |

## General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices.

*Table 8. Comparison of APEX 20K & APEX 20KE Features*

| Feature | APEX 20K Devices | APEX 20KE Devices |
|---|---|---|
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

### *LE Operating Modes*

The APEX 20K LE can operate in one of the following three modes:

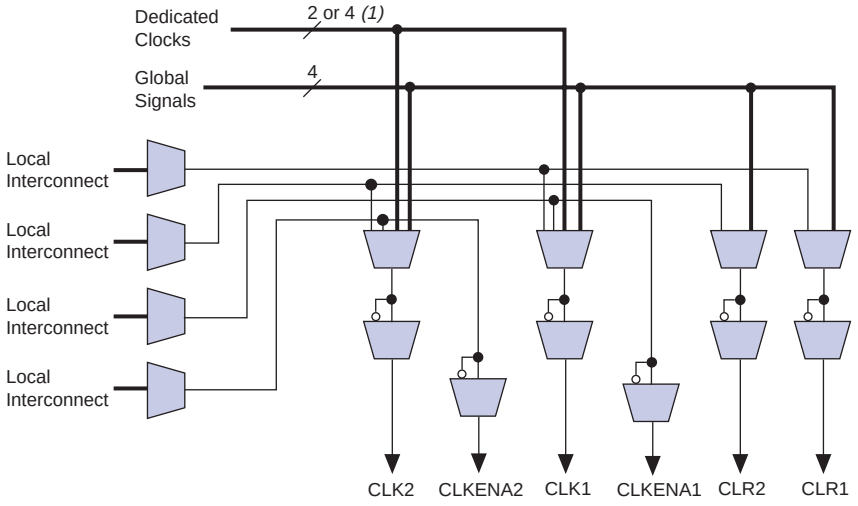
- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*




*Note to Figure 15:*
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

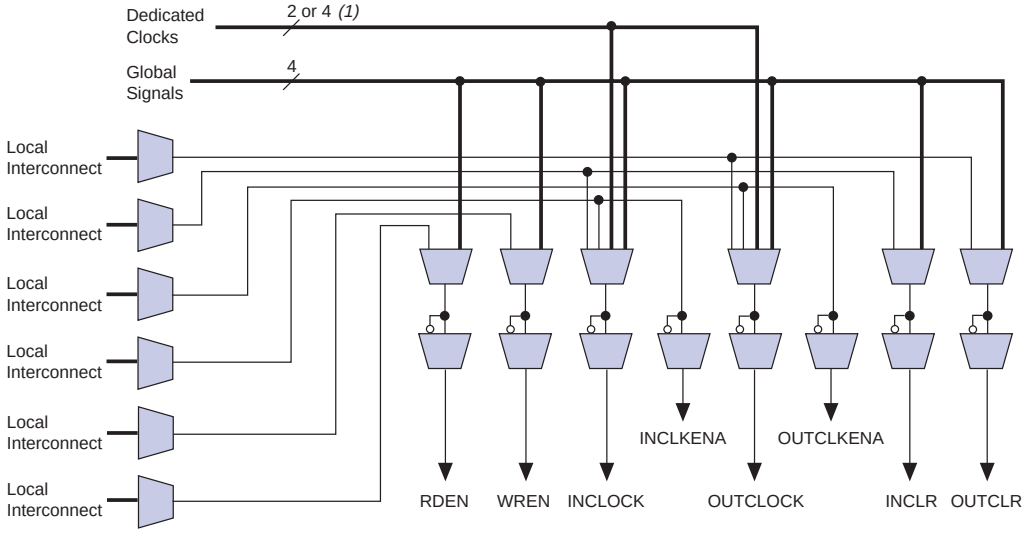
To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

***Figure 24. ESB Control Signal Generation***




*Note to Figure 24:*
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

*Table 11. APEX 20KE Programmable Delay Chains*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input Pin to Core Delay | Decrease input delay to internal cells |
| Input Pin to Input Register Delay | Decrease input delay to input registers |
| Core to Output Register Delay | Decrease input delay to output register |
| Output Register $t_{CO}$ Delay | Increase delay to output pin |
| Clock Enable Delay | Increase clock enable delay |

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

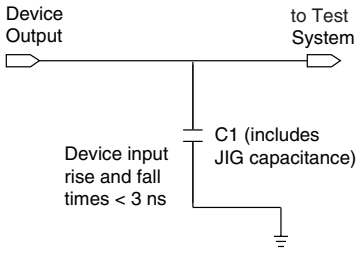
The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

*Table 20. APEX 20K Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K30E | 420 |
| EP20K60E | 624 |
| EP20K100 | 786 |
| EP20K100E | 774 |
| EP20K160E | 984 |
| EP20K200 | 1,176 |
| EP20K200E | 1,164 |
| EP20K300E | 1,266 |
| EP20K400 | 1,536 |
| EP20K400E | 1,506 |
| EP20K600E | 1,806 |
| EP20K1000E | 2,190 |
| EP20K1500E | 1 *(1)* |

***Note to Table 20:***
(1) This device does not support JTAG boundary scan testing.

*Figure 32. APEX 20K AC Test Conditions* *Note (1)*




*Note to Figure 32:*

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

*Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings* *Notes (1), (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(3)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(11)* | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade *(12)* | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades *(12)* | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | W |
| | | $V_{CCIO}$ = 2.375 V *(13)* | 30 | | 80 | W |

*Figure 33. Relationship between $V_{CCIO}$ & $V_{CCINT}$ for 3.3-V PCI Compliance*

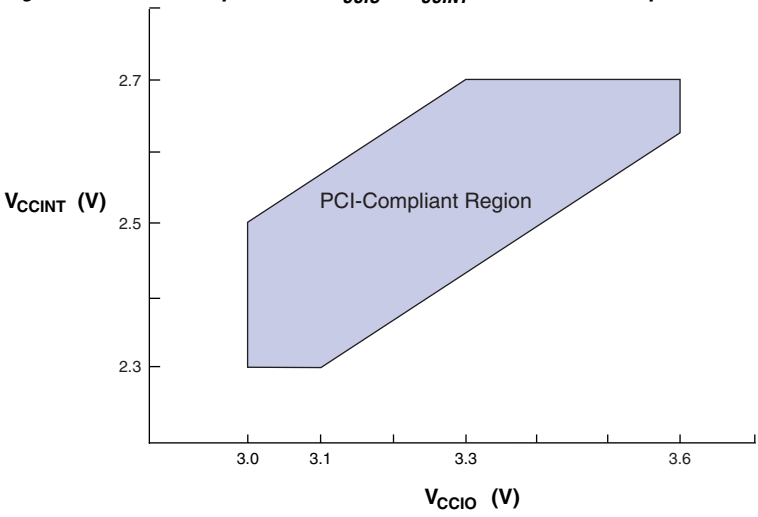
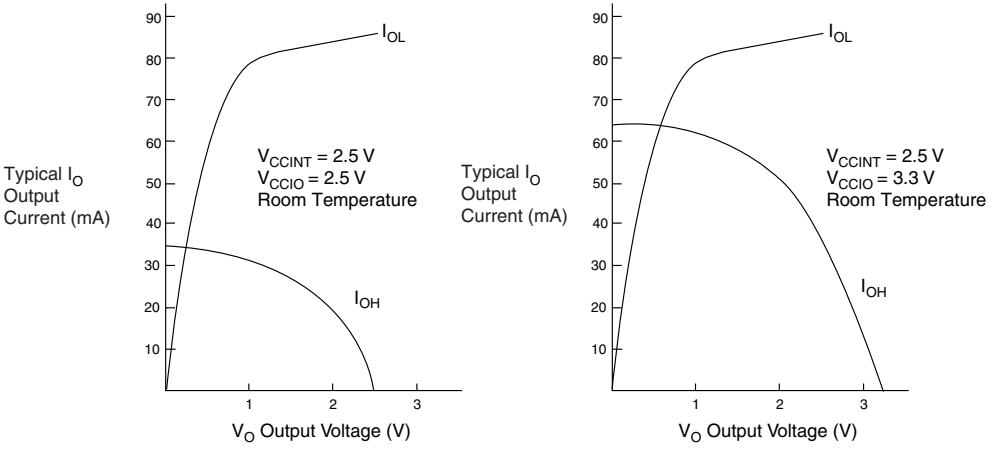



Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when VCCIO pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

*Figure 34. Output Drive Characteristics of APEX 20K Device* *Note (1)*




*Note to Figure 34:*
(1) These are transient (AC) currents.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the $f_{MAX}$ timing model for APEX 20K devices.

*Figure 36. APEX 20K $f_{MAX}$ Timing Model*

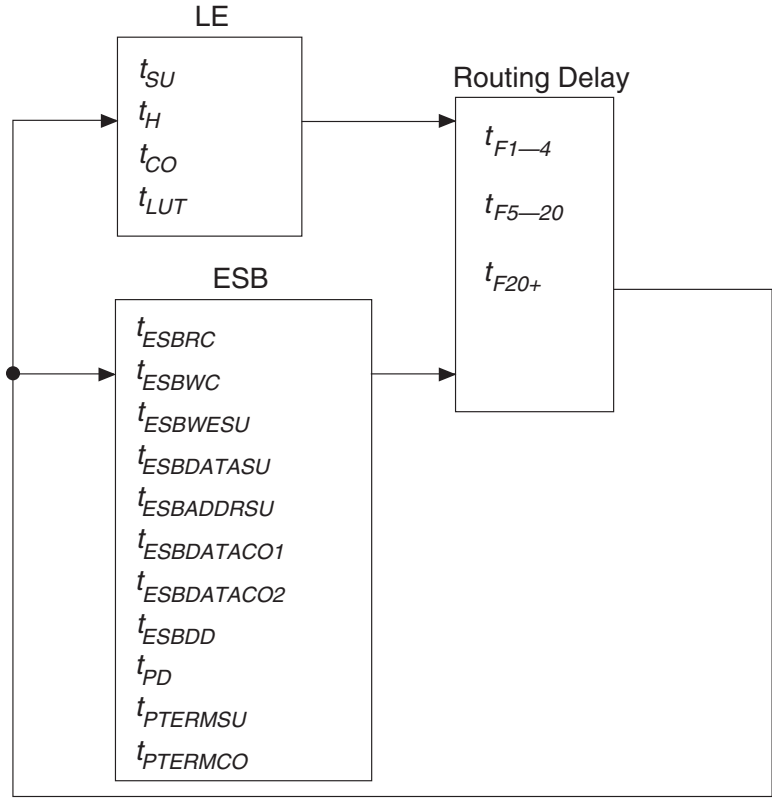



Figure 37 shows the $f_{MAX}$ timing model for APEX 20KE devices. These parameters can be used to estimate $f_{MAX}$ for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

*Table 42. EP20K400 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.1 | | 0.3 | | 0.6 | | ns |
| $t_{H}$ | 0.5 | | 0.8 | | 0.9 | | ns |
| $t_{CO}$ | | 0.1 | | 0.4 | | 0.6 | ns |
| $t_{LUT}$ | | 1.0 | | 1.2 | | 1.4 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.5 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.1 | | 3.6 | ns |
| $t_{PTERMSU}$ | 1.7 | | 2.1 | | 2.4 | | ns |
| $t_{PTERMCO}$ | | 1.0 | | 1.2 | | 1.4 | ns |
| $t_{F1-4}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{F5-20}$ | | 2.6 | | 2.8 | | 2.9 | ns |
| $t_{F20+}$ | | 3.7 | | 3.8 | | 3.9 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.5 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.2 | | 1.4 | | ns |

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

*Table 51. EP20K30E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

*Table 62. EP20K100E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.61 | | 1.84 | | 1.97 | ns |
| $t_{ESBSRC}$ | | 2.57 | | 2.97 | | 3.20 | ns |
| $t_{ESBAWC}$ | | 0.52 | | 4.09 | | 4.39 | ns |
| $t_{ESBSWC}$ | | 3.17 | | 3.78 | | 4.09 | ns |
| $t_{ESBWASU}$ | 0.56 | | 6.41 | | 0.63 | | ns |
| $t_{ESBWAH}$ | 0.48 | | 0.54 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.71 | | 0.80 | | 0.81 | | ns |
| $t_{ESBWDH}$ | .048 | | 0.54 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.57 | | 1.75 | | 1.87 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.20 | | ns |
| $t_{ESBWESU}$ | 1.54 | | 1.72 | | 1.80 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.16 | | -0.20 | | -0.20 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.12 | | 0.08 | | 0.13 | | ns |
| $t_{ESBRADDRSU}$ | 0.17 | | 0.15 | | 0.19 | | ns |
| $t_{ESBDATACO1}$ | | 1.20 | | 1.39 | | 1.52 | ns |
| $t_{ESBDATACO2}$ | | 2.54 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.06 | | 3.56 | | 3.85 | ns |
| $t_{PD}$ | | 1.73 | | 2.02 | | 2.20 | ns |
| $t_{PTERMSU}$ | 1.11 | | 1.26 | | 1.38 | | ns |
| $t_{PTERMCO}$ | | 1.19 | | 1.40 | | 1.08 | ns |

*Table 63. EP20K100E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.04 | | 1.26 | | 1.52 | ns |
| $t_{F20+}$ | | 1.12 | | 1.36 | | 1.86 | ns |

*Table 74. EP20K200E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.68 | | 2.06 | | 2.24 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 2.77 | | 3.18 | ns |
| $t_{ESBAWC}$ | | 3.10 | | 3.86 | | 4.50 | ns |
| $t_{ESBSWC}$ | | 2.90 | | 3.67 | | 4.21 | ns |
| $t_{ESBWASU}$ | 0.55 | | 0.67 | | 0.74 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.83 | | 0.95 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.90 | | 2.09 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.42 | | 1.71 | | 2.01 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.06 | | -0.07 | | 0.05 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.13 | | 0.31 | | ns |
| $t_{ESBRADDRSU}$ | 0.18 | | 0.23 | | 0.39 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.35 | | 1.51 | ns |
| $t_{ESBDATACO2}$ | | 2.19 | | 2.75 | | 3.22 | ns |
| $t_{ESBDD}$ | | 2.75 | | 3.41 | | 4.03 | ns |
| $t_{PD}$ | | 1.58 | | 1.97 | | 2.33 | ns |
| $t_{PTERMSU}$ | 1.00 | | 1.22 | | 1.51 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.37 | | 1.09 | ns |

*Table 75. EP20K200E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.02 | | 1.20 | | 1.41 | ns |
| $t_{F20+}$ | | 1.99 | | 2.23 | | 2.53 | ns |

*Table 78. EP20K200E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.81 | | 3.19 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.12 | 2.00 | 5.62 | 2.00 | 6.11 | ns |
| $t_{XZBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{ZXBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{INSUBIDIRPLL}$ | 3.30 | | 3.64 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.01 | 0.50 | 3.36 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |

Tables 79 through 84 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

*Table 79. EP20K300E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.17 | | 0.18 | | ns |
| $t_{H}$ | 0.31 | | 0.33 | | 0.38 | | ns |
| $t_{CO}$ | | 0.28 | | 0.38 | | 0.51 | ns |
| $t_{LUT}$ | | 0.79 | | 1.07 | | 1.43 | ns |

*Table 92. EP20K600E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 2.39 | | 3.11 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 3.07 | | 3.86 | ns |
| $t_{ESBAWC}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{ESBSWC}$ | | 3.51 | | 4.62 | | 5.72 | ns |
| $t_{ESBWASU}$ | 1.46 | | 2.08 | | 2.70 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.60 | | 2.29 | | 2.97 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 2.30 | | 2.99 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.49 | | 2.30 | | 3.11 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.01 | | 0.35 | | 0.71 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.19 | | 0.62 | | 1.06 | | ns |
| $t_{ESBRADDRSU}$ | 0.25 | | 0.71 | | 1.17 | | ns |
| $t_{ESBDATACO1}$ | | 1.01 | | 1.19 | | 1.37 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 3.12 | | 4.05 | ns |
| $t_{ESBDD}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{PD}$ | | 1.57 | | 2.25 | | 2.92 | ns |
| $t_{PTERMSU}$ | 0.85 | | 1.43 | | 2.01 | | ns |
| $t_{PTERMCO}$ | | 1.03 | | 1.21 | | 1.39 | ns |

*Table 93. EP20K600E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.26 | | 1.39 | | 1.52 | ns |
| $t_{F20+}$ | | 3.51 | | 3.88 | | 4.26 | ns |

*Table 106. EP20K1500E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 107. EP20K1500E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.09 | | 3.30 | | 3.58 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 6.18 | 2.00 | 6.81 | 2.00 | 7.36 | ns |
| $t_{INSUPLL}$ | 1.94 | | 2.08 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.67 | 0.50 | 2.99 | - | - | ns |

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$ added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.