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Intel - EP20K200EQC240-2 Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	8320
Total RAM Bits	106496
Number of I/O	168
Number of Gates	526000
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep20k200eqc240-2

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All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industrystandard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.





Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higherorder bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB[™] structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in n + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

LE Operating Modes

The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.



Figure 15. ESB Product-Term Mode Control Logic

(1) APEX 20KE devices have four dedicated clocks.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.



Notes to Figure 20:

- (1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
- (2) APEX 20KE devices have four dedicated clocks.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit[™] option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

Table 14. Multiplication Factor Combinations				
Clock 1	Clock 2			
×1	×1			
×1, ×2	×2			
×1, ×2, ×4	×4			

APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

External PLL Feedback

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

Clock Multiplication

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where *m* and *k* range from 2 to 160, and *n* and *v* range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

Symbol	Parameter	Min	Max	Unit				
t _{JCP}	TCK clock period	100		ns				
t _{JCH}	TCK clock high time	50		ns				
t _{JCL}	TCK clock low time	50		ns				
t _{JPSU}	JTAG port setup time	20		ns				
t _{JPH}	JTAG port hold time	45		ns				
t _{JPCO}	JTAG port clock to output		25	ns				
t _{JPZX}	JTAG port high impedance to valid output		25	ns				
t _{JPXZ}	JTAG port valid output to high impedance		25	ns				
t _{JSSU}	Capture register setup time	20		ns				
t _{JSH}	Capture register hold time	45		ns				
t _{JSCO}	Update register clock to output		35	ns				
t _{JSZX}	Update register high impedance to valid output		35	ns				
t _{JSXZ}	Update register valid output to high impedance		35	ns				

Table 22. APEX 20K JTAG Timing Parameters & Values

For more information, see the following documents:

- Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)
- Jam Programming & Test Language Specification

Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.



Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compatible with the 3.3-V *PCI Local Bus Specification, Revision 2.2* (when VCCIO pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.







Altera Corporation

Figure 39. ESB Synchronous Timing Waveforms



ESB Synchronous Write (ESB Output Registers Used)



Figure 40 shows the timing model for bidirectional I/O pin timing.

Table 36. APEX 20KE Routing Timing Microparameters Note (1)						
Symbol	Parameter					
t _{F1-4}	Fanout delay using Local Interconnect					
t _{F5-20}	Fanout delay estimate using MegaLab Interconnect					
t _{F20+}	Fanout delay estimate using FastTrack Interconnect					

Note to Table 36:

 These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

Table 37. APEX ZUKE FUNCTIONAL TIMING MICROPARAMETERS					
Symbol	Parameter				
ТСН	Minimum clock high time from clock pin				
TCL	Minimum clock low time from clock pin				
TCLRP	LE clear Pulse Width				
TPREP	LE preset pulse width				
TESBCH	Clock high time for ESB				
TESBCL	Clock low time for ESB				
TESBWP	Write pulse width				
TESBRP	Read pulse width				

Table 37. APEX 20KE Functional Timing Microparameters

Tables 38 and 39 describe the APEX 20KE external timing parameters.

Table 38. APEX 20KE External Timing Parameters Note (1)							
Symbol	Symbol Clock Parameter Condi						
t _{INSU}	Setup time with global clock at IOE input register						
t _{INH}	Hold time with global clock at IOE input register						
t _{оитсо}	Clock-to-output delay with global clock at IOE output register	C1 = 10 pF					
t _{INSUPLL}	Setup time with PLL clock at IOE input register						
t _{INHPLL}	Hold time with PLL clock at IOE input register						
t _{OUTCOPLL}	Clock-to-output delay with PLL clock at IOE output register	C1 = 10 pF					

Tables 67 through 72 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

Table 67. EP20K160E f _{MAX} LE Timing Microparameters										
Symbol	-1		ol -1 -2		-	Unit				
	Min	Max	Min	Max	Min	Max				
t _{SU}	0.22		0.24		0.26		ns			
t _H	0.22		0.24		0.26		ns			
t _{CO}		0.25		0.31		0.35	ns			
t _{LUT}		0.69		0.88		1.12	ns			

Table 76. EP20K200E Minimum Pulse Width Timing Parameters									
Symbol		1	-	-2		-3			
	Min	Max	Min	Max	Min	Max			
t _{CH}	1.36		2.44		2.65		ns		
t _{CL}	1.36		2.44		2.65		ns		
t _{CLRP}	0.18		0.19		0.21		ns		
t _{PREP}	0.18		0.19		0.21		ns		
t _{ESBCH}	1.36		2.44		2.65		ns		
t _{ESBCL}	1.36		2.44		2.65		ns		
t _{ESBWP}	1.18		1.48		1.76		ns		
t _{ESBRP}	0.95		1.17		1.41		ns		

Table 77. EP20K200E External Timing Parameters									
Symbol	-	-1		-2		-3			
	Min	Max	Min	Max	Min	Max			
t _{INSU}	2.24		2.35		2.47		ns		
t _{INH}	0.00		0.00		0.00		ns		
t _{outco}	2.00	5.12	2.00	5.62	2.00	6.11	ns		
t _{INSUPLL}	2.13		2.07		-		ns		
t _{INHPLL}	0.00		0.00		-		ns		
t _{outcopll}	0.50	3.01	0.50	3.36	-	-	ns		

Table 92. EP20k	Table 92. EP20K600E f _{MAX} ESB Timing Microparameters								
Symbol	-1 Spee	ed Grade	-2 Spe	-2 Speed Grade		-3 Speed Grade			
	Min	Max	Min	Max	Min	Max			
t _{ESBARC}		1.67		2.39		3.11	ns		
t _{ESBSRC}		2.27		3.07		3.86	ns		
t _{ESBAWC}		3.19		4.56		5.93	ns		
t _{ESBSWC}		3.51		4.62		5.72	ns		
t _{ESBWASU}	1.46		2.08		2.70		ns		
t _{ESBWAH}	0.00		0.00		0.00		ns		
t _{ESBWDSU}	1.60		2.29		2.97		ns		
t _{ESBWDH}	0.00		0.00		0.00		ns		
t _{ESBRASU}	1.61		2.30		2.99		ns		
t _{ESBRAH}	0.00		0.00		0.00		ns		
t _{ESBWESU}	1.49		2.30		3.11		ns		
t _{ESBWEH}	0.00		0.00		0.00		ns		
t _{ESBDATASU}	-0.01		0.35		0.71		ns		
t _{ESBDATAH}	0.13		0.13		0.13		ns		
t _{ESBWADDRSU}	0.19		0.62		1.06		ns		
t _{ESBRADDRSU}	0.25		0.71		1.17		ns		
t _{ESBDATACO1}		1.01		1.19		1.37	ns		
t _{ESBDATACO2}		2.18		3.12		4.05	ns		
t _{ESBDD}		3.19		4.56		5.93	ns		
t _{PD}		1.57		2.25		2.92	ns		
t _{PTERMSU}	0.85		1.43		2.01		ns		
t _{PTERMCO}		1.03		1.21		1.39	ns		

Table 93. EP20K600E f _{MAX} Routing Delays									
Symbol	-1 Spe	-1 Speed Grade		-2 Speed Grade		ed Grade	Unit		
	Min	Max	Min	Max	Min	Max			
t _{F1-4}		0.22		0.25		0.26	ns		
t _{F5-20}		1.26		1.39		1.52	ns		
t _{F20+}		3.51		3.88		4.26	ns		

Tables 97 through 102 describe f_{MAX} LE Timing Microparameters, f_{MAX} ESB Timing Microparameters, f_{MAX} Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

Table 97. EP20K1000E f _{MAX} LE Timing Microparameters									
Symbol	-1 Speed Grade		ol -1 Speed Grade -2 Speed Grade		-3 Spee	Unit			
	Min	Max	Min	Max	Min	Max			
t _{SU}	0.25		0.25		0.25		ns		
t _H	0.25		0.25		0.25		ns		
t _{CO}		0.28		0.32		0.33	ns		
t _{LUT}		0.80		0.95		1.13	ns		

Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

Version 5.1

APEX 20K Programmable Logic Device Family Data Sheet version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note* (5) to Tables 27 through 30 was revised.
- Added *Note* (2) to Figure 21 on page 33.

Version 5.0

APEX 20K Programmable Logic Device Family Data Sheet version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for t_{ESBDATAH} parameter.

Version 4.3

APEX 20K Programmable Logic Device Family Data Sheet version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note* (2) to Table 13.
- Updated notes to Tables 27 through 30.

Version 4.2

APEX 20K Programmable Logic Device Family Data Sheet version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note* (1) to Figure 29.

Version 4.1

APEX 20K Programmable Logic Device Family Data Sheet version 4.1 contains the following changes:

- *t*_{ESBWEH} added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.